Journal of Engineering and Applied Sciences 8 (9-12): 269-272, 2013
ISSN: 1816-949X

Design of 4-Bit Memory Column Dram Cell in 0.18 μm CMOS Process

Nasima Sedaghati, Md. Mamun, Labonnah F. Rahman and Hafizah Husain
Department of Electrical, Electronic and Systems Engineering,
Universiti Kebangsaan Malaysia, 43600 Bangi, Selangor, Malaysia

Abstract: A Dynamic Random Access Memories (DRAM) memory cell is a capacitor that is charged to produce a 1 or a 0. Over the years, several different structures have been used to create the memory cells on a chip. In today's technologies, the capacitive storage element of the memory cell is used to create trenched filled with dielectric material. However to progress to the next generation DRAM, all the major physical limitations like circuit complexity, longer read/write times and delays of the 1-Transistor (1-T) and capacitor storage cell need to overcome. In this research, a 4-bit memory column cell for DRAM is presented. To design the column cell, 3-transistor DRAM is chosen as it is distinguished from the one transistor cell to rely on a driver transistor. Moreover, the column cell operates as a constant current source during the discharge of the bit-line. CEDEC 0.18 μm CMOS process has been utilized to design the column cell. Therefore, the simulated results show that the designed circuit has been operates successfully to comply with the DRAM.

Key words: DRAM, 4-bit memory column, 3-transistor, DRAM cell, Malaysia

INTRODUCTION

Memory cell is a fundamental component in any storage device. Column cell circuit is very important element in memory systems design (Akter *et al*., 2008a, b; Reaz *et al*., 2003, 2005, 2007a, b; Marufuzzaman *et al*., 2010). Devices, such as computer require a large data facility to store program instructions and data. A read/write memory provides a solution for this storage problem. There are two types of read-write memory like Static Random Access Memory (SRAM) and DRAM. SRAM stores data as long as power supply is supplied to the memory (Reaz *et al*., 2006; Reaz and Wei, 2004; Mohd-Yasin *et al*., 2004; Mogaki *et al*., 2007). The manufacture of SRAM involves the use of six transistors per cell. The main advantages to SRAM are differential and very fast (Verma and Chandrakasan, 2008). On the other hand, the disadvantages are the size of the memory. Due to the high transistor count of SRAM it is expensive and impractical to build such memory to store large amounts of data. Therefore, SRAM is manufactured with low densities (Chang *et al*., 2009).

Semiconductors are one of the most important inventions of all time in the world. DRAM is a read-write memory which fulfills the large data and program to use as the storage for the computers with a typical DRAM size 64 MB (Xie, 2011). Higher memory density, low power dissipation and lower transistor count (1-3 transistors per cell) are the advantages of DRAM. On the other hand, the expenses of added circuit complexity, longer read and write times and delays due to refresh requirements are the disadvantages of DRAM. Moreover, DRAM cannot hold data for long without being refreshed. The DRAM cell uses an aggressive 3-transistor implementation with 1-transistor functionality as the read port, one as the write port and the third as a storage device to store a binary bit by means of gate capacitance. Besides having fewer transistors than a SRAM implementation, the 3-transistor DRAM cell uses solely in NMOS devices and achieves greater speed without the larger and slower P-devices (Chun *et al*., 2012).

This study presents an improved 4-bit memory column using DRAM cell circuit which is designed using CEDEC 0.18 μm CMOS process. Firstly, the study is discussed with the DRAM cell operation process. Then, the design methodology of the 4-bit memory column circuits is presented. After that the simulated results, the comparison study among other designed memory column circuits and conclusions are given, respectively.

DRAM CELL OPERATION

Two types of DRAM cell are used for CMOS designing. The 1-Transistor (1-T) cell has been dominating the DRAM market for the last 30 years due to its smallest cell size (Agrawal *et al*., 1994). The cell structure is extremely simple and the most straight forward among all the memories. Figure 1 illustrates

Corresponding Author: Md. Mamun, Department of Electrical, Electronic and Systems Engineering,
Universiti Kebangsaan Malaysia, 43600 Bangi, Selangor, Malaysia

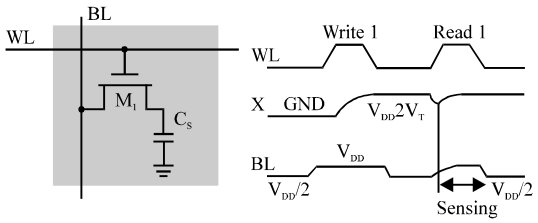

Fig. 1: The 1-transistor DRAM cell (Leiss *et al*., 1982)

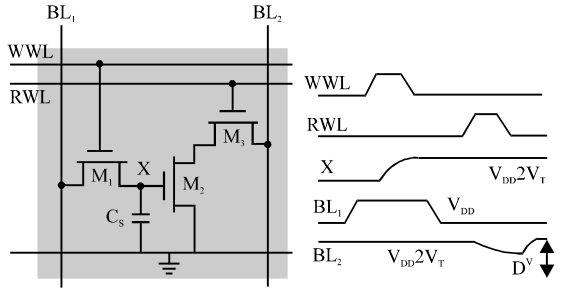

Fig. 2: The 3-transistor DRAM cell (Diodato *et al*., 1997)

the 1-T DRAM cell structure which consists of one storage element, capacitor and one pass-transistor, M_1. A capacitor is used to hold the stored value and therefore occasional refresh is needed (Tsuchiya and Itsumi, 1982). The 1-T DRAM requires a sense amplifier for each Bit Line (BL) due to charge redistribution read-out. When writing a 1 into a DRAM cell, a threshold voltage is lost (Cao *et al*., 2012).

On the other hand, a 3-Transistor (3-T) structure of DRAM cell is shown in Fig. 2. A signal is first sent to the write pin of transistor M_1. The write enable pin is then set to high, allowing the signal to move through transistor M1 and into the capacitor and transistor M_2 (Luk *et al*., 2006). As shown in Fig. 2, the capacitor holds the signal for a brief period. In order to store the signal for extended periods, the capacitor must be refreshed often (usually about once every 1000 ns), meaning that the signal must be re-sent to the cell and stored again. In order to read the signal stored in the capacitor, the read enable pin on transistor M_3 must be set to high. As a result, the signal is allowed to flow through transistor M_3 and out of the read pin of the DRAM cell (Diodato *et al*., 1997).

MATERIALS AND METHODS

For the design method of 4-bit memory column for DRAM cell, CEDEC 0.18 μm CMOS process has been utilized. The 4-bit memory column using the DRAM cells is shown in Fig. 3. The memory column is simply 4-DRAM cells wired in parallel with a few added transistors. To

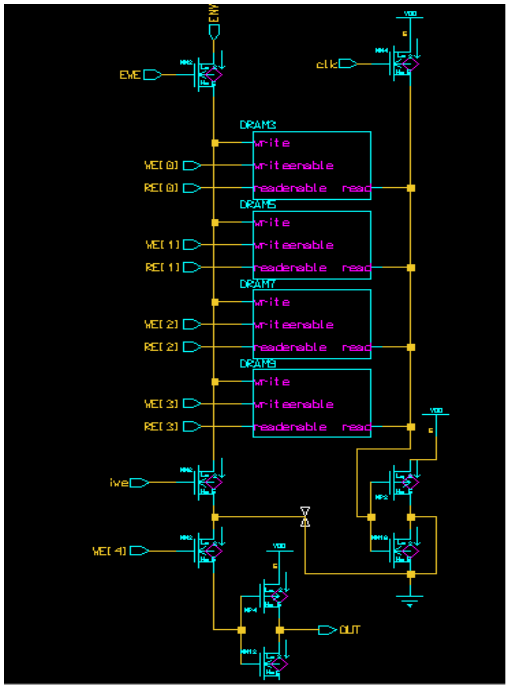

Fig. 3: Schematic diagram of the 4-bit memory column DRAM cell

design the 4-bit memory column cell for DRAM, the 3-T method is used which is solely constructed from NMOS transistors. The circuit is using entire NMOS transistors, so the substrate current is also reduced for the overall circuit design.

RESULTS AND DISCUSSION

CEDEC 0.18-μm CMOS process is used to measure the output results of the modified 4-bit memory column DRAM cell with the ELDONET simulator. About 1.8 V power supply voltage and 27°C operating condition is used for the design parameters of the 4-bit memory column DRAM cell. All the design parameters for the 4-bit memory column cell are shown in Table 1.

The simulated output results of the 4-bit memory column DRAM cell is shown in Fig. 4. Simulation results show that the modified circuit performs better by reducing the size of capacitor to 10 pF to get the best result.

In Fig. 5, the completed chip layout of the modified 4-bit memory column DRAM cell is presented. In this layout, CEDEC 0.18 μm CMOS process IC station has been used. From Fig. 5, it is clear that the small capacitor takes only a small space of the circuit layout and eventually reduce the cost of the whole chip.

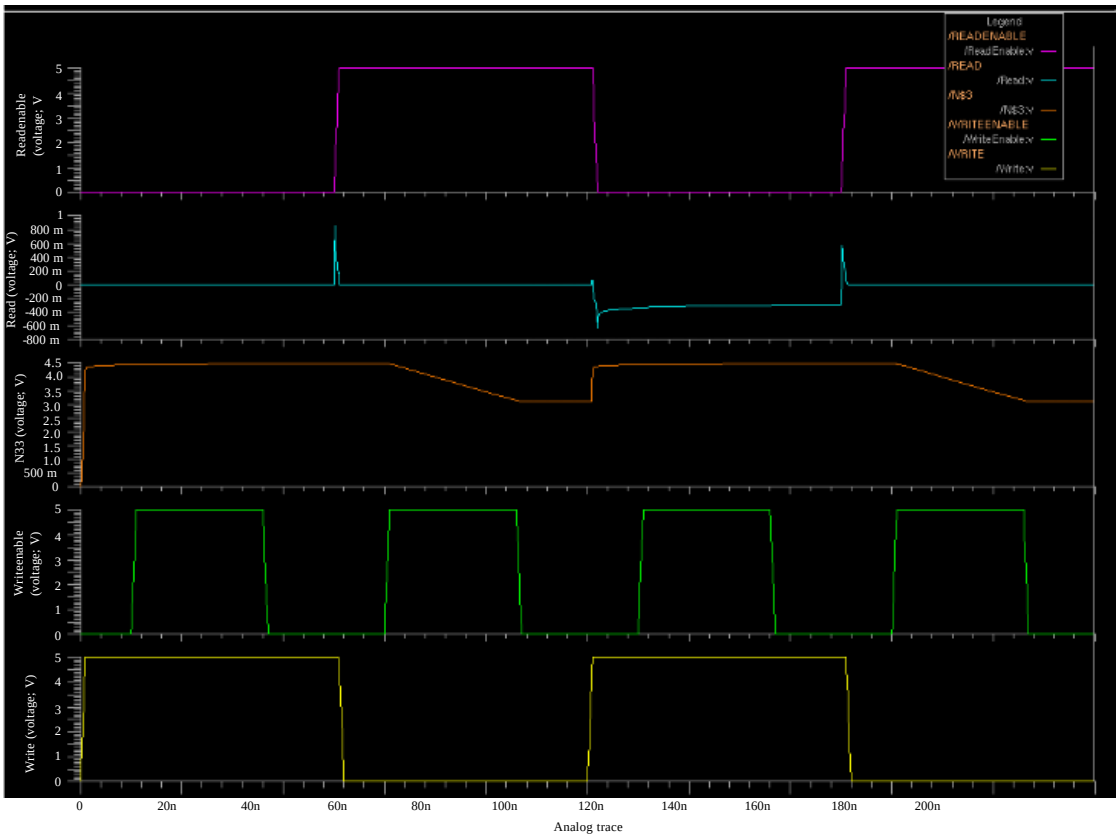

Fig. 4: Simulation result of DRAM cell

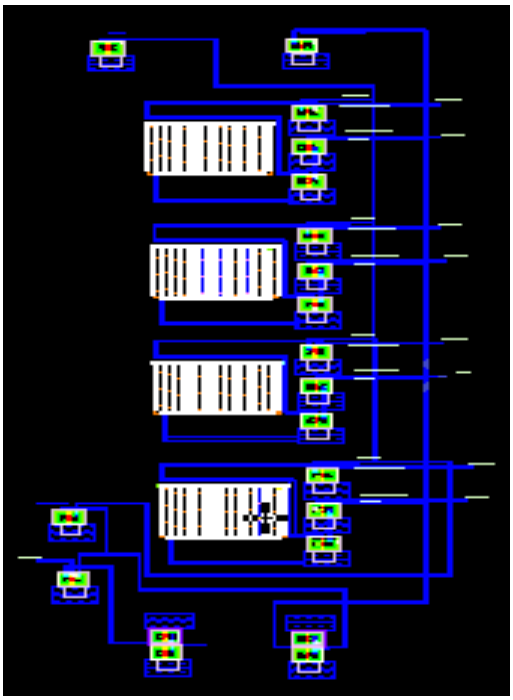

Fig. 5: Layout diagram of the 4-bit memory column DRAM cell

Table 1: Main design parameters

Parameters	Values
Power supply	1.8 V
Temperature	27°C
NMOS length	0.18 μm
NMOS width	3 μm
Capacitor	10 pF

CONCLUSION

In this study, the 4-bit memory column DRAM cell is designed using the CEDEC 0.18 μm CMOS process. Between the two methods, 3-T method is used for designing the DRAM memory column cell. The simulation verifies that the circuit is able to perform properly. According to the research result, it is obvious that the circuit is capable of working in 0.18 μm CMOS process with small capacitor value. Moreover, the modified circuit requires lower power consumption. In addition, the small capacitor size also reduces the overall chip size which ultimately reduces the cost of the circuit. The 3-T DRAM cell which is presented in 4-bit memory column cell, only used the NMOS transistors instead of PMOS transistors. Therefore, high speed also achieved from the design of the 4-bit memory column DRAM cell.

REFERENCES

Agrawal, G.R., L.W. Massengill and K. Gulati, 1994. A proposed SEU tolerant dynamic random access memory (DRAM) cell. IEEE Trans. Nucl. Sci., 41: 2035-2042.

Akter, M., M.B.I. Reaz, F. Mohd-Yasin and F. Choong, 2008a. A modified-set partitioning in hierarchical trees algorithm for real-time image compression. J. Commun. Technol. Electr., 53: 642-650.

Akter, M., M.B.I. Reaz, F. Mohd-Yasin and F. Choong, 2008b. Hardware implementations of an image compressor for mobile communications. J. Commun. Technol. Electr., 53: 899-910.

Cao, C.W., S.G. Zang, X. Lin, Q.Q. Sun, C. Xing, P.F. Wang and D.W. Zhang, 2012. A novel 1T-1D DRAM cell for embedded application. IEEE Trans. Electron Devices, 59: 1304-1310.

Chang, I.J., J.J. Kim, S.P. Park and K. Roy, 2009. A 32 kb 10T sub-threshold SRAM array with bit-interleaving and differential read scheme in 90 nm CMOS. IEEE J. Solid-State Circuits, 44: 650-658.

Chun, K.C., P. Jain, T.H. Kim and C.H. Kim, 2012. A 667 MHz logic-compatible embedded DRAM featuring an asymmetric 2T gain cell for high speed on-die caches. IEEE J. Solid-State Circuits, 99: 1-13.

Diodato, P.W., J.T. Clemens, W.W. Troutman and W.S. Lindenberger, 1997. A reusable embedded DRAM macrocell. Proceedings of the IEEE Custom Integrated Circuits Conference, May 5-8, 1997, Murray Hill, New Jersey, pp: 337-340.

Leiss, J.E., P.K. Chatterjee and T.C. Holloway, 1982. dRAM design using the taper-isolated dynamic RAM cell. IEEE Trans. Electron Devices, 29: 707-714.

Luk, W.K., J. Cai, R.H. Dennard, M.J. Immediato and S.V. Kosonocky, 2006. A 3-transistor DRAM cell with gated diode for enhanced speed and retention time. Proceedings of the Symposium on VLSI Circuits, June 15-17, 2006, New York, USA., pp: 184-185.

Marufuzzaman, M., M.B.I. Reaz, M.S. Rahman and M.A.M. Ali, 2010. Hardware prototyping of an intelligent current dq PI controller for FOC PMSM drive. Proceedings of 6th International Conference on Electrical and Computer Engineering, December 18-20, 2010, Dhaka, Bangladesh, pp: 86-88.

Mogaki, S., M. Kamada, T. Yonekura, S. Okamoto, Y. Ohtaki and M.B.I. Reaz, 2007. Time-stamp service makes real-time gaming cheat-free. Proceedings of the 6th Annual Workshop on Network and Systems Support for Games: Netgames 2007, September 19-20, Melbourne, Australia, pp: 135-138.

Mohd-Yasin, F., A.L. Tan and M.I. Reaz, 2004. The FPGA prototyping of iris recognition for biometric identification employing neural network. Proceedings of the 16th International Conference on Microelectronics, December 6-8, 2004, Tunis, Tunesia, pp: 458-461.

Reaz, M.B.I., M.T. Islam, M.S. Sulaiman, M.A.M. Ali, H. Sarwar and S. Rafique, 2003. FPGA realization of multipurpose FIR filter. Proceedings of the Parallel and Distributed Computing, Applications and Technologies, August 27-29, 2003, Chengdu, pp: 912-915.

Reaz, M.B.I. and L.S. Wei, 2004. Adaptive linear neural network filter for fetal ECG extraction. Proceedings of the International Conference on Intelligent Sensing and Information Processing, January 4-7, 2004, Chennai, India, pp: 321-324.

Reaz, M.B.I., F. Mohd-Yasin, S.L. Tan, H.Y. Tan and M.I. Ibrahimy, 2005. Partial encryption of compressed images employing FPGA. Proceedings of the IEEE International Symposium on Circuits and Systems, May 23-26, 2005, Kobe, Japan, pp: 2385-2388.

Reaz, M.B.I., F. Choong and F. Mohd-Yasin, 2006. VHDL modeling for classification of power quality disturbance employing wavelet transform, artificial neural network and fuzzy logic. Simulation, 82: 867-888.

Reaz, M.B.I., F. Choong, M.S. Sulaiman and F. Mohd-Yasin, 2007a. Prototyping of wavelet transform, artificial neural network and fuzzy logic for power quality disturbance classifier. Electr. Power Components Syst., 35: 1-17.

Reaz, M.B.I., M.I. Ibrahimy, F. Mohd-Yasin, C.S. Wei and M. Kamada, 2007b. Single core hardware module to implement encryption in TECB mode. Informacije MIDEM J. Microelect. Electron Compon. Mater., 37: 165-171.

Tsuchiya, T. and M. Itsumi, 1982. New dynamic RAM Cell for VLSI memories. IEEE Electron Device Lett., 3: 7-10.

Verma, N. and A.P. Chandrakasan, 2008. A 256 kb 65 nm 8T subthreshold SRAM employing sense-amplifier redundancy. IEEE J. Solid-State Circuits, 43: 141-149.

Xie, Y., 2011. Modeling, architecture and applications for emerging memory technologies. IEEE Design Test Comput., 28: 44-51.