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Design and Implementation of Direct Sequence Spread Spectrum System Using Combinatorial Linear Search Method with Residence of Variable and Parallel by FPGA

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Abstract: Due to the rapid growth of telecommunications systems and the increasing demand for radio-frequency spectrum, spread spectrum technique that makes optimal use of the frequency spectrum is important. Proper performance of these systems against unintentional and intentional interferences, low probability of eavesdropping and many other benefits have been caused the ubiquitous of these systems in martial and commercial areas. This increasing expansion on the one hand and the possibility to implement reconfigurable hardware with small dimensions and high-speed on the other hand causes simulation and implementation of the sender and messages acquisition section in receiver of Direct Sequence Spread Spectrum (DSSS) using FPGA chip, be considered in this article. The results of this implementation, the processing profit 27.408dB, PN clock frequency is equal to 35.24 meg, power consumption is 90.231 mw and code length is 264-1 which is comparable with all designed digital direct sequence spread spectrum system systems. Combinatorial linear search method with integration variable and parallel search is used to implement the acquisition section.

Key word: Direct Sequence Spread Spectrum system (DSSS), synchronization, acquisition, FPGA, search

INTRODUCTION

"Optimal use management of the frequency spectrum is very difficult due to presence of several technologies and different services. This was done in the past by assigning frequency spectrum to each service but recently a method has been presented for solving this problem that relies on features of a type of modulation. This modulation shares frequency band without significant interference. This method is called spread spectrum modulation". In fact, this is spread spectrum of sending method in which the sending signal bandwidth is greater than the minimum bandwidth required. Bandwidth is expanded by a series of pseudo-random code independent of the information from a receiver in accordance with the code in order to remove spectrum extension and restore information.

Design and implementation by FPGA: A spread spectrum system achievement depends on the receiver power in synchronization of sequence produced by received PN sequence. Recipient is informed of pseudo-random code of extender in receiver but its phase at the time of receiving should be obtained from signal. This is for the reason that sending message through a communication channel causes some delay which consists of two parts: fixed and variable. The fixed part depends on the distance between sender and receiver. The variable part depends on atmospheric conditions. Therefore, PN synchronization in general is divided into two parts. The first part is called acquisition This part is obliged to adapt received PN phase and produced PN signal phase in a certain interval, for example one or two chips.

This interval is dependent on the tracking circuitries' power. In this study, assuming that the channel delay is an integral multiple of a chip. Synchronization task is taken by acquisition section, and taken from the tracking. There are various methods for acquisition such as linear search, parallel search, state diagrams and matched filter. Methods such as matched filter and simple linear search are not suitable for codes with very high length. Parallel search method also requires an implementation of high-volume hardware. State diagrams method requires also very high complex computations for long codes. Therefore, combinatorial linear search method with variable integration and parallel method are used in this article for spread spectrum system with frequency period of PN code about 1019.

MATERIALS AND METHODS

In this method, at first partial correlation is performed on delays guessed at the time of T1, means by taking into account a certain number of chips. Then delays that have relative correlation maximum value among all guessed delays are considered for the second phase. In the second phase, the first phase is repeated in the time. A number of other suitable delays are chosen again for the third phase, and the operation is repeated in the time.

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The advantage of this method compared to linear search with fixed residence is its higher speed. Better speed can be obtained by combining this method with parallel method. Of course, in parallel method all the guessed delays are examined simultaneously and proper delay is determined ultimately. But given that doing such an act requires high volume of hardware, therefore, all three aforementioned delays are examined simultaneously using three units of calculation of correlation, compared with each other and finally are stored in memory. They are compared with a comparison result of three next delays.

The final result that is the same finding correct delay is achieved by repeating this action. Given that the number of examined delays at every phase is lower than delays which should be examined using parallel search method alone; therefore it will be hardware volume much lower than the parallel search method. In this study, search for the appropriate state is done in four phases.

Chips has been intended for the first phase, 4 chips for the second phase, 6 chips for the third phase and 63 chips for the final phase. Time interval in the final phase has been selected according to the point that in a sequence with a maximum length of frequency period of N = 2m-1, every m-1 chip and only appears once in the sequence.

Sender: Designed system sender includes PN clock producer, spectrum extender section, registers to model channel delay, PN code generator and modulation section. Of course, the modeled channel should be put after modulation section. But because in the modulation section, 4 or 8 five-bit sinusoidal coefficients are sent per information chip, therefore, a channel should be used after PN code generator instead of using five parallel channels after modulation section. However, modeling channel registers are not required when implementing. Also information is reached to the receiver as frames. Start bit forms its primary bits, and information forms the next bits. Figure 1 shows a simulated structure view of the sender.

Clock producer: This clock producer input is the required clock of modulation and the highest system frequency is assigned to it. This block output is the also required clock for PN code generator. It is also used to produce reset signal of counters is used for calculating partial correlation in different time intervals (4 different intervals), as well as to produce clock that select various guessed delays. In fact, a clock producer is a clock divider.

PN code producer: Pseudo-random codes with a maximum length are made using linear feedback registers shift and

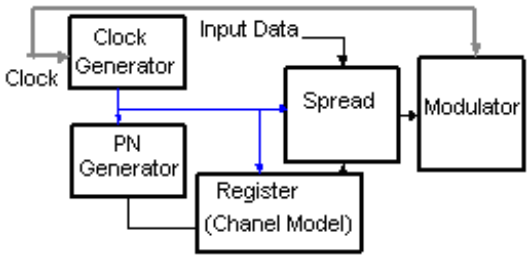

Fig. 1: Sender structure

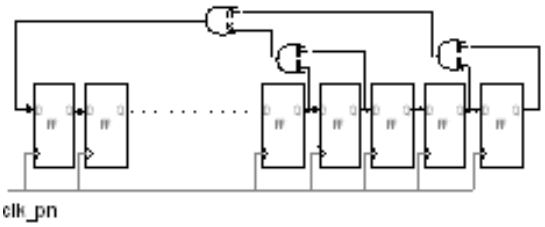

Fig. 2: Linear feedback register shift

specific polynomials. For example, 4 feedbacks and 64 registries are needed to make a 64-bit register shift that has been used in this research (Fig. 2). Considering the fact that each FPGA cell has been composed of two CLB and two flip-flops, at least clb 32 (only to make flip-flops shown in Fig. 2) is needed to implement such a structure. If readable and writable memories are used instead of storing code in flip-flop, less CLB is required and hardware occupies less volume.

Peter (1995) has provided 63 and 32-bit pseudo-random code generator using RAM. The binary counters are used in these generators in order to address memories. 4 or 5-bit pseudo-random counters are preferably used to create a higher telecommunications security. In this paper, 64-bit code generator is designed and implemented using RAM (Fig. 3). Pseudo-random code generator with maximum length using RAM has higher speed and less volume. Frequency of this generator is 3.180 MHz RAM. However, the structure of Fig. 2 has a maximum frequency of 109.8 MHz

Modulator: Modulator duty in a telecommunications system is to receive a bit chain as input and to convert it to an electric wave form suitable for transmission by telecommunication channels. "Modulations is used in order to facilitate dissemination, sharing, overcoming the limitations of the equipment, as well as allocation of frequency and reduction of noise and interference" (Sam, 2001). Given that the designed structure is used for PCM audio systems with data rate of 64kbit, BPSK method that has a rate lower than QPSK as well as easier implementation can be also used for modulation.

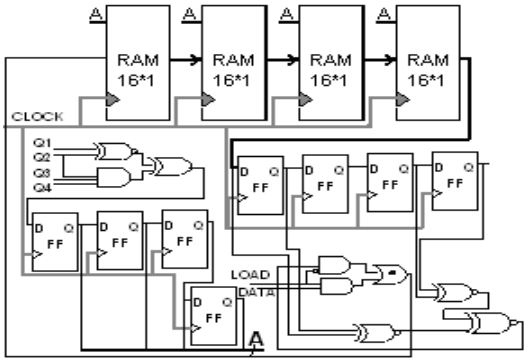

Fig. 3: 64-bit code generator using RAM

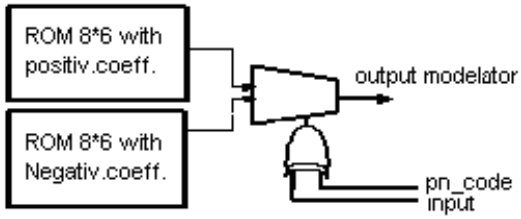

Fig. 4: modulator design structure

Considering that in BPSK modulation, the carrier phase is changed by the digital information changes, the positive or negative sinusoidal coefficients stored in both memories (ROM) are send out according to the amount of extended signal. This means numbers of sinusoidal coefficients (8 or 4) per chip of extended information are sent to the receiver. Ferreiro *et al.* (2003) has used six samples for this purpose (Fig. 4). In this study, four and eight samples have been put at each sinusoidal frequency period. Both simulation states have been synthesized and implemented.

Receiver: The designed system receiver consists of a detector, clock divider, and correlation calculating unit, control unit, register, multiplexer and memory unit. The signal received by the receiver is examined after detection by the demodulator to find the correct delay. Information is entered into system. Start bits consists the first part of this frame, and then information is sent. In T1 technology the allotted time to start bits or in the other word the allowed time for synchronization is equal to 301us. The designed system, according to the used combinatorial method, is unable to find a proper delay less than one-third of the allowed time.

Modulator: "Modulation is an invertible process and extract message from information carrier wave form (produced by modulation) by demodulator "(Sam, 2001).

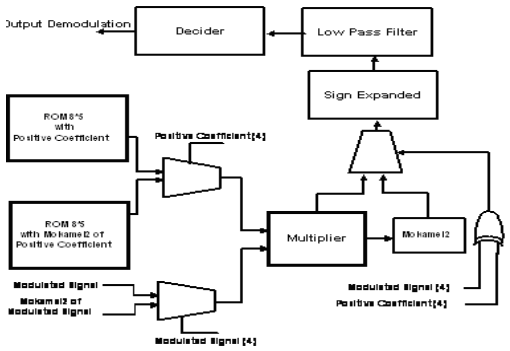

Figure 5: Modulator structure

In general, in a BPSK demodulator, the signal received in the receiver in a sinusoidal carrier multiplication of a low-pass filter passed and then is decided. After BPSK demodulation, another type of detection is also done that is removal of the received signal extension.

Demodulator purpose is to detect information chips among these sinusoidal samples received by the receiver. To do this, modulation output is multiplied in these sinusoidal coefficients or in better word in the sinusoidal samples stored in a read-only memory. Then it is passed through low-pass filter that calculates the mean input data. And thus we retrieve the expanded chips. The structure of this design has been shown in Fig. 5.

According to the fourth bit of the multiplier inputs that is sign bit, these inputs or supplement of their two are placed at the disposal of the multiplier. The applied change is modified after multiplication. This is done by making the fourth bits xor and assigning xor gate's output to select signal of a multiplexer. So if both inputs are negative means their fourth bits is one or both inputs are positive means their forth bits are zero, xor gate's output becomes zero, and multiplier output is valid. Otherwise the product's supplement of two is considered as a valid output. By considering the channel delay as an integral multiple of a chip, demodulation can be done before removing expansion. Otherwise, means if there are less delays of a chip for sending signal, removal of the expansion must be done at first.

Register: As shift register was used in the sender section to model the actual delay of channel, shift register is also used in the receiver section in order to create delays guessed for tracking phase. Considering that this system has been designed for distance up to 10 and 10km delay is also equal to 212 chips due to PN rate, so possible delays are considered between zero and 220 chips. The number of shift register cells is equal to 220. The output of each of these cells enters the input of a multiplexer.

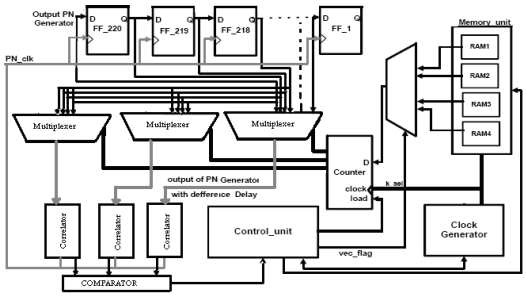

Fig. 6: Structure of shift register used in the receiver

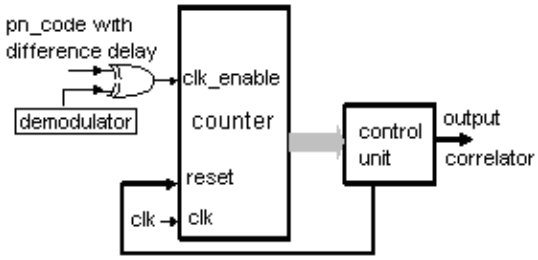

Figure 7: correlation calculating unit

Signal select of this output is a counter that its input clock is one when a partial correlation of a particular state is calculated (Fig. 6).

RESULTS AND DISCUSSION

Correlation calculating unit: Correlation function, which can be defined as the sum of the products of the two signals shows the similarity of two signals. Linear search method is used in spread spectrum systems. A code periodicity with delay has been considered PN code with a short length, it is multiplied in received signal by receiver; and synchronous with PN clock, summation is took place. If the sum, namely, correlation unit output is greater than a certain threshold limit, the considered delay is accurate.

Otherwise, the correlation is calculated for another delay and the operation is repeated to specify the correct delay. Considering a full code frequency period is not possible in codes with long length due to time constraints of synchronization, and correlation is done in a limited time interval. This type of correlation is called partial correlation. In this study, partial correlation method must be used because frequency period of extender PN code is about 1019. The main task of calculating correlation unit is multiplication and summation.

Multiplication is done using xor gate and summation as shown in Fig. 7 is done by the counter that gate's output xor enables or disables actuator signal of its clock. This counter reset signal is activated at the time of half of a chip after a period of time interval specified by the control unit and is prepared for calculation of the partial correlation of the next state.

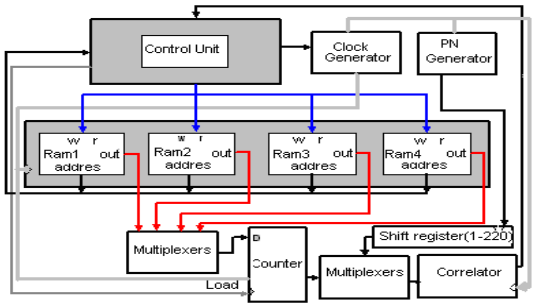

Fig. 8: Memory unit

Memory unit: The combinatorial linear search with variable integration and parallel method are used in this paper. The possible delays intervals are also considered between 0 to 220 chips. Therefore, at first partial correlation must be calculated in time interval of T1, for 220 different states. It must be considered each of the states that allocated the maximum amount of partial correlation to itself. But n states may have equal partial correlation among these 220 different states.

Therefore, after the end of each phase, equal states should be stored in a readable and writable memory and recall them in the next phase, and partial correlation is calculated for them. According to the linear search carried out in four phases, 4 memories are required. The memory address is called at the end of each phase. If its value is zero, the content of zero address is considered as the correct delay. If the address refers to the other number, for example n, it is realized that n states have been occurred, which are recalled at the next stage, and partial correlation is calculated for them (Fig. 8).

Comparison with other works: In recent years, a spread spectrum instruments with different specifications and various parameters have been supplied to the market. Chips of sender, receiver and sender-receiver, internal and external modems and so on can be noted among these instruments. In this article it had been tried to design the sender and message acquisition section in the receiver using combinatorial linear and parallel search method for the long code in full digital. Deng and Chien, 1999) has designed a fully digital spread spectrum system for codes that can be acquired with filter matched to acquisition section using combinatorial linear search method and matched filter method. Ferreiro *et al.* (2003) has designed this fully digital system using the matched filter method. Comparison of these systems is shown in Table 1.

Table 1: Comparison with other works

Power PN rate consumption	Value	Length and type Tracing Processing Referenc of code	Method	Profit	e
_____	8.192meg	127	Matched filter	18.06db	(Ferreiro *et al*., 2003)
91.583mw	20meg	M Sequence	combined method of linear searching and matched filter	21db	(Deng and Chien, 1999)
90.231mw	35.24 meg	To Tracing lengths with a matched filter M_sequence	combined method of linear searching with staying variable and parallel	27.4 db	this research

CONCLUSION

The of the sender section and message acquisition section in the receiver of a fully digital direct sequence spread spectrum system has been designed and implemented in this paper. The way of implementation of various parts of the sender and receiver were described, including the optimal way to implement the PN code generator with frequency period of about 1019 using reading-writing memory and the acquisition message receiver section in this system receiver. A system introduced on Spartan2 chip, 2s50fg256 series, manufactured in Xilinx Company was implemented, and the results were presented. These results include improved clock rate of pseudo-random code with maximum length and frequency period of 1019 at the extent of 35.24meg. Processing profit is equal to 27.408dB, and consuming power is 90.231mw. This system with mentioned capabilities is comparable to similar fully digital systems.

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