Journal of Engineering and Applied Sciences 12 (4): 1040-1049, 2017
ISSN: 1816-949X

Design of a Three-Phase Buck-Type PFC PWM Rectifier

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Abstract: This study presents the design of a three-phase buck-type PFC PWM rectifier simulation to step down 7.5 KVA, 400 V line-to-line AC to form a 380 V DC bus. Low power version of the buck rectifier is also implemented in hardware. The buck rectifier circuit topology is adopted by modifying the commonly known current source rectifier. A SVPWM technique called Switching Loss Optimized (SLO) modulation is employed to easily control the rectifier and carryout power factor correction. An input AC filter is designed to reduce THD and at the same time achieve a high leading power factor. An output DC filter is also designed to provide ripple-free constant DC current and voltage. Closed loop control is applied to maintain steady output voltage in the event of disturbances in the AC supply or the load. The circuit is first designed to meet the specifications and then tested using Simulink/Matlab. The finalized design from the simulation is verified by low power hardware implementation.

Key words: SLO, THD, DC current, AC supply, voltage

INTRODUCTION

The NUS-Smart grid project involves the formation of a 415 V AC bus and two DC buses of 48 and 380 V. Renewable and intermittent energy captured by solar photovoltaic panels, wind turbines and diesel generator are used to power loads such as data centers. In 2005 alone, data centers around the world consumed 120 TWh of energy but more than half the energy consumed was dissipated in power conversion, distribution and maintenance (Pratt *et al*., 2007). In conventional data centers that use the 400 V AC architecture, a UPS (uninterruptible power supply) receives the AC input, rectifies it to DC and stores it in a battery to be inverted back to AC. A PSU (Power Supply Unit) again rectifies this AC input to 380 DC which can be further stepped down by isolated DC/DC converters. As a result, the overall power conversion efficiency is <50% (Pratt *et al*., 2007). Thus, DC distribution achieves higher efficiency without the inverter in the UPS and rectifier in the PSU.

In a three-phase buck-type PFC PWM rectifier as shown in Fig. 1 (Kolar and Friedli, 2013), power switches are added to the diode bridges to arbitrarily apply the mains phase voltages to the output dc side so that AC voltage-independent control of power transfer is possible. The switches in a diode-bridge are complementary and when a top switch from one phase and bottom switch from another phase are on, the output inductor current flows from the phase of the top switch into the phase of the bottom switch. At the same time, the output DC-link voltage is formed by the line-to-line AC voltage. When all of the top or bottom switches of three bridges are off, current flows through the freewheeling diode, D causing the input phase currents and output DC voltage to be zero. The freewheeling or zero period is essential for controlling the magnitude of DC voltage and for the formation of switching pattern by Switching Loss Optimized (SLO) Space Vector Pulse Width Modulation (SVPWM) control algorithm.

The SLO algorithm distributes the output DC current between the three-phases after lowpass filtering the discontinuous input AC currents from the switches to produce sinusoidal input AC currents. In the output side, output voltage and current are also filtered by the output inductor and capacitor to produce steady DC voltage. The input LC lowpass filter removes the high frequency switching harmonics in the discontinuous input AC currents while at the same time causing the filtered input phase current to lead the input phase voltage due to the filter capacitor. This phase shift degenerates the power factor but it is kept at a reasonably low value by keeping the capacitance value small and raising the inductance value to meet the correct cutoff frequency. Buck-type PFC rectifier systems are expected to provide an option in future for the supply of dc distribution grids or possibly also for the charging of electric vehicle batteries (Friedli *et al*., 2014; Trentin *et al*., 2012).

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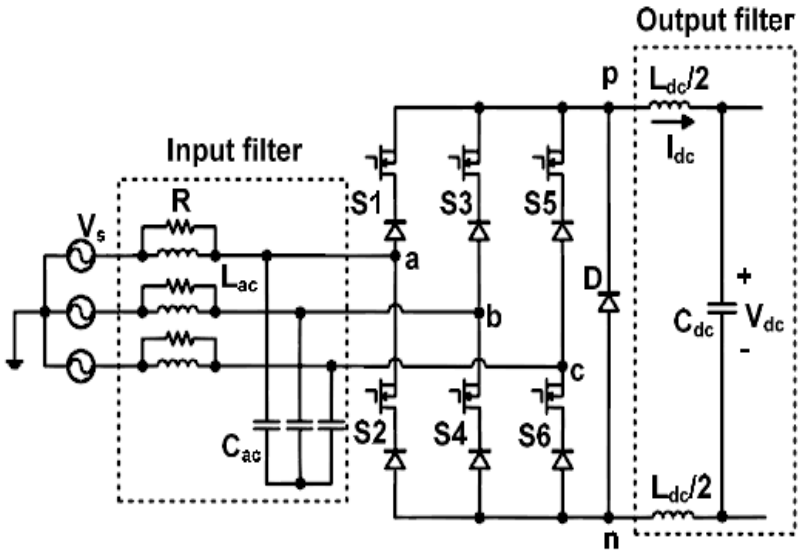

Fig. 1: Circuit topology of the three-phase buck-type PWM rectifier

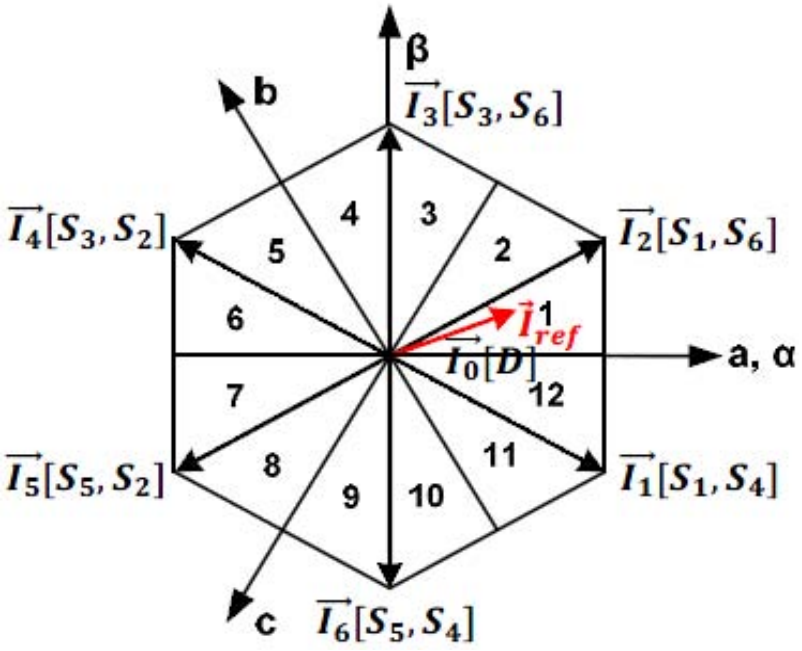

Fig. 2: Six fixed current space vectors on the α-β coordinate plane

MATERIALS AND METHODS

Control and modulation: The SLO algorithm used to control the buck rectifier is implemented through SVPWM. The space vector is implemented by six fixed current space vectors in the alpha-beta coordinate plane as shown in Fig. 2. These states are chosen so that the DC output can be varied between 0 V to maximum voltage.

The rotating current space vector, I_{ref} is formed from the two nearest fixed states and a zero vector/freewheeling state, I_0. The free wheeling state is formed when current only flows through the freewheeling diode with the entire top or bottom switches off. Table 1 shows the switches involved in each of the six fixed current space vector states and the applied output DC voltage.

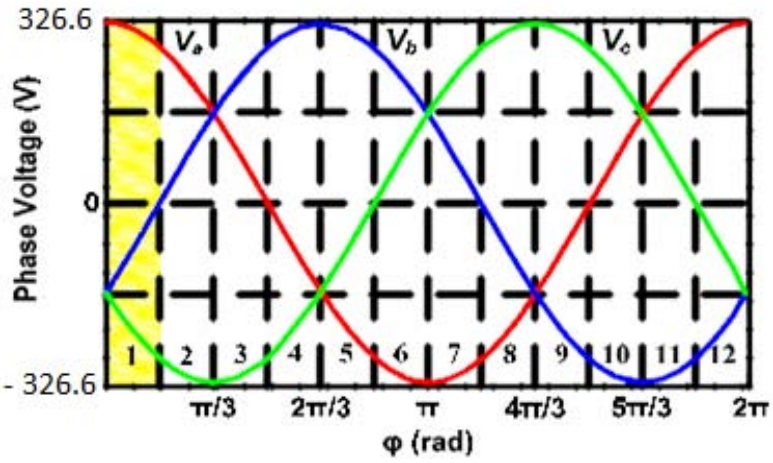

Fig. 3: Six fixed current space vectors on the α-β coordinate plane

Table 1: Switches involved in the fixed current space vector states and resulting output voltage

State	Top switch	Bottom switch	Output voltage
I_1	S_1	S_4	V_{ab}
I_2	S_1	S_6	V_{ac}
I_3	S_3	S_6	V_{bc}
I_4	S_3	S_2	V_{ba}
I_5	S_5	S_2	V_{ca}
I_6	S_5	S_4	V_{cb}

Table 2: Look-up table to calculate the final duty ratios of the three-phase bridge

Sector	$\delta_{eff,a}$	$\delta_{eff,b}$	$\delta_{eff,c}$
1,7	δ_a	$1-\delta_c$+td	δ_c
2,8	δ_a	$1-\delta_a$+td	δ_c
3,9	$1-\delta_b$+td	δ_b	δ_c
4,10	$1-\delta_c$+td	δ_b	δ_c
5,11	δ_a	δ_b	$1-\delta_a$+td
6,12	δ_a	δ_b	$1-\delta_b$+td

The input phase voltage is divided into 12 sectors as numbered in Fig. 2. Two sectors are formed between two fixed current space vector states. For e.g., sectors 1 and 12 are formed between states I_1 and I_2 as seen from the α-β coordinate plane in Fig. 3. The space vectors are formed using the SLO modulation scheme which produces the least switching losses. When the rotating current space vector, I_{ref} is in any sector, the duty ratios of the switches in the two fixed states can be calculated from Eq. 1 and look-up Table 2 (Czapor *et al*., 2009):

$$\delta_i = \frac{V_{o,ref}}{\sum_{j=a,b,c} VCF,j^2} \times |VCF,i| \quad (1)$$

Where:

Vo, ref = The constant output DC voltage reference

VCF, j and VCF, i = The instantaneous AC capacitor voltages

i = Phase a, b or c

Where td is the overlapping time, to ensure continuous current conduction between the 3 bridges. δ_a, δ_b and δ_c are the preliminary duty ratios calculated from Eq. 1. $\delta_{eff,a}$, $\delta_{eff,b}$ and $\delta_{eff,c}$ are the final duty ratios applied to the switches of the three-phase bridge. In each sector, there are 4 current commutations and the space vectors are arranged so that the average switching voltage to the freewheeling state is the line-to-line voltage with smaller absolute value. This is to reduce conduction losses in the freewheeling diode. As the switching frequency is very high, the states can be in any order and the resulting output average will still be the same. Figure 4 shows the switching pattern of the six switches (S_1-S_6) in Sector 1.

For example, in Sector 1, current commutates from switch 6-S_4 with S_1 on. Secondly, current commutates from S_1 to D with S_4 on. Thirdly, current commutates from D to S_1 with S_4 on. Finally, current commutates from S_4 back to S_6 with S_1 on.

Design of the three-phase buck-type PFC PWM rectifier input lowpass LC filter design: The desired frequency of filtered input sinusoidal AC currents is 50 Hz. The need for small capacitor, Cf and inductor, Ls values and the occurance of resonance in the region of residual harmonics make it necessary to use a higher cutoff frequency, fc in the KHz region. The formula to calculate the cutoff frequency, fc is given in Eq. 2:

$$fc = \frac{1}{2\pi\sqrt{LsCf}} \quad (2)$$

To begin designing the filter, an initial capacitor value is selected to be 4 mF. The filter capacitance is kept

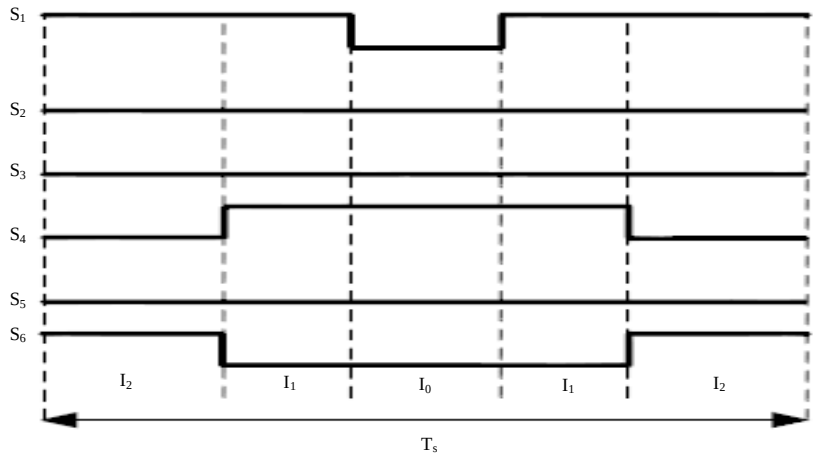

Fig. 4: Sequence of fixed current space vectors in Sector 1

as low as possible to reduce leading power factor between the filtered current and capacitor voltage. As there is lesser constraint in choosing the cutoff frequency compared to choice of filter inductor, the next step is to determine the inductance value to give the least THD in the filtered AC current.

Output lowpass filter design: In order to achieve a pure DC waveform without any frequency components, the cutoff frequency should ideally be very low. In the DC waveform produced by the switches, there are two main frequency components around 300 Hz and 19.8 KHz. Removal of components in such small frequencies requires large inductor and capacitor filter. The capacitor value should be a high value like 2200 mF to provide a constant DC without any distortions. Having obtained the capacitor value and choosing a cutoff frequency of 30 Hz the inductor value required can be calculated by reshuffling (Eq. 2).

Igbt and fast recovery diode selection and power loss: The voltage rating of the required IGBT is 1.2 KV. This voltage is higher than the 10% peak input line voltage of 622 V. The reverse voltage rating required in the fast recovery diodes is also 1.2 KV. In DCM, the voltage applied across the freewheeling diode can be the peak input line voltage, Vline (pk) or output DC voltage, Vo of 380 V (Czapor *et al*., 2009). Equation 3 gives the maximum blocking voltage, Vmax required for the diode as 755.69 V:

$$V_{max} = V_{line}(pk) + V_o \times 0.5 \quad (3)$$

The conduction losses in the IGBTs and diodes are given by Eq. 4-6 (Trentin *et al*., 2012):

$$P_{cond}(IGBT) = 6 \times V_{ce} \times IC \quad (4)$$

$$P_{cond}(diode) = 7 \times if \times V_f \quad (5)$$

$$P_{cond} = P_{cond}(IGGT) + P_{cond}(diode) \quad (6)$$

Where:
V_{ce} = Collector emitter voltage
IC = Collector current of IGBT

If is the forward current and V_f is the forward voltage drop of the diode. The switching losses in the IGBTs is given by Eq. 7:

$$P_{sw} = 6 \times F_{sw} \times (E_{on} + E_{off}) \quad (7)$$

Where:
P_{sw} = The switching power loss
F_{sw} = The switching frequency
E_{on} and E_{off} = The energy dissipated in the IGBT during on and off times (Trentin *et al*., 2012)

Therefore, the significant power losses in the buck rectifier are the sum Eq. 6 and 7. It is estimated to be 827.128 W.

Switching frequency selection: A high switching frequency around 20 KHz is preferred. These frequencies reduce the size of output inductors and at the same time they are low enough to cause the least EMI issues. From Simulink simulations it is known that the PWM buck-type rectifier exhibits better input current and voltage characteristics like less distortion and more sinusoidal at higher switching frequencies (Kanchan *et al*., 2005). Therefore, a high switching frequency of 19.8 KHz is selected for the simulation because 19.8 KHz is an exact multiple of the line frequency of 50 Hz and to maintain a whole number of switching periods within a sector which has a period of 1.67 mS (0.02/12).

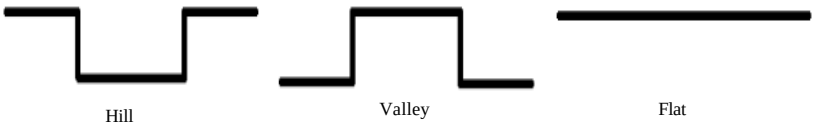

Fig. 5: Standard switching pattern in the 12 sectors

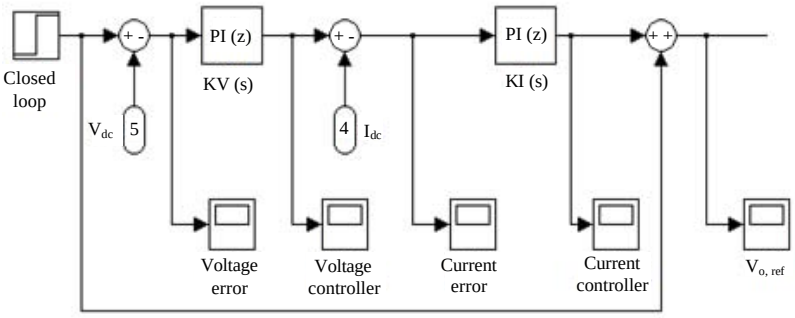

Fig. 6: Cascade control structure of the buck rectifier

SLO control algorithm implementation: The SLO control algorithm is written in matlab code, implemented as a simulink model and realized through dSPACE. Initially, the duty cycle of the three phase bridge is calculated from the instantaneous values of capacitor voltages using Eq. 1 and look-up (Table 2). These duty ratios are checked for overmodulation or undermodulation due to any noise in the measurements. The final duty ratios are converted into SVPWM signals following the SLO algorithm. The SLO algorithm also produces symmetrical switching pattern which generates fewer harmonics in unfiltered and discontinuous input AC currents. Basically, the algorithm implements the SVPWM signals for the 12 sectors. In all 12 sectors, there are only 3 types of switching patterns as shown in Fig. 5.

To implement the hill and valley pattern, their switching pattern is divided into 3 sections. The first section is built when logic 0 and 1 are applied for the first half of on time for hill pattern and first half of off time for valley pattern. The second section of the pattern is generated by applying logic 1 and 0 from start time of switching period plus half of on time for hill pattern and half of off time for valley pattern untill the end time of switching period minus half of off time for hill pattern and on time for valley pattern. The final section is generated by applying logic 0 and 1 from end time of switching period minus half of off time for hill pattern and half of on time for valley pattern untill the end time of switching period.

Close-loop control: Closed-loop control maintains the DC output voltage at the desired reference voltage for various load and supply disturbances. In the buck rectifier, cascade control is implemented by an inner current loop and an outer voltage loop as shown in Fig. 6. The PI voltage controller, KV(s) tries to maintain the DC output voltage of the rectifier close to the reference/set point, closed loop.

The PI current controller, KI(s) controls the DC current in order to supply current as KV(s) would want to maintain the reference point. When there are any fluctuations in current, KI(s) will re-manipulate the current supplied before the output voltage is affected. This is possible because current dynamics are faster than voltage changes. The current disturbances are quickly "rejected" before they affect the DC output voltage. The output from the current controller is summed with the voltage reference/set point, Closed Loop as feedforward to produce a controlled V_{o}, ref in Eq. 1.

Table 3: Design parameters

Electrical component	Value in simulation	Value in hardware setup
AC voltage source	326.6 peak	32.66 peak
AC frequency	50 Hz	50 Hz
Input AC inductor	600 uH	600 uH
Input AC capacitor	4 uF	4 uF
Diode resistance	12 U	12 U
Diode forward voltage	2.69 V	2.69 V
Output DC inductor	10 mH	10 mH
Output DC capacitor	2200 uF	2200 uF
Load resistance	150/450 U	80Ω
OL step input	380	38
CL step input	380	-
Voltage controller proportional gain	3.3	-
Voltage controller integral gain	0.155	-
Current controller proportional gain	2	-
Current controller integral gain	7	-
Switching frequency	19.8 KHz	10 KHz
Overlapping time	1 us	1 us
td	0.02	0.02

Design parameters: Table 3 summarizes the design parameters used in simulation and low power hardware implementation.

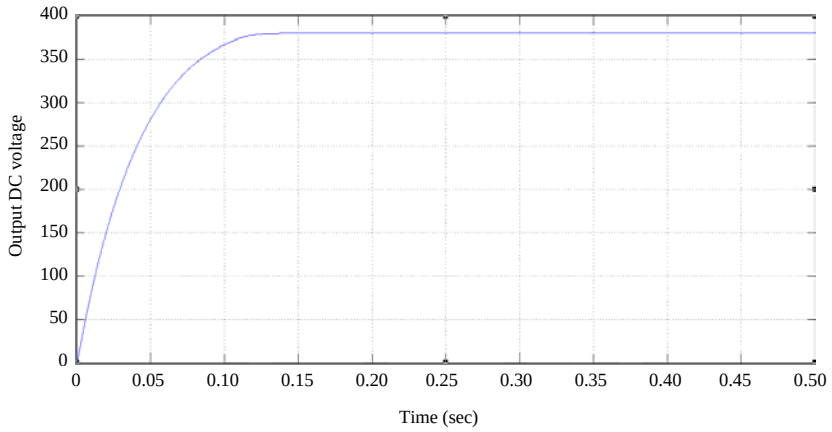

Fig. 7: Output DC voltage

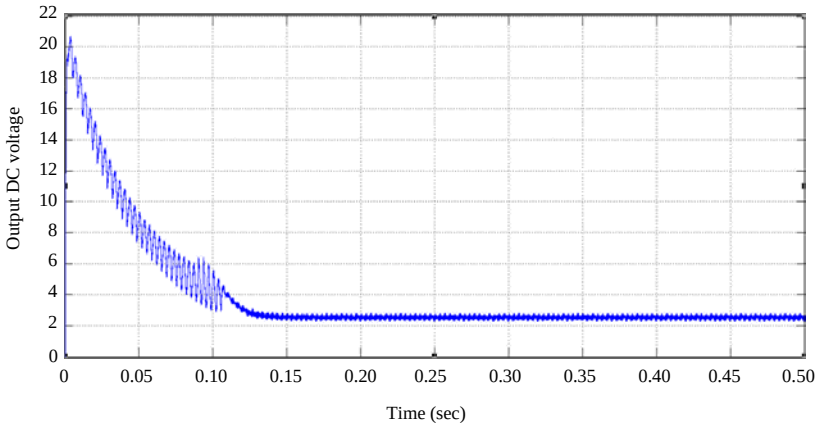

Fig. 8: Output DC current

RESULTS AND DISCUSSION

The simulation carried out in matlab involves rectifying 400 V line-to-line AC to 380 V DC for a resistive load of 150 Ω under closed-loop control. In section E, response due to a series load disturbance of 300 Ω is simulated at 0.35 sec of the 0.9 sec long simulation.

DC output-150 Ω: Figure 7 shows the steady state output DC voltage of 380 V which is reached at around 0.13 sec without any overshoot. The corresponding output DC current waveform is shown in Fig. 8. The current waveform also reaches steady state at approximately 0.13 sec. The steady state value is 2.55 A and the peak overshoot is 21 A.

AC input-150 Ω: The input lowpass filtered three phase AC sinusoidal currents (shown as phase a in yellow, phase b in magenta and phase c in cyan) are shown in Fig. 9. At steady state, all three phases are almost perfectly sinusoidal without any ripples and 120° apart.

Power factor measurementt-150 Ω: The power factor of the buck rectifier is calculated to be 0.987 leading from Fig. 10.

Duty ratios-150Ω: These duty ratios generated by Eq. 1 are shown in Fig. 11 as time-varying duty ratios (shown as phase a in yellow, phase b in magenta and phase c in cyan) over one AC cycle.

Frequency spectrum and THD of filtered AC currents: The sinusoidal AC currents have a THD within 5% as shown in Fig. 12. Three significant frequency components are the fundamental frequency (50 Hz), cutoff frequency (~3 kHz) and the switching frequency (19.8 kHz).

Load disturbance of 300 Ω: The result of the load disturbance is seen in the output DC voltage as shown in Fig. 13. The increased resistance causes the voltage across the 450 Ω load to increase to 387 V but it quickly returns to 380 V by the end of 0.9 sec. Figure 14 shows the

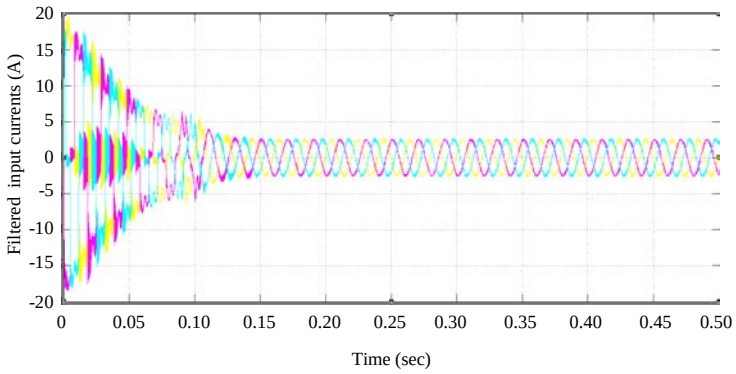

Fig. 9: Filtered three-phase AC currents

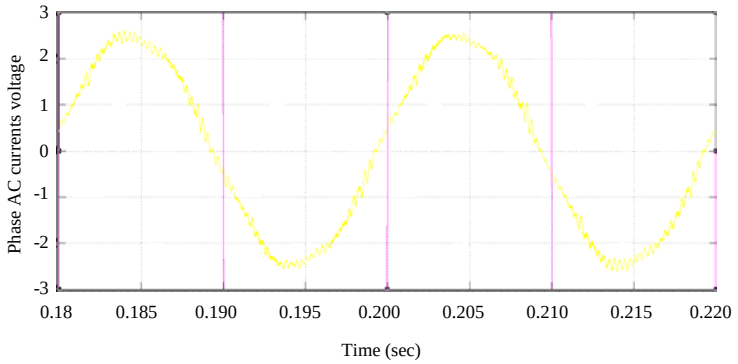

Fig. 10: Power factor measurement

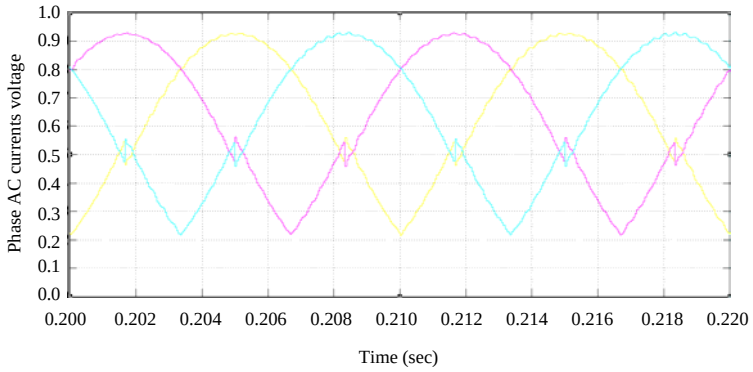

Fig. 11: Duty ratios over one AC cycle

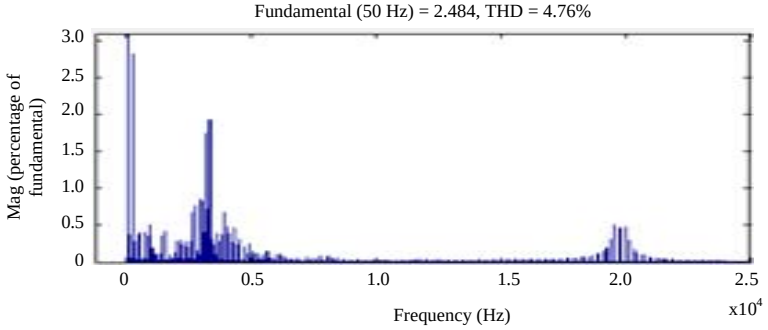

Fig. 12: Frequency spectrum of filtered phase a current

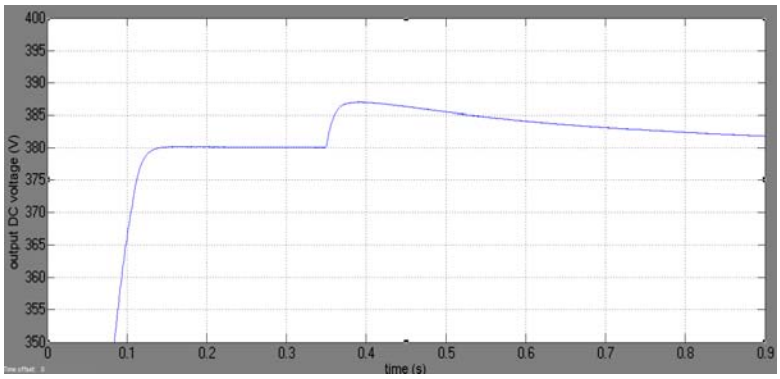

Fig. 13: Effect of load disturbance on the output DC voltage

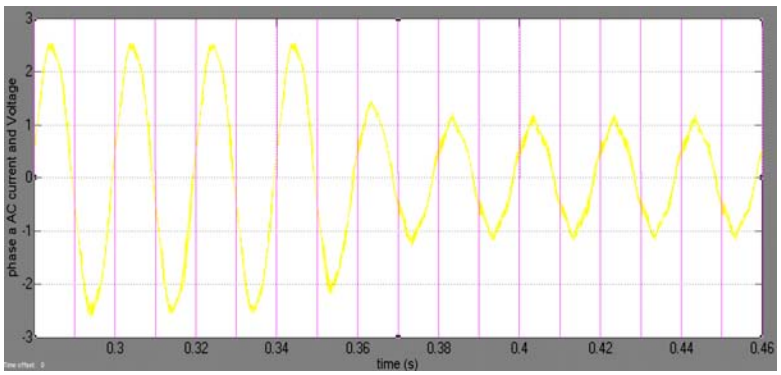

Fig. 14: Effect of load disturbance on power factor

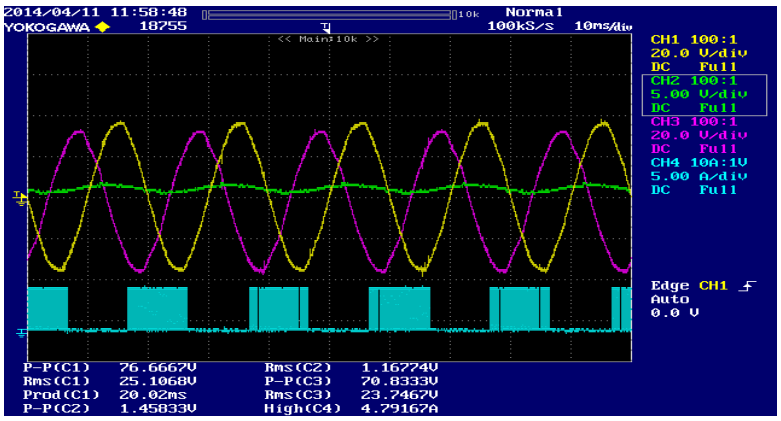

Fig. 15: AC voltages (Phase a-yellow, c-magenta), AC current (phase a-green) and SVPWM signal (blue)

effect of load disturbance on power factor. The new power factor for the 450 Ω load resistance is 0.970 leading which is <0.987 leading for the 150 Ω load resistance.

Results from hardware implementation: Hardware low power tests under open loop control are carried out by removing cascade control and giving a constant output voltage reference to $V_{0,\ ref}$. The instantaneous AC capacitor voltages are sensed by dSPACE and the resulting six SVPWM signals are generated by the Digital I/O channels.

Buck rectifier u nder open loop control: Low power of 20 VA, 40 V line-to-line AC voltage is used to test the buck rectifier for a resistive load of 80 Ω. Figure 15 shows four waveforms, the capacitor AC voltages of phase a

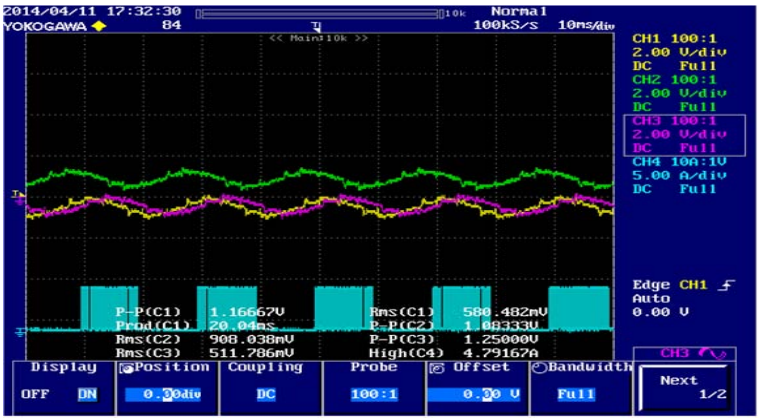

Fig. 16: Three-phase filtered AC currents (Phase a-yellow, b-green, c-magenta) and SVPWM signal (blue)

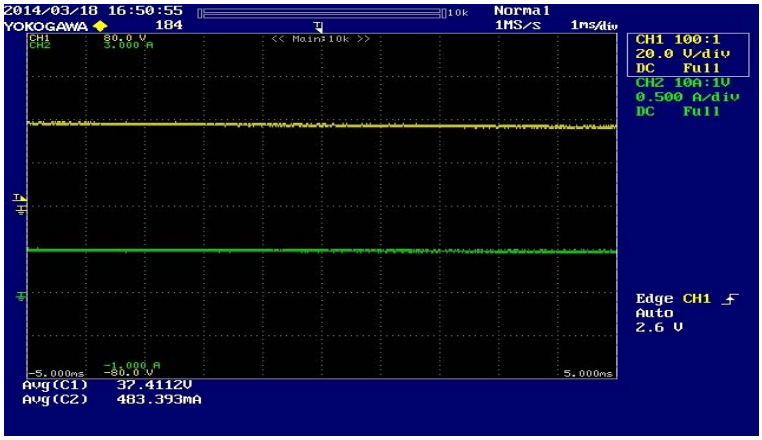

Fig. 17: DC output current (green) and DC output voltage (yellow)

and c are shown in yellow and magenta, the AC current of phase a is shown in green and SVPWM signal for switch S_5 is shown in blue. It can be observed that the capacitor AC voltages are unbalanced. The power factor of the buck rectifier is calculated to be 0.81 leading. The three phase AC currents have a frequency of 50 Hz and are 120° apart as shown in Fig. 16. Figure 17 shows the output DC voltage and current for the 80 Ω load.

CONCLUSION

This study has demonstrated that it is feasible to design and develop a three-phase buck-type PFC PWM rectifier in simulation and in hardware. The buck rectifier is designed to produce SVPWM switching signals following the SLO algorithm in matlab code. Initially, the discontinuous AC currents produced by the switches are in phase with the phase voltages produced by the switches. However, this unity power factor is slightly deteriorated by the input lowpass filter capacitor which results in a close to unity leading power factor as shown in the simulation results. The simplicity in controlling the buck rectifier enables it to be easily implemented by just using the duty ratio generator Eq. 1, the look-up Table 2 and cascade control with two PI controllers. The simulation results section proves that it is possible to operate the buck rectifier in low power as well as high power modes in closed loop output DC voltage control. Simulation results were used to verify the correct working procedure of the Hardware buck rectifier. However, the simulations were only ideal behavior of the buck rectifier so hardware behavior and results were found to be different. The open loop hardware tests and results shown in results from hardware implementation section prove that the buck rectifier is capable of operating at low power.

RECOMMENDATIONS

The distortion in capacitor voltages may be due to an unbalanced AC voltage source and may be reduced by using Phase Locked Loop (PLL) to generate reference AC

capacitor voltages of the correct amplitude. When open loop control of the buck rectifier works normally without any irregularities in the DC output, high power levels like 7.5 KVA can be tested. High power testing of buck rectifier under open and closed loop control should then be verified with simulation results obtained earlier to ensure normal operation of the buck rectifier.

Father hardware tests that can be done on this project includes an investigation into the effect of load on power factor as discovered in the load disturbance section of simulation results. And an investigation into the effect of PI values in current and voltage controllers on the THD of filtered input AC currents. A balance needs to be struck between DC output characteristics such as quick response and minimum overshoot versus AC input characteristics such as smooth three phase sinusoidal AC currents with minimum THD and maximum power factor.

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