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A High Speed SLVS Driver Based Transmitter for Low Power Serial Links

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Abstract: The study presents the design of a power efficient high-speed transmitter using a new SLVS (Scalable Low Voltage Signalling) driver architecture. It is a chip to chip signalling protocol which is aimed to provide maximum performance and minimum power consumption. It is also a differential signalling system that transmits information on a pair of wires as the difference between the two single ended output voltages. SLVS offers advantages like high noise tolerance, low power consumption and high speed in transmission when compared to previous diver architectures. It can provide a data transmission rate up to tens of Gbps. It is widely used in applications like video, storage and data communications. The project work is done in Cadence Virtuoso and 55 nm technology is used.

Key words: SLVS driver, transmitter, serial links, storage, consumption

INTRODUCTION

In present day communication system, there is an ever-increasing demand for high data rate. This leads to the emergence of several leading industrial standards. Data transmission standards aims to provide low implementation cost, high speed data transfer and low power consumption. SLVS offers gigabit performance levels with milliwatt power consumption. Its differential signalling nature makes it highly noise tolerant. As differential signalling mechanism results in common mode rejection the voltage difference will always remain same and unaffected by noise variations. Low power consumption and high-speed characteristics of the circuit is due to the smaller signal swing. This driver configuration is widely used in applications which demands high speed and low power (Purushothaman and Parikh, 2015a, b).

A transmitter, receiver and channel are the main components of a typical communication link shown in Fig. 1. Transmitter takes digital data input and convert it to analog wave forms which is then transmitted through the channel. The receiver will convert these back to digital data. A channel is a physical medium, it can be coaxial cable, twisted-pair cable and so on (Lee *et al*., 1995). It is a lossy medium hence there are chances that the signal being transmitted will get attenuated before it reaches receiver (Menolfi *et al*., 2007) (Table 1).

Initial transmitter architectures where implemented using low voltage pseudo ECL logic. This had very high driving capability but involves very high-power consumption also. Later came the use of Current Mode Logic (CML) which was better than ECL logic but still involved high power due to its parallel termination logic. Later came the introduction of Voltage Mode Logic (VML) which uses only less power because of its differential termination logic. Even though it is less accurate than CML logic, it can serve the mobile applications perfectly. LVDS and SLVS drivers are widely used drivers in VML logic. SLVS proves to be more effective than its corresponding LVDS drivers (Wong *et al*., 2004; Purushothaman and Parikh, 2015a, b; Sahoo and Razavi, 2013).

Our objective is to have a transmitter with low power and compact area that works in high frequency range from around 40-7.5 GHz that gives data rate of

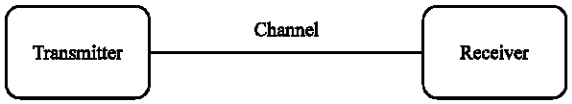

Fig. 1: Communication link

Table 1: Specifications of high speed transmitter

Parameter	Minimum value	Typical value	Maximum value
Resistance	40 Ω	50 Ω	62.5 Ω
Vod (Vdp-Vdn)	140 mV	200 mV	270 mV
Vcm ((Vdp+Vdn)/2)	150 mV	200 mV	250 mV
tr and tf	50 ps		160 ps
Jitter (with noise)			80 ps
Power (main driver)			3 mW
Power (pre-driver)			1.5 mW
ΔVcmtx			±5 mV(3)

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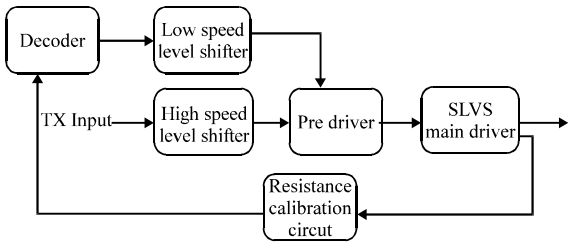

Fig. 2: Block diagram of transmitter

80 Mbps to 15 Gbps and that provide less termination variation across all PVTs. A high-speed transmitter is used to transmit data and a low power transmitter is used to send clock. HSTX usually have a signal swing of 300-100 mV. This study is organized as follows.

Proposed transmitter architecture: The Transmitter Architecture consist of five main blocks: Level Shifter, Pre-driver, SLVS Main Driver, Decoder and Resistance Calibration Circuit as shown in Fig. 2. The digital data input and enable signals which are at a lower voltage level say 0-0.8 V are level shifted to higher levels say 1.08-1.32 V using level shifter circuits before it is applied to the main analog circuitry. The pre-driver enhances the signal quality before it is applied to high speed transmitter output driver. The driver is designed to meet the specifications that are required to transmit the signal properly through the channel to the receiver. If the resistance specifications are not meeting, the variation is detected by the resistance calibration circuit. This in turn will generate a 4 bit decoder input which produces an 8 bit output that controls the no of parallel output driver stages to be turned on. Hence, the resistance value falls back within limits.

SLVS main driver: The proposed main driver is formed using NMOS transistors arranged in the form of an H-Bridge configuration. Like previous architectures it is also having a differential structure. It eliminates reflections by impedance matching and thereby provides maximum performance. It achieves minimum power consumption by small signal swing. The driver determines the transmitter specifications like impedance, rise-fall time, power and area. The termination impedance of the transmitter is made equal to the characteristic impedance of line (say 50 Ω) for impedance matching. A signal will propagate properly through a channel only if the impedance remains constant throughout. The impedance mismatch will result in reflections. Proper terminations at source and load end reduces reflections. This architecture shown in Fig. 3 is adopted for main driver as it offers less leakage, coupling, loading, etc. These decreases due to increased series resistance in the path. Since, these series resistances contribute most of the terminal impedance,

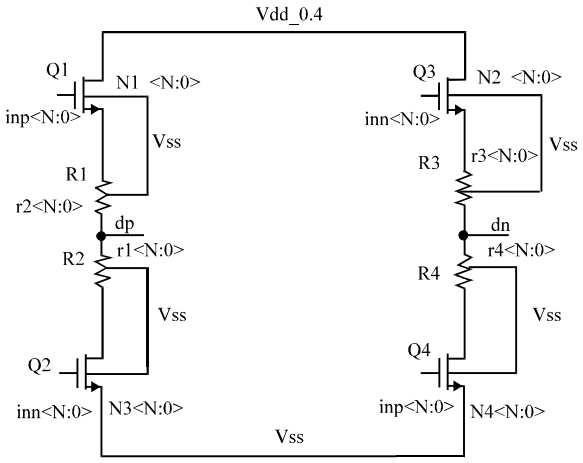

Fig. 3: Proposed SLVS output driver

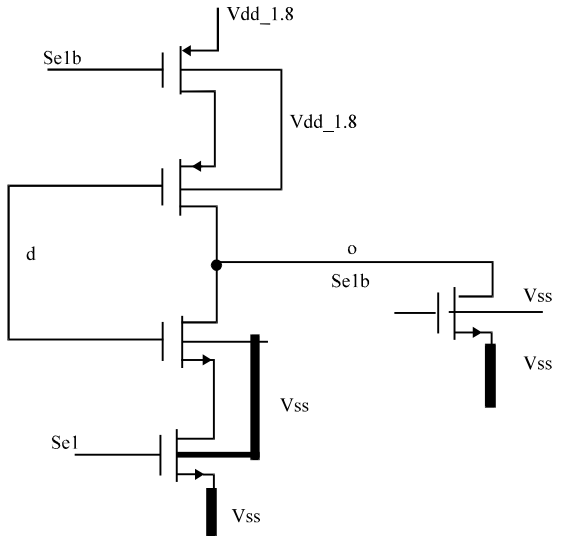

Fig. 4: Pre-driver

the mismatch factor also reduces tremendously. Usage of all the FETs as NMOS in the upper and lower part of leg also make a contribution towards mismatch reduction. To achieve a small impedance of about 50 Ω several identical stages are used in parallel. The resistance offered at particular time determines the no of stages to be turned on for that particular corner.

Pre-driver: It is a buffer stage formed by connecting two tristate inverters in series. The tristate inverter enable is formed using decoder output. It determines the no of Pre-driver stages to be turned on to transfer the data to channel. Paths with different delay, that is pre-driver segmentation, can be done based on requirement (Purushothaman and Parikh, 2015a, b; Purushothaman, 2016). The architecture in Fig. 4 shows a pre-driver

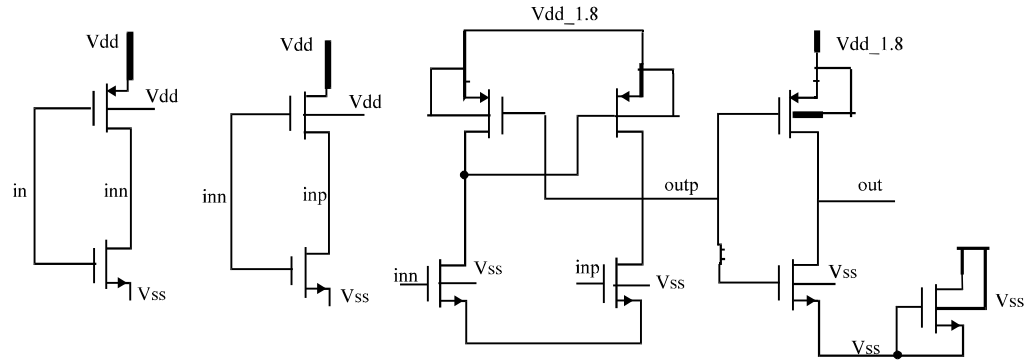

Fig. 5: Low speed level shifter

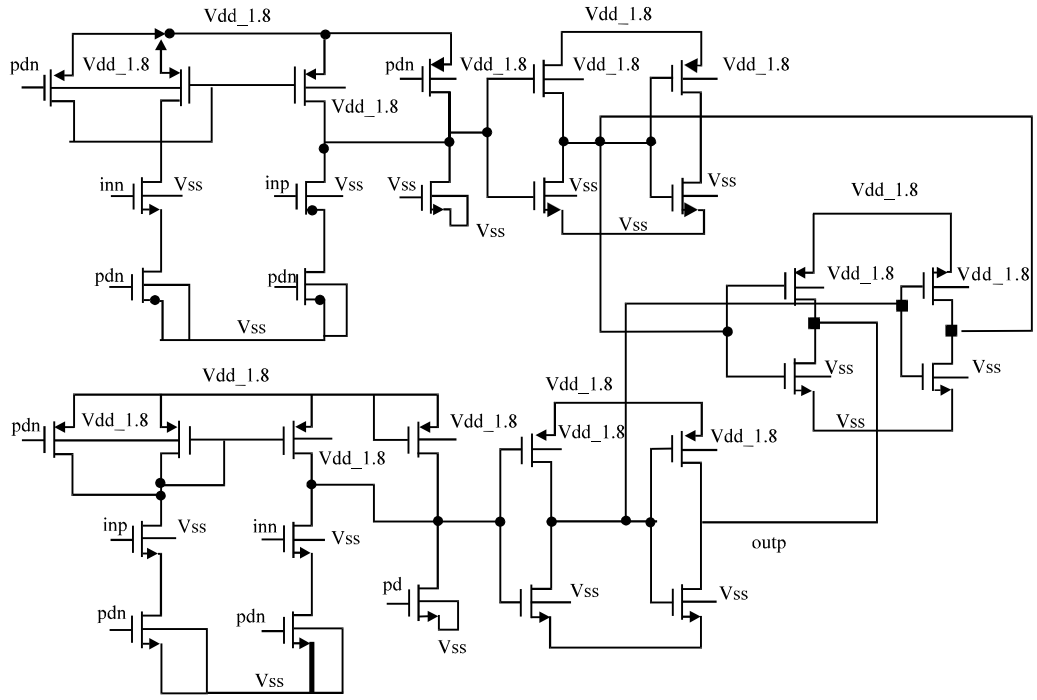

Fig. 6: High speed level shifter

with enable signals at the extreme ends. This architecture offers advantages like lower delay for input and less glitches at output, due to enable signal variations. From the circuit point of view, the rise and fall time of the signal increases due to limited channel bandwidth. This leads to inter symbol interference effect based signal degradation. This effect can be compensated by introducing pre-emphasis at transmitter. Pre-driver does the action of pre-emphasis in transmitter. Boosting of the high frequency components of the signal before it is sent through the channel is pre-emphasis. This action is achieved by slew adjustment.

Level shifter: Level shifter circuits are used for boosting the level of digital data and enable signals. The digital data at a lower level is level shifted to higher levels to make it compatible with the analog circuitry. Low speed level shifters (Fig. 5) are used for enable signals while High speed differential level shifters (Fig. 6) are used for input. As head room is less the structure in Fig. 6 is more effective for input that is switching at a high rate.

Table 2: Decoder truth table

Select input	Output	No. of stages
0000	0000 0000	16
0001	0000 0001	17
0010	0000 0011	18
0011	0000 0111	19
0100	0000 1111	20
0101	0001 1111	21
0110	0011 1111	22

Decoder: Decoder receives its select signals from resistance calibration circuit and its output act as enable for pre-driver section (Table 2). It determines

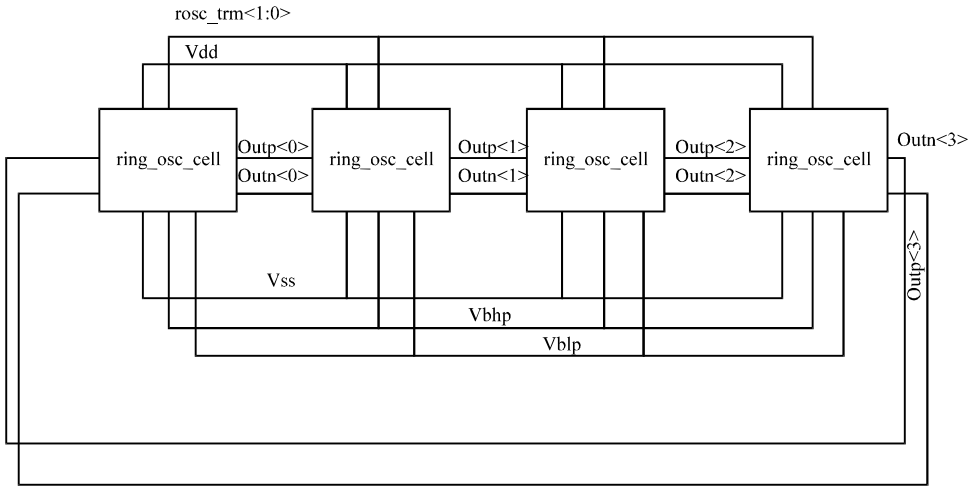

Fig. 7: Ring oscillator block

the on-stage number and thereby the equivalent output resistance value. It is implemented usingmultiplexers. The decoder truth table is shown in Table 2.

Resistance calibration unit: It is used to meet the terminal specifications. It determines the effective stage ratio required to achieve the required resistance. This section is composed of a ring oscillator and counter. The output driver leg is used as the load of ring oscillator. It produces oscillations of varying frequency according to load variations in corners (Behzad, 2001). Even no of stages are used so as to achieve symmetry while implementing the corresponding circuits layout (Fig. 7) (Baker, 2009) Number of pulses in the output of the ring oscillator is determined using the counter by comparing with a 1 MHz reference clock. This count is mapped with a 4 bit code which is given as input to decoder. The counter block is implemented using Verilog coding.

RESULTS AND DISCUSSION

Simulation results and observations: A digital data input and enables is applied to the circuit at 0.8 V. The circuit is simulated with pre-driver supply 1.8 V and main driver supply 0.4 V. Data input 2.5 Gbps is used as the test case. At typical corner a leg (combining upper and lower parts) is designed to have an impedance of 2 K, so as to achieve an effective impedance of 100 ohms the driver requires 20 stages (say at typical corner).

Similarly, the stage ratio is determined for all corners and thereby the decoder input is determined. It is found that except resistance specifications with initial configuration all other specifications where obtained in range shown in Table 3. To achieve resistance specifications also we used calibration section. The ring oscillator is designed to operate at typical corner at a frequency of 210 MHz at typical corner. A main driver with 24 stages is used here. Default will keep 16 stages on and 8 stages programmable. Hence, the decoder required is a 4-8 decoder. The calibration code is designed to give the calibrated resistance at around 8 u.

The output waveform is shown in Fig. 8 and transmitter eye diagram is shown in Fig. 9. Table 4 shows the Impedance variations with and without calibration. Table 5 shows the no of stages required to achieve 100 Ω termination value and the resultant ring oscillator frequency at all corners. It is seen that the variation which was initially 22% was reduced to about 7% in impedance spec. The maximum jitter spec. without supply noise is 4.865 ps and with +/-5% noise is 32.8 ps which falls within the required maximum specifications. The total power consumption of the transmitter is obtained around 2.3 mW. This reduction in power consumption in SLVS circuits is due to lower swing and small common mode voltage. The LVDS circuits won't work when supply is scaled further down and the common mode voltage is fixed at 1.2 V which is very high (Reyes *et al*., 2014). The Δvcmtx variation is detected using Monte Carlo analysis shown in Fig. 10, the maximum 3 variation of ΔVcmtx is only ±145.408 uV.

By using the new driver architecture several advantages where obtained like reduction in short circuit current, cross bar current, mismatches and regulator loading. Here major contribution of terminal impedance is

Table 3: Parameter variation result across corners

Parameter	TT 27deg	FF -40deg	FF 125 deg	SS -40deg	SS 125deg
Vdp	300.2033 mV	290.437 mV	289.029 mV	313.902 mV	309.623 mV
Vdn	98.67844 mV	104.422 mV	110.968 mV	86.041 mV	93.673 mV
Rdn	48.96 Ω	56.13 Ω	62.31 Ω	38.26 Ω	43.35 Ω
Rdp	49.52 Ω	58.90 Ω	62.32 Ω	37.89 Ω	41.78 Ω
Vod	201.5248 mV	186.0149 mV	178.058 mV	227.064 mV	216.047 mV
Vcm	199.4408 mV	197.429 mV	199.9 mV	199.953 mV	201.697 mV
tr	118.8 ps		132.7 ps	141 ps	97.23 ps
tf	103.8 ps		107.7 ps	116.9 p	96.7 ps

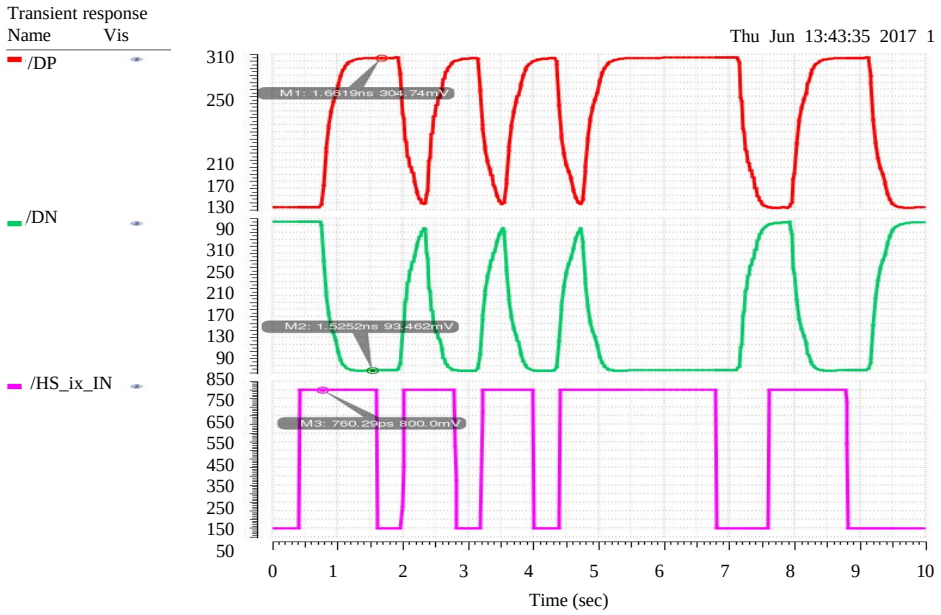

Fig. 8: Output of transmitter at typical corner

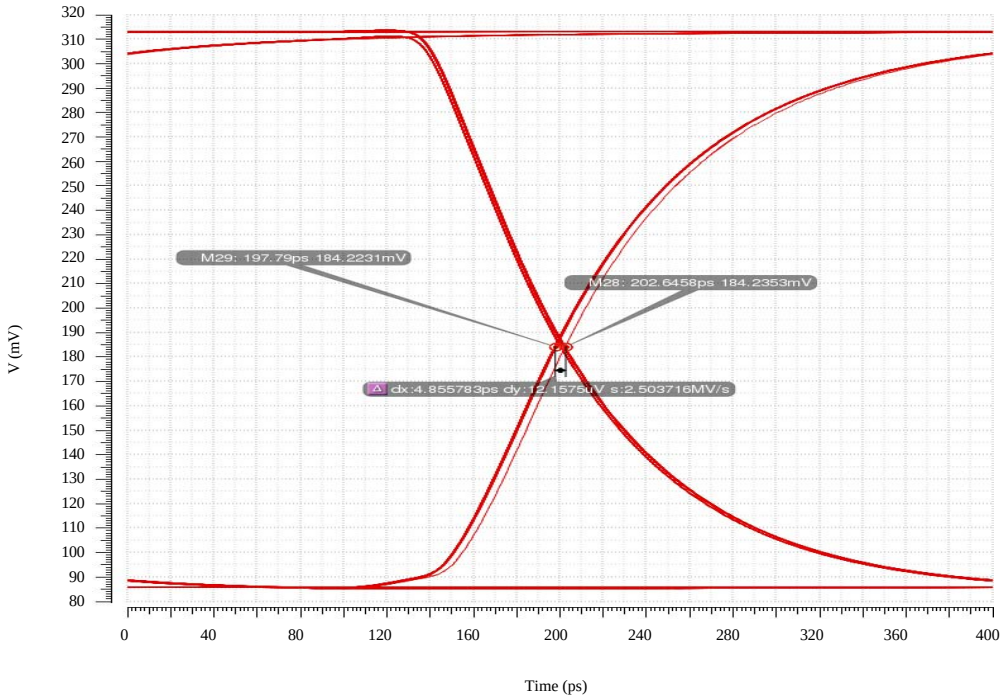

Fig. 9: Eye diagram of transmitter

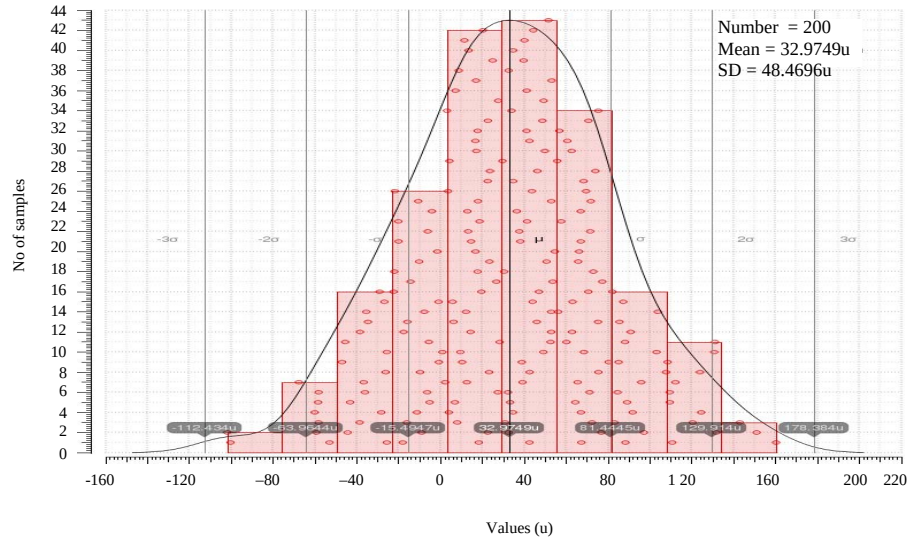

Fig. 10: Monte carlo for ΔVcmtx

Table 4: Impedance variations

Parameter	min (Ω)	typ (Ω)	max (Ω)
Before calibration	37.87	49.5	59.36
After calibration	46.40	49.5	53.57

Table 5: Frequency and stage count variation

Corner (°)	Impedance (K)	Stage count required	Oscillator Freq. (MHZ)
TT 27	1.967	20	210.82
FF -40	1.520	16	277.70
FF 125	1.702	18	238.10
SS -40	2.489	22	191.70
SS 125	2.295	23	162.30

made by Resistors than FETs. Resistor contributes around 75% of the total terminal impedance value. Hence a further additional power reduction is achieved. It was found that the power consumption was about 0.41 mW with no resistors and is reduced to 0.23 mW with resistors (Jeong *et al*., 2012).

CONCLUSION

The implementation of high speed low power Transmitter for serial links is discussed in this study. The Transmitter is implemented in 55 nm CMOS technology. It was observed the circuit offers very low power consumption. Supply scaling and low common mode voltage makes it more power efficient than LVDS. It is found that SLVS architectures use almost less than half the power of LVDS structures. The new architecture of driver with resistors in between makes it further more power efficient. Performance wise the new architecture offers about twice better than previous architectures of SLVS Drivers.

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