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Performance Evaluation of Parallel Multipliers

A.L. Siridhara, Mahendra Vucha and T. Ravinder
Department of Electronics and Communication Engineering,
MLR Institute of Technology, Dundigal, Hyderabad, 5000043 Telangana, India

Abstract: Now a days multimedia applications are demanding high speed computing architectures. Adders and multipliers are very important functional blocks in Arithmetic and Logic Unit (ALU) of high speed computing architectures. For computing systems fast multiplication is always a significant requirement for high performance. This study presents the implementations of the high speed multipliers and their comparative analysis. In this study, we have proposed VLSI architecture for widely used parallel multipliers such as Booth's multiplier, Wallace multiplier and Dadda tree multipliers in order to acquire their design attributes like speed, area. The acquired design parameters of the multipliers can be analyzed to design optimum speed Multiply and Accumulate (MAC) unit used for multimedia applications like filters, synthesizers, wireless communication channels, etc.

Key words: Arithmetic logic unit, Digital Signal Processing (DSP), Serial Parallel Multiplier (SPM), Multiply and Accumulate Unit (MAC), multimedia applications, computing architectures

INTRODUCTION

Multiply and Accumulation (MAC) unit in digital signal processors contains the combination of adder and multiplier. The architecture and comparison study of various adders and few multipliers used in MAC has been demonstrated in literature (Gurjar *et al*., 2011; Sudeep *et al*., 2014). The multiplication is a performance critical unit in most of the microprocess or digital signal processor and graphics engines. Fast multipliers are essential in advance electronic systems where high speed calculations are required such as digital signal processors, microprocessors and FIR filters, etc. At present time taken to perform multiplication operation is important in determination of instruction cycle time period of a DSP chip. Since, the demand of high speed computing for signal processing applications is increasing, many Digital Signal Processing (DSP) systems started using high speed multiplication unit for implementing algorithms such as convolution, filtering and frequency analysis. There are three types of multipliers called serial multiplier, parallel multiplier and serial-parallel multiplier.

Serial multiplier: In serial multiplication, sequential circuits are being used with feedbacks. The inner products are sequentially produced and then added serially as per the operation. The speed of serial multiplier is less as compared to parallel multiplier because (Callaway and Swartzlander, 1993). Serial multiplier adds each bits of the multiplicandand sequentially and this process is repeated for each of the multiplier bits (Wallace, 1964). Only one adder can beused to add m×n number of partial products where m and n are number of bits of multiplicand and multiplier, respectively.

Parallel multiplier: In the parallel multiplier, multiplying the multiplicand with each bit of the multiplier is done first for generation of partial products. Then to generate a resultant product P these partial products are added in parallel together. The parallel multiplication process can be consider as two parts, namely partial product accumulation and partial product generation. Number of partial products which are to be added plays significant role in determining the delay caused by the parallel multiplier. Parallel multiplier is further divided into array multiplier and tree multiplier. Booth's multiplier is kind of array multiplier and Wallace and Dadda is a kind of tree multiplier and it also known as column compression multipliers.

Serial-Parallel Multiplier (SPM): SPM operates on each bit of multiplier serially but it uses parallel adder for partial product accumulation. It brings intermediate trade-off between serial multiplier which is time consuming and parallel multiplier area consuming device.

MAC unit: A MAC unit consists of accumulators and multipliers that contains the sum of the previous

Corresponding Author: Ravinder Tirupati, Department of Electronics and Communication Engineering,
MLR Institute of Technology, Dundigal, Hyderabad, 5000043 Telangana, India

consecutive product (or) products. MAC unit is one of the vital block for digital signal processing system and plays important role in its delay and area determination. The MAC unit function is given by the following eqution:

$$P = \sum_{(i=0)}^{N} A_i \times B_i, N = \text{Length of the sequence}$$

Where:
P = The product
A and B = The multiplicand and multipliers, respectively

MATERIALS AND METHODS

Due to the high speed functioning, column compression multiplier is prolonged for study. This multiplier total delay is proportionate to the logarithm of the input word length. The column compression multipliers are rapider than array multipliers in which delay varies linearly with operand word length. According to Callaway and Swartzlander (1993) column compression multipliers are more power proficient as compared to array multipliers. Wallace (1964) introduced a method for fast multiplication centred on summing (or) adding the partial product bits on parallel by using carry save adders as a tree of which was recognized as Wallace tree. Dadda (1965) later advanced Wallace's method with a significant compressor placement strategy that requires fewer compressor in partial product reduction stage with fee of larger carry propagate adder Veeramachaneni proposed novel architectures and the designs of low power and high speed compressors used for addition in the partial product addition stage or accumulation stage. The compressors 3:2, 4:2 and 5:2 are the essential components in many applications where addition is required most importantly in multiplication (Veeramachaneni *et al*., 2007). Booth multiplier algorithm works by analyzing the initial partial product P last two bits and the corresponding operation of (01) add (10) subtract (11, 00) arithmetic right shift operation is done on the partial product P and this stage prolongs for n bit stages. Booth multiplier along with additional modules like logic functions, subtraction module, addition module division module squaring module are combined to design calculator (Sharma *et al*., 2014). Malik and Dhall, they had designed a MAC that consisted of 8 bit Booth's multiplier, 16 bit ripple carry adder and 17 bit accumulator (the accumulator is made of parallel in parallel out shift register). The basic operation of MAC is the product of X_i and Y_i is always given to the 17 bit-accumulator and then again added with successive product of X_i and Y_i (Malik and Dhall, 2012). In the year 1950's, multiplier speed was notably improved with the introduction of Booth multiplier. Booth's method and the modified Booth's method does not require a rectification for the product when either or both the operands is negative for two's complement numbers (MacSorley, 1961). The MAC unit (Sen *et al*., 2013) is composed of 17 bit register, 17 bit accumulator (its 17 bit carry look-ahead adder used to increase the speed), 8 bit Wallace tree multiplier and then 18 bit register. The MAC has the ability to multiply and add with the previous product for 8 times. It also consist of block enabling technique in which the block which is not being used for the operation will be kept off.

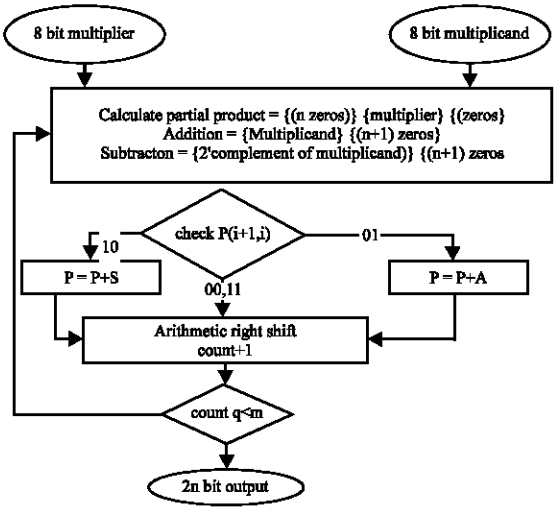

Fig. 1: Flow chart of Booth's multiplier

Behaviour and architecture of parallel multipliers

Booth multiplier: Implemented Booth's multiplier using Booth's algorithm is one of the important algorithm to perform a signed number multiplication. It consist of repeatedly adding one of thetwo already determined values A and S to a initial product P, then performing the rightward arithmetic shift on P. Let's consider x and y be the multiplicand and multiplier. Let n_x and n_y represent the number of bits with in x and y. The flow chart of fast Booth's multiplier algorithm to obtain the product of x and y is shown in Fig. 1.

Wallace tree multiplier: Wallace (1964) introduced a method for the multiplication centred on summing the partial product bits inparallel using a tree of carry save adders which became well-known as the Wallace tree. The flow chart of Wallace-tree multiplier is shown in Fig. 2.

Implementation of digital multiplier is reliant to the scheme used for addition of partial product array bits. As delay is proportional with the size of the multiplicand, the multiplier blocks will need a large quantity of time to perform the task. Therefore, partial products are condensed using a technique called carry save addition

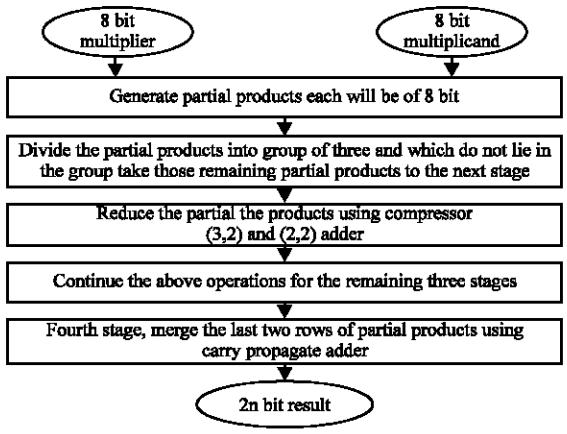

Fig. 2: Flow chart of Wallace multiplier

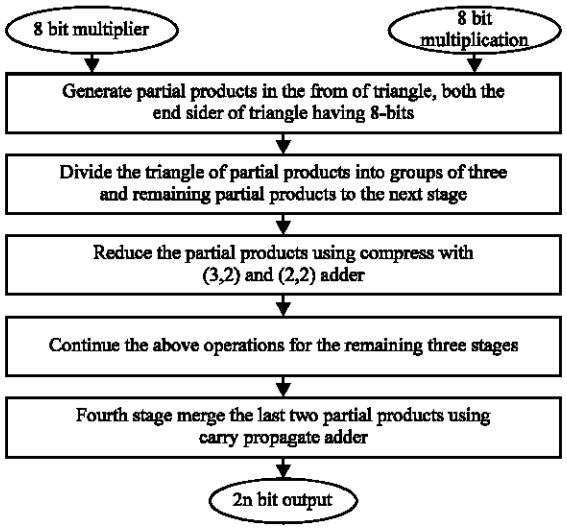

Fig. 3: Flow chart of Dadda multiplier

which allows successive additions in one global step. In the carry-save adder, carry transmission is avoided by treating the intermediary carries as outputs instead of advancing them to the next higher bit position.

Dadda multiplier: The Dadda multiplier follows refined Wallace's method. The flow chart of Dadda multiplier is shown in Fig. 3.

RESULTS AND DISCUSSION

The above implemented multipliers are simulated using Xilinx and synthesized using Xilinx 13.2, Virtex-5, XC5VLX110T-FF1136. The synthesis results for all three multiplier are obtained and their attributes are analyzed. The attributes, i.e., area and speed of the parallel multipliers are summarized in Table 1. Table 2 demonstrates the detailed comparative analysis of the

Table 1: Summary of parallel multipliers

Multiplier algorithm	Area (number of bit slices)	Delay (nsec)
Booth	95	3.2900
Wallace	107	14.6650
Dadda	111	12.8340

Table 2: Summary of multipliers is depicted at 500MHz

Multipliers (500MHz)	Area (μm^2)	Power delay product (aJ)	Transistor count	Average power consumption (μW)	Delay (ps)
Booth wallace	11.78	1252.69	281	34.15	40.29
Array	17.75	1388.60	367	38.07	40.75
Column bypass	16.20	1313.29	301	35.12	40.15
Row bypass	17.57	1411.66	321	36.80	41.29
Vedic	19.57	1375.81	588	40.06	41.67

Table 3: Summary of ultipliers is depicted at 1 GHz

Multipliers (1 GHz)	Transistor count	Average power consumption (μW)	Delay (ps)	Power delay product (aJ)	Area (μm^2)
Booth Wallace	285	49.29	39.90	1286.10	11.85
Array	369	53.06	39.72	1396.33	18.73
Column bypass	300	53.12	39.75	1330.70	15.26
Row bypass	325	52.29	40.35	1421.51	17.53
Vedic	588	54.33	40.54	13782.45	19.36

implemented multipliers in terms of delay, area. From Table 3, Booth's multiplier delay is 3.29 nsec, Wallace multiplier delay is 14.665 nsec and the delay for Dada multiplier is 12.834 nsec.

CONCLUSION

The behavior of parallel multipliers Booth, Wallace and Dadda multiplier is described using Verilog HDL and then simulations results and synthesis reports are obtained. The synthesis report for the multiplier shows that Booth's multiplier has the least delay and can be used for low cost application devices. Further, study and comparative analysis can be done on higher range multiplier like 16, 34 and 64 bit. In future, the analysis can be carried out on a single precision and double precision floating point multiplier.

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