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Design of 128-Point FFT using Mixed Radix with Combined SDF-SDC Structure for OFDM Application

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Abstract: Fast Fourier Transform (FFT) is one of the major operations in any communication system. The efficiency of the communication system is depends on the internal process (FFT/IFFT) of the system. In this study, designed a VLSI based 128-point mixed radix with combined Single path Delay Feedback (SDF) Single path Delay Commutator (SDC) FFT structure. The mixed Radix-2 and Radix-4 FFT architecture provide fast computation during the process. Combined SDF-SDC dataflow structure has different advantages, SDF structure is used to improving the speed of the process and the SDC structure is used to reducing the area (LUTs and slices) utilization and also reducing the power consumed by the processor. Because of these advantages only combined the both structure and get the efficient performance of the FFT architecture. The proposed architecture is applied into the OFDM communication system for speed transmission. Simulation of the proposed architecture is done by using ModelSim simulation environment. The performance can be analyzed and validated by Xilinx plan-ahead 12.4 tool.

Key words: Mixed Radix-2 and Radix-4, Single path Delay Feedback (SDF), Single path Delay Commutator (SDC), Xilinx plan-ahead 12.4, ModelSim

INTRODUCTION

In wireless and digital communication system used Orthogonal Frequency Division Multiplexing (OFDM) for many reasons; these are reconfigurability, less hardware utilization, low power consumption and so on. OFDM is a multi-carrier transmission system because it convert single data stream with higher data rate to multiple data streams with low data rate which are orthogonal to each other. Different types of functions are present in both the transmitter and receiver of the OFDM system. Frequency transformation is the essential step of OFDM system. Fast Fourier Transform (FFT) and Inverse Fourier Transform (IFFT) are the technique used to perform the transformation from time domain signal to frequency domain signal and frequency and vice versa. FFT processor present in the receiver of the system, likewise IFFT is present in the transmitter part. Discrete Fourier Transform (DFT) is a technique to get the frequency response of time domain signal. But it contains complexity during the frequency response analysis. So, most of case FFT is preferred for computation. Decimation in Time (DIT) and Decimation in Frequency (DIF) are the two types of FFT designs. DIT-FFT process follows the divide and conquers for computing the transformation of frequency. Likewise, DIF-FFT processes follows the same divide and conquer approach for getting frequency signal from the time signal. Twiddle factor multiplication of both the DIT and DIF-FFT can be performed after the subtraction of even and odd outputs. FFT can be classified as Radix-2, Radix-4, Mixed Radix, Split Radix, etc. Based on the applications the classified FFT techniques are used. In the FFT architecture different feedback structures are widely used to convert time domain to frequency domain. The feedback structures are Single path Delay Feedback (SDF), Multipath Delay Feedback (MDF), Single path Delay Commutator (SDC) and Multipath Delay Commutator (MDC). These feedback structures are not applied at a same time, because each structure has different advantages and different drawbacks, based on the advantage the feedback structure is selected. In the VLSI system design, every feedback structure offers high speed of computation and every commutator structure offers less LUTs and slices

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utilization and low power consumption. If suppose a need both the advantages can combine the feedback and commutator structures. The combined architecture provides high speed, less area and low power utilization. Without the FFT/IFFT process cannot process the signal in the transmitter and the receiver.

Literature review: In a wireless communication OFDM is a key technique for high spectral efficiency and high data rate. Fast Fourier Transform (FFT) processing is one of the key processes in OFDM systems. Parallel FFT and pipelined FFT are the types used in the system. Now a day's pipelined FFT is mostly used in the system for high speed communication. Adiono *et al.* (2009) proposed a 64 point Radix-4 FFT for OFDM applications. Twiddle factors values are not stored in ROM; instead of using ROM pipelined FFT can access the value directly. Radix-4 algorithm is better because it reduces the steps for reducing the butterfly structure. It is faster than Radix-2 algorithm. To increases the point in the FFT structure has processes the large amount of data and provides a higher speed.

In general FFT algorithm can be developed in two ways, Decimation in Time (DIT-FFT) and Decimation in Frequency (DIF-FFT) are the methods developing the FFT algorithm. Both the methods have same complexity and operations but only one different is the input and outputs are arranged differently. Sowjanya and Balivada (2013) proposed a Radix-2, Radix-8 and Split Radix algorithm. In Radix-2 algorithm the computation is split into odd and even pairs. The number of stages is higher in this radix. Radix-8 FFT process is used to improve the speed of the computation. Split radix is combination of two or more radix. Split radix method provides better performance than Radix-2 method like speed, LUTs and slices utilization. Split radix is preferred for High speed applications.

Yang *et al.* (2013) has been proposed a new Multipath Delay Commutator (MDC) based FFT/IFFT processor for MIMO-OFDM system. In a traditional MDC structure occupy most of the area for storage. The proposed memory scheduling mechanism is to decrease the memory required for storing the twiddle factor values. The proposed architecture can use different butterfly structures at each stage. First stage is performed by Radix-4 and the last stage is performed by Radix-8 method because the twiddle factor multiplication is done by constant multiplier. MDC structures occupy less area utilization and consume low power than compared to the other feedback structures. The power saving is achieved by reduction in usage of memory element in the processor.

Algnabi *et al.* (2012) presented a pipelined Radix-2 Single path Delay Feedback (SDF) with digit slicing. SDF structure is mostly used for high speed applications. In the structure a digit slicing based multiplier less method is used for fast computation. The designed slices contain four blocks, each block carrying four bits. It uses shift and addition technique for multiply the two values. The right shifts twiddle factor value stored in the ROM. The multiplier less architecture takes less area utilization. The implementation had been done by verilog HDL codes language and tested into the FPGA hardware. The performance is very much improved than the other conventional techniques.

Fast Fourier Transform (FFT/IFFT) is a process to convert a signal from time to frequency and vice versa. The main purpose of the FFT is improving the speed of the communication system. He and Torkelson (1998) developed a high speed and power efficient multiplier for FFT applications. Most of the VLSI based architecture adders and multipliers play an important role. FFT design is also based on multipliers and adders. To increase the speed and reduce the power consumption of the FFT using Adaptive Hold Technique (AHT) based multiplier. Multiplier with AHT is most efficient in power and also adjusts the cycle pattern percentage to minimize the performance reduction. It also eliminates the timing error, so, can do error free operations. The modified FFT applied into many applications.

MATERIALS AND METHODS

Radix-2 FFT structure: Fast Fourier Transform (FFT) is classified in both time and frequency. The time based FFT is denoted as DIT-FFT and the frequency based FFT is denoted as DIF-FFT. Both the operations are same only the difference is bit reversal. In DIF-FFT process the normal input bits and the DIT-FFT process the bit reversal inputs. In previous, Discrete Fourier Transform (DFT) is used to process the frequency and time transformation. But today all are using FFT process for computation, the reason is DFT is very difficult to design. One of the drawback is complexity is referred as O (n^2). To overcome the problem by introducing the FFT processor to make the computation faster. N-point DFT time signal is represented as:

$$X_k = \sum_{n=0}^{N-1} x_n \, W_N^{nk}, 0 \le k \le N\text{-}1 \quad (1)$$

Where:

N = The number of points
x_n = The discrete time input signal
W_n^{nk} = The twiddle factor value

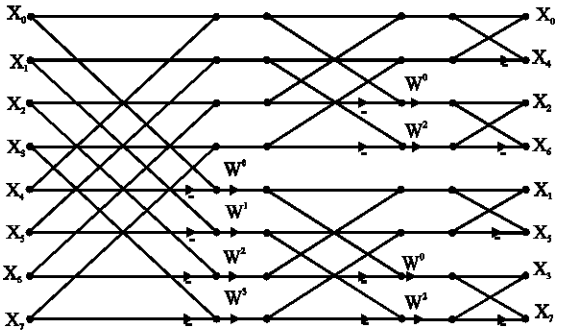

Fig. 1: Radix-2 FFT structure

In the Radix-2 FFT reduce the overall butterfly structure by step by step process. For example, the 16 point FFT can be reduced by 16-8-4-2 this is the processing steps using the Radix-2 algorithm. Data flow model of Radix-2 DIF-FFT is divide the N-point FFT into N/2 point FFT process. The signal is represented as follows (Fig. 1):

$$X[2K]=\sum_{n=0}^{\frac{N}{2}-1}\left(x[n]+y\left[n+\frac{N}{2}\right]\right)W_{N/2}^{kn} \quad (2)$$

$$X[2K+1]=\sum_{n=0}^{\frac{N}{2}-1}\left(x[n]+y\left[n+\frac{N}{2}\right]\right)W_{N}^{n}\,W_{N/2}^{kn} \quad (3)$$

Radix-2 FFT structure divides the input sample into two half, one is even weights of input and another one is odd weight of inputs. In order to reduce the computational complexity the input samples are divided and perform the operations simultaneously. Equation 2 and 3 represents the input signals of even and odd parts. Different feedback and commutator structure are introduced in the Radix-2 FFT structures for computations.

Radix-4 FFT structure: The Radix-4 FFT structure is shown in Fig. 2. Radix-4 FFT structure reduces the computation step when compared to Radix-2 FFT structure. Radix-4 stages can be performing two stages of Radix-2 FFT structure. For example, the 16-point FFT can be reduced by 16-4. Mathematical representation of input signal is follows:

$$X[K]=\sum_{n=0}^{\frac{N}{4}-1}x(n)W_{N}^{nk}+\sum_{n=N/4}^{\frac{N}{2}-1}x(n)W_{N}^{nk}+\sum_{n=N/2}^{\frac{3N}{4}-1}x(n)W_{N}^{nk}+\sum_{n=3N/4}^{N-1}x(n)W_{N}^{nk} \quad (4)$$

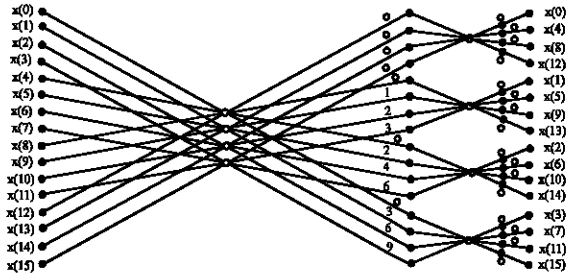

Fig. 2: Radix-4 FFT structure

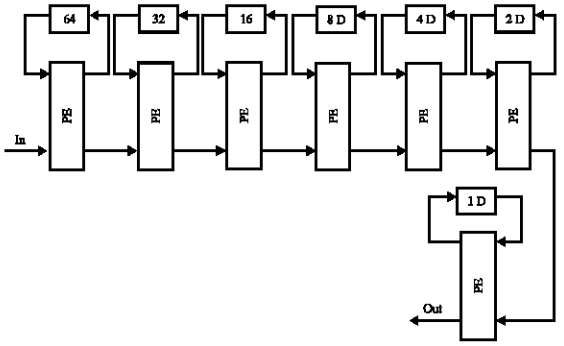

Fig. 3: Radix-2 Single path Delay Feedback (SDF) structure

$$X[K]=\sum_{n=0}^{\frac{N}{4}-1}x(n)W_{N}^{nk}+\sum_{n=0}^{\frac{N}{4}-1}x\left(n+N/4\right)W_{N}^{\left(n+\frac{N}{4}\right)k}+\sum_{n=0}^{\frac{N}{4}-1}x\left(n+N/2\right)W_{N}^{\left(n+\frac{N}{2}\right)k}+\sum_{n=0}^{\frac{N}{4}-1}x\left(n+3N/4\right)W_{N}^{\left(n+\frac{3N}{4}\right)k} \quad (5)$$

Compared to Radix-2 FFT, Radix-4 reduces the half of the steps during the computation. Also it can be achieve higher speed than the Radix-2 FFT process.

Single path Delay Feedback (SDF) structure: Single path delay feedback is a technique based on pipelined architecture (Fig. 3). It provides high speed operation during the computation process. In the Radix-2 SDF architecture the input are applied serially. It is only suitable for high speed operation; it does not concentrate the area and power consumption of the processor. In the SDF structure delay elements are used to compute the feedback structure. The number of delay elements are depends on the FFT point of operation. SDF technique is more suitable for long distance communication system. Radix structure is not problem to implement

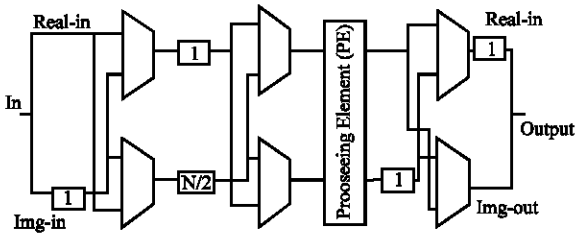

Fig. 4: Single path Delay Commutator (SDC) structure

technique the into the FFT; in any radix structure can easily apply the SDF structure. It consumes more power compared to the other type of structure.

Single path Delay Commutator (SDC) structure: In general, commutator structure is differing from feedback structure. The operation done in the FFT process is similar for both the structures. But only the difference is speed, area and power utilization. SDF structure need more delay elements to process because of the delay element the area occupied by the structure is larger and also it consumes more power. Only the advantage is it provides less delay. But the SDC structure offers less area utilization and consumes less amount of power to compute the FFT operation. The structure of SDC is shown in Fig. 4.

Mixed Radix-2 and Radix-4 architecture with combined SDF-SDC structure: Mixed radix FFT has more advantage than normal radix FFT. In the proposed architecture contain mixed Radix-2 and Radix-4 with Single path Delay Feedback (SDF) and Single path Delay Commutator (SDC) structure. The advantage of SDF structure is high speed, likewise the advantages of SDC structure are less LUTs, slices utilization and low power consumption. Both the methods have advantages and drawbacks, so, combine the SDF-SDC structure and design the new architecture. The designed architecture provides better results than compared to the individual structure. In the same way, Radix-2 FFT architecture has high computational steps than compared to Radix-4 FFT architecture. Here, the 128 point is not fully designed by Radix-2; it was designed by both the Radix-2 and Radix-4 architecture because the mixed radix architecture reduces the computational steps of the 128 point FFT architecture. Bit parallel multiplier is used for twiddle factor multiplication because it consists of adders and shifters only. It reduces the hardware complexity of the circuit. The combined SDF-SDC architecture shown in Fig. 5.

The combined architecture consists of four butterfly unit and one commutator unit. Signed addition and signed subtraction operation is performed in butterfly unit. Commutator used to relocate the real and imaginary data

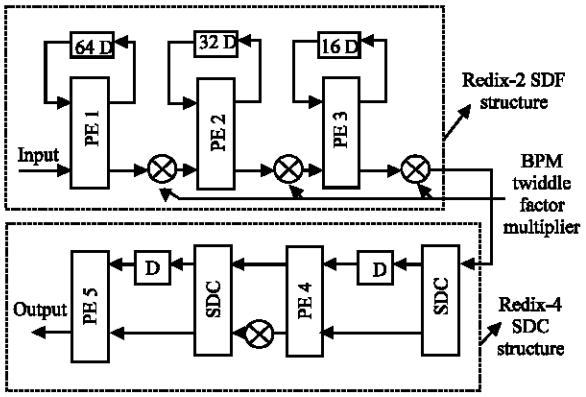

Fig. 5: Mixed radix with combined SDF-SDC architecture

Table 1: Performance evaluation of 32, 64 and 128 point mixed radix SDF-SDC FFT structure

Types of parameters	32 point mixed radix SDF-SDC FFT	64 point mixed radix SDF-SDC FFT
Number of slice registers	8165/93120	22014/93120
Number used as flip-flops	3497	7309
Number of slice LUTs	30383	86985
Number used as logic	29335	84784
Number of occupied slices	8484	10782
Number with an unused flip-flops	22577	66655
Number with an unused LUT	186	1680
Number of fully used LUT-FF pairs	7806	20330
Delay (NS)	20.241	31.291

Table 2: Performance evaluation of 64 point and 128 point normal and mixed radix FFT structure

Types of parameters	128 point normal radix structure	64 point mixed radix structure	64 point normal radix structure	128 point mixed radix structure	Reduction (%)
Number of slice registers	16544	22014	26202	26202	~
LUTs utilization	13559	7309	132923	116476	12
Delay (NS)	31.987	31.291	33.001	30.603	7.21

inputs. The relocation or position changing is used for optimizing vthe hardware complexity. The combined architecture has improved the performance better, to further improve the performance by using bit parallel multiplier. The proposed architecture is not only for 128 point FFT, it is also applicable for 256, 512 and 1024 point FFT architecture (Table 1 and 2).

RESULTS AND DISCUSSION

The design of 128 point mixed radix with combined SDF-SDC architecture has been proposed by using

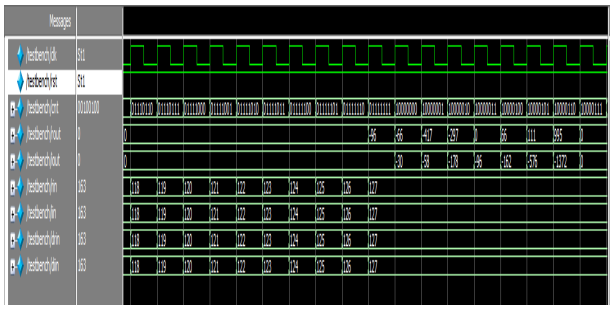

Fig. 6: Simulation results of 128 point mixed radix SDF-SDC FFT

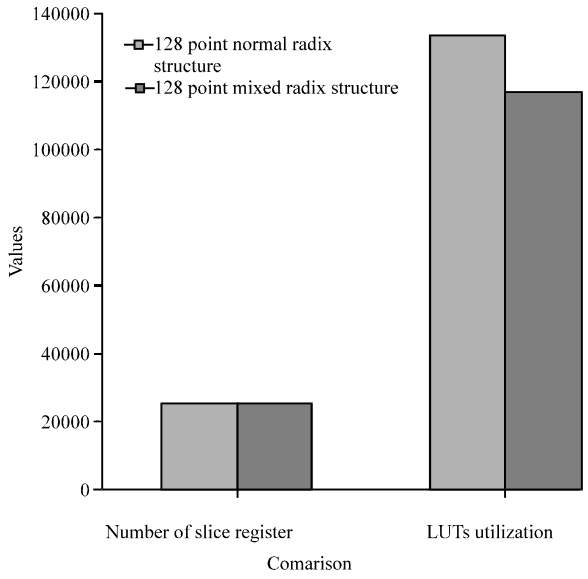

Fig. 7: Comparison graph of normal and mixed radix FFT

Verilog Hardware Description Language (verilogHDL). The advantage of 128 point mixed radix FFT has less number of computation steps compared to that the single radix FFT design.

The 128 point FFT simulation results were evaluated by using Modelsim 6.3c simulation software. The results 1were synthesized and estimated by using Xilinx plan-ahead 12.4 design tool. The simulation results of 128 point mixed radix FFT is shown in Fig. 6.

The design of proposed 128 point mixed radix SDF-SDC FFT offers 17.22% reduction in power and 43.22% reduction in area. Also, the proposed FFT structure offers 12.34% reduction in delay. It gives better performance when compared to existing FFT structures (Fig. 7 and 8).

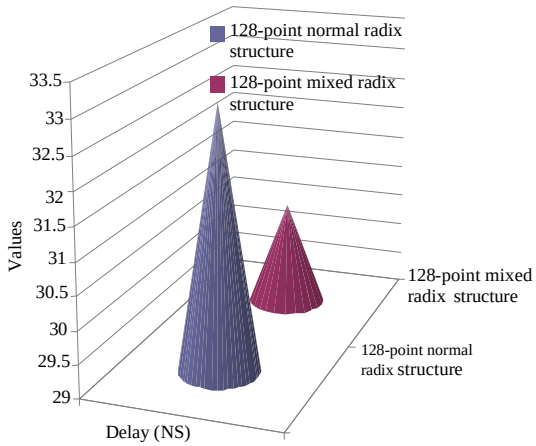

Fig. 8: Delay Comparison of Normal and Mixed Radix 128-FFT

CONCLUSION

In this study discussed about the concept of 128 point pipelined mixed radix with combined SDF-SDC architecture. The main goal of the 128 point pipelined mixed architecture is to achieve a speed and low power during the computation of FFT processor. SDF structure was used to achieve a speed; likewise SDC offered the advantages like low power and less hardware utilization. The results were synthesized and evaluated by Xilinx plan-ahead 12.4. Compared to the normal FFT structure the proposed FFT structure reduced 12% of LUT utilization and 7.21% of delay. In future points can be extended by to 512 for increasing the data rate of the OFDM system.

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