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Enhanced Launch-Off-Capture Testing Using BIST Designs

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Abstract: Now a days chip designing has become more and more complex and then the transistor size had been decreased to nanometre level. The designing of the chip is taking so long and to test, it would take many more years. So, in order to decrease the testing time circuit is made to test itself making it possible to self test which is built inside the chip. Built in self test is design which can test itself and reduce the testing time. But, there are many more difficulties in continuing the processes. One among is the transition fault. Here, we present an idea to overcome the transition fault in the bist by using the fault generation of the transition pattern methods. They are LOC (Launch Off Capture) and LOS (launch off shift) methods. And also, we are implementing the enhanced launch off capture method in the bist. Work is done by the Xilinx 14.5 Version.

Key words: BIST, LOS, LOC, ELOC, testing, Xilinx

INTRODUCTION

In vlsi testing of a circuit in chip, system or board there exists a method which tests itself it is known as the BIST (built in self test) (Abramovici *et al*., 1990; Bushnell and Agrawal, 2000a, b; Stroud, 2002; Jha and Gupta, 2003; Wang *et al*., 2006; 2007, 2009) and it is a Design For Testability (DFT) technique. It is used in many applications like life-critical and mission critical applications. They are most common in the electronics, banking sector, automobile, health care and telecommunications in these fields they require the on-chip on board and in system testing to make sure that the results are accurate. So, built in self test is necessary in these fields. With that the tested circuits which are good to go are sent to the consumers with the hope of working fine within the validity of the chip or circuit time, this is called as the off-line testing. But hoping for the circuit to work in given time for the present day ICs (Integrated Circuits) due to the sub-micron technology they may create problems during the usage within the valid time. So, a circuit is tested every time it started to make sure that the circuit is fine. If in any case a fault is occurred it can be replaced with the respective part. Testing of the circuit every time it starts is known as the BIST (Built-In-Self-Test) .The widely used bist method is based on the MISR (Multiple Input Signature Register) and stumps (parallel shift register sequence generator) structure. In the stumps architecture, a Pseudo-Random Pattern Generator (PRPG) is needed to come up with pseudo-random patterns along with change every pattern with parallel for the advices on the search within stores set within a scan based style and a multiple input signature register is needed to the lightweight particular test results moved outside of the scanned chain results in order to generate a signature. Subsequently, determined amount of evaluation cycles can be implemented, the last signature is then in comparison towards a set gold (good circuit) signature for the assessment of the CUT (Circuit Under Test) pass or not. While no test patterns are offered on the surface, logic BIST can reduce test expense and as well enable the enterprise to do in-field self-test. BIST offers many advantages; its true value is seen in at-speed testing for very high speed and extremely high performance circuits (Fig. 1).

Previously, functional patterns were employed for at-speed test out. Even so functional testing is not a new practical option as a solution due to difficulty along with the time to create checks to intricate designs with good gate thickness. Furthermore, quantity of prescribed patterns to realize high fault coverage is hugely high with regard to present day models. For that reason more robust at-speed techniques are expected as the particular number associated with timing akin defects keeps spreading and efficiency of functional and IDDQ screening was minimized (Lin *et al*., 2003). The transition fault and the path delay fault testing collectively contribute a comparatively positive protection for delay-cajoled flaws (Cheng, 1993; Mak *et al*., 2004). Path hold off model locates the aggregate delay over the entire report on gates inside a pre-defined path even though the transition fault product aims every single gate output within the design

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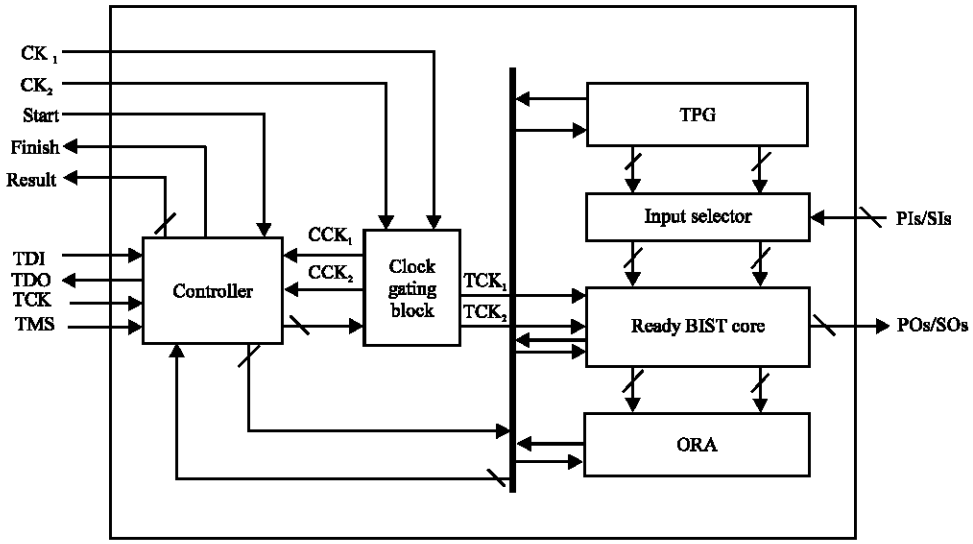

Fig. 1: The logic BIST architecture

of slow-tories along with slow to fall hold off fault (Bushnell and Agrawal, 2000a, b). Transition fault testing is broadly exercised with trade credited primarily for you to its workable fault sum (2 errors in every single gate) and accessibility to commercial appliance. Transition fault is tested a circuit is loaded by providing pattern initially and an additional pattern is given to employ the transition with a destination checkpoint terminal. Reaction could be examined at the outputs of Circuit-Under-Test (CUT). At-speed functional pattern approach can be replaced by the cost compelling Automatic-Test-Pattern-Generator (ATPG) which generates the scan based structural tests (Lin *et al*., 2003; Jayaram *et al*., 2003).

The accomplishment of a scan based transition error examination; a style combination V_1_V_2 is given to circuit under test. Design V_1 can be called because the initializing style and V_2 as the launch style. The signal transition (0-1 or even 1-0) with the desired node was launched by the V2. Additionally, it helps multiply the result transition towards output regarding circuit under test (scan flops or even initial yields). Your feedback regarding the circuit under test towards pattern V_2 must be secured at functional rate. Full procedure can be branched directly into 3 rounds Initialization Cycle (IC) where the circuit under test can be initialize into a precise condition (V_1 can be practiced), Launch Cycle (LC) where a transition is casted with the destination entrance terminal (V_2 can be practiced) as well as) Capture Cycle (CC) where transition can be generated as well as trapped at an observable notch. Different scan based transition fault screening scheme ended up proposed in literature (Savir, 1992; Savir and Patil, 1994; Dervisoglu and Stong, 1991). Based on how the actual transition can be launched as well as captured you will find trio transition fault style formation techniques are labelled as launch off shift, launch off capture as well as enhanced launch off capture (Fig. 2 and 3).

Literature review: Inside initial process is LOS (launch off shift), (Savir, 1992), transition at gate yield is presented at the last shift period throughout your shift operations. Figure 1a displays path involving transition introduction in launch off shift way for multiple-DFF pattern; identical method might be adapted a great level sensitive scan design. Transition is sent from your scan in port (SD) regarding any f-flops within the scan cycle. This triggers the desired transition in the destination gate terminal that is generated as well as secured from functional path from a visible mark (D) regarding a f-flop within the scan cycle. Figure 2b displays the waveforms in diverse series involving launch off shift functioning. LC can be part of shift functioning which was immediately accompanied by a quick get heart beat. You have a look at help (SEN) indication is large throughout the last shift as well as should head out low for you to get the result at the closed circuit clock edge. The period of time intended as SEN (scan enable signal) to produce the indicated 1and 0 transitions go along on the functional regularity. Thus launch off shift calls for SEN transmission facing become timing essential. Altering the clock (CLK) produces greater capture clk recurrence when compared with common shift clock recurrence. Saxena *et al*. (2002) listing additional launch off shift strategies. Figure 3a displays transition start journey in the 2nd technique, known as LOC (Savir and Patil, 1994) technique. Within

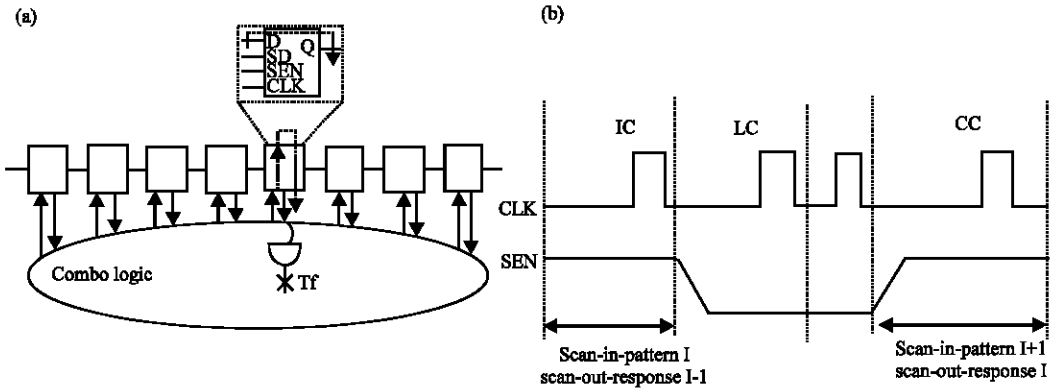

Fig. 2: a, b) LOS transition fault pattern

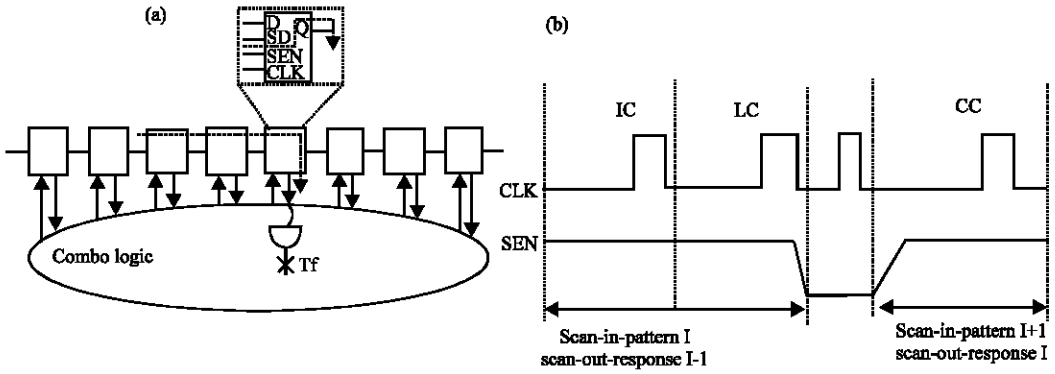

Fig. 3: a, b) LOC transition fault pattern

this technique, transition was introduced as well as grabbed as a result of the functional port (D) in any flip-flop from the have a look at chain. Due to the fact, the start pattern V_2 bets on functional result involving initialization vector V_1 the start path can much lesser governable over that your analysis out coverage is small. Figure 2b displays waveforms in launch off capture technique that launch cycle is severed in shift functioning. By the end involving scan-in (mode shift), pattern V_1 is utilized as well as circuit under test could set with an initialize state. This particular relaxes the at-speed constraint around the (Scan Enable) SEN indication as well as deceased series usually are extra after the past shift to produce the required time for that SEN indication to be in low. The next process, referred to as enhanced scan (Dervisoglu and Stong, 1991), needs a couple signals V_1 and V_2 which ware relocated into scan f-flops together. The major influence of mentioned technique will be which explains automatic test pattern generation and much improved coverage to the pair of LOC and LOS strategies because it gets rid of any reliance involving V_2 and V_1. Enhanced scan further possess advantageous have an effect on test data volume, due to the fact more compact test designs is usually generated. The particular disadvantage in enhanced scan will be which it wants hold-scan f-flops which are area-in-depth, ASIC designs are not attractive. Hold scan f-flops are used by the enhanced scans which are found at the process of field connected microprocessor with high realization which can be justified easily. LOS process is usually preferable coming from ATPG complication and also routine depend view points by comparing to LOC process. With circumstance regarding LOC, high fault coverage is not confirmed thanks towards link between a couple of designs, V_1 and also V_2. Because the design dimensions will increase the actual SEN fan-out is higher than any other net inside design. LOS demands sen to become time crucial making it problematic in order to put into action making use of inexpensive testers and also in types the spot that turnaround time is crucial (Ahmed *et al*., 2005). This is certainly deduction that LOC process has become broadly utilized, specifically in inexpensive testers (Jayaram *et al*., 2003). Be aware that absolutely at-speed SEN is essential intended to launch off capture process. Methods are appropriate to enhance launch off capture fault coverage. In view of this particular study all of us recommend an approach to boost this fault coverage along with slow up the design matter

by making use of an improved LOC technique. This smartly decides a subset connected with check cells to get handled simply by LOC technique and the relaxation since scan path. That boosts this controllability connected with check cells along with detects a number of tough to identify LOC faults. Many approaches are actually suggested to develop the particular launch off shift fault coverage however considerably effort is not yet to be done with particular launch off shift solution of most beneficial of our own information. Throughout Wang *et al.* (2004), any hybrid scan architecture will be proposed which usually handles a small subset connected with chosen scan cells are simply LOS along with sleep usually are governed by simply LOC tactic.

Timely scan enable sign generator is constructed and could usually push particular LOS governed scan flops. Actual ATPG technique employed will be difficult and current industrial resources will not assistance this kind of approach. Also the selection consideration in the launch off shift composed scan flops ascertains potency of strategy. Under some circumstances, sum of habits earned because of the hybrid technique surpasses the particular LOC pattern. The execution regarding LOS process using low priced testers is offered within (Ahmed *et al.*, 2005). A neighbourhood at-speed scan enable sign is generated having a slow enable sign achieved by means of economical checker. A neighbourhood scan enable generator is made it may be put any place in scan chain and also the launch as well as capture facts are usually summarized within check information as well as transported to the scan chain. The suggested process within (Ahmed *et al.*, 2005), concentrates simply about LOS and execution about low priced testers. The process doesn't have effect about fault coverage as well as pattern relies.

MATERIALS AND METHODS

Logic BIST architecture

General architecture: The Stated logic built in self test architecture is shown in the Fig. 1. It consists a TPG (Test Pattern Generator) which generates test patterns and a ATPG (Automatic Test Pattern Generation) for generating the patterns for testing the BIST ready core. For compacting test results an ORA (Output Response Analyzer) is used. Test clocks are generated from the functional or original clocks using the clock gating block this entire processes is controlled by the built in self test controller. The automatic test pattern generation patterns are compressed to increase the fault coverage during the production test. The self test activity is started by the start signal and ends by the finish signal and the results by the results signal. A TAP (test access port) controller is employed for controlling the internal states of the built in self test.

BIST-ready core: The scan designs of the circuit which obeys the all the rules of the scan design is the bist ready core. it may be needed the an extra circuit to avoid the disputes in the tri state buses and the set/reset signals and the false paths. Bist ready core consists of the circuit under test which is rule checked and it may also obeys the bist specific design rules which are the x-blocking.

TPG circuitry and ORA circuitry: In the TPG (Test Pattern Generation) and the ORA (Output Response Analyser) blocks which are shown in Fig. 1 are not properly managed and the TPG block consists of the PRPG (Pseudo random pattern generator) circuit which is constructed using the LFSR method. The LFSR can act as the PRPG which can generate the random test patterns and the ORA block consists of the MISR circuit and it could act as the response analyser for the BIST circuit.

Test control circuitry: The circuit of the test controller contains the clock gating block and the BIST controller. The BIST consist of the system clock which is divided into 2 clocks namely CK1, CK2 and these clocks are given to the clock gating block as the inputs and they are processed by the few buffers generating the outputs such as CCK1,CCK2 and these given to the TPG and the ORA blocks .the clock block is under control of BIST controller by using the test clocks namely TCK_1,TCK_2.the BIST controller is a circuit which coordinate with the test and debug the tasks and it is a test access port (TAP) controller.

Enhanced launch-off-capture: The functional reaction of circuit is to kick off transition at targeted gate terminal and it is propagating the fault impact with an noticeable point by the LOC method. There are many controllability difficulties because of the transition launch through functional response. We now explain the controllability of LOC along with summarize how a LOC's test coverage can be enhanced through growing it is controllability. Figure 4 a exhibits a compact case having 2 have a look at scan chains, SC1 along with SC2, every single composing of 2 have a scan cells. Scan-in slots are usually SI_1 along with SI_2 plus the scan-out slots are usually SO_1 along with SO_2, proportionately. In unique case, 2 have a look at scan chains have got separate have a look at help alerts SEN1 along with SEN2, respectively. Point Y (Fig. 4 a is mainly focused due to the slow rise and fall of the transition is occurred. Launch off capture is occupied with fault detecting movement of 0-1 move; scan operations with

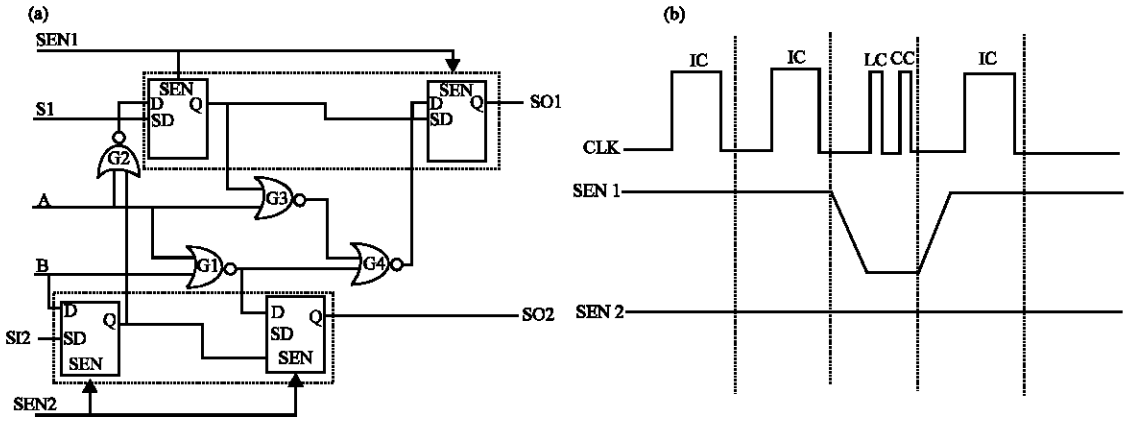

Fig. 4: Enhanced launch off capture method: a) circuit diagram and b) wave forms

shift have the logic 0 by actual scan cell SC22. Gate G1 is involved in the productivity of logic 1 from a circuit which launches the 0-1 transition at point Y. ability to generate the transition, involves 4th gate for other suggestions then the actual once to Y point where non-controlling value with production of 1st Gate (G1) which obstructs the actual generation of move at an detectable stage. Therefore, the actual slow-to-rise transition fault in aiming point Y simply can be no testable by the conventional launch off capture method.

The particular scan enable signals tend to be large through the move operations and also small through the launch and also capture course (Fig. 4b). Sometimes, actual controllability can be improved through the use of the actual scan path as opposed to the functional path. Figure 4a displays the identical instance where the slow to rise transition fault in point Y simply, employing typical LOC method, can be deductible by means of preventing the actual launch path of focus on transition fault employing the actual scan enable signals. The particular 0-1 transition in Y simply can be presented throughout the scan path as opposed to the functional procedure. Residual inputs of gate G4 other than the prospective fault point Y simply tend to be manageable for you non-regulating value 0 for you to propagate actual transition. Current scheme is called ELOC (Enhanced Launch Off-Capture), Fig. 4b displays actual scan enable signals SEN_1 and also SEN_2 through the shift (IC), launch (LC) and also capture (CC) cycle. here actual scan make it possible for indicate of the minute scan chain SEN2 can be stored continual in 1 while in each start and also capture course. Basically, the actual scan chain SC2 is used and then shift portions. It operates being a shift register and also isn't going to capture virtually any practical reply of circuit.

Typical (Launch off Capture) LOC method could consider exceptional ailment of the enhanced LOC (ELOC) method, in which the scan enable signals of all so-called stores tend to be 0 through the launch and also capture course. ELOC offers extra controllability involving starting actual shift possibly throughout the scan trail or actual functional trail. Note, actual Scan Enable (SEN) signals tend not to alter involving the launch and also capture course and also virtually any scan enable transition are at shift regularity. Figure 5 displays some sort of circuit using a couple scan chains, one alternate to be shift register as well as some alternative inside the actual functional approach. Particular changes from primary scan chain tend to be presented throughout the functional path while transitions from the second scan chain tend to be presented from your scan path.

RESULTS AND DISCUSSION

Local scan enable signal generation: Particular enhanced launch off capture procedure offers extra controllability in order to launch any transition. A number of SEN ports may be used nevertheless this increases many pins. The particular scan enable control details for all you have a scan chains differ simply in the launch in addition to capture cycle with the pattern. For this reason this have a scan enable indication in the outer tester works extremely well to the scan shift function plus the scan enable control details intended for simply this launch in addition to capture course is usually made inside. The scan enable generator cells usually are introduced inside the scan chains. Therefore, this control details will be approved within the analyze information. The particular scan control details may be part of every single analyze pattern and it is located inside the tester's recollection (Fig 5a-c).

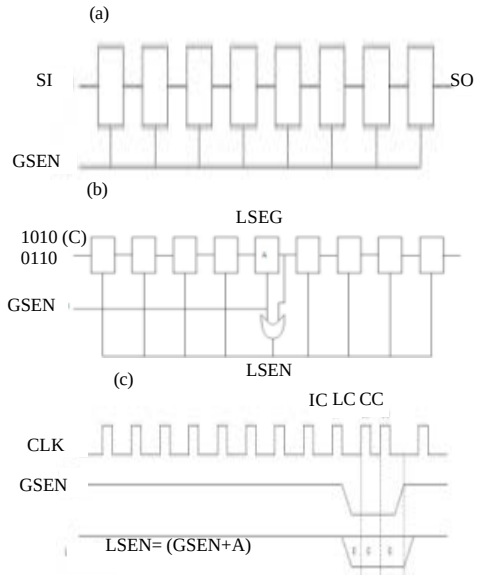

Fig. 5: a) Scan chain; b) LSEN generation and c) LSEN generation process

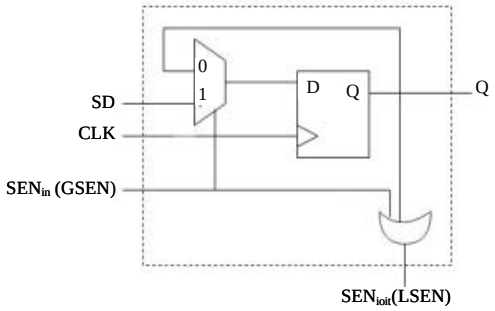

Fig. 6: LSEG cell

The regular scan structure with scan enable sign from outside checker can be displayed in Fig. 6. You will discover 8 scan f-flops from scan chain and evaluation pattern shifted can be 11100110. This outside scan enable sign from checker can be known as actual global scan enables. Figure 5 b demonstrates a similar signal when a local scan enable sign can be earned from test pattern information to the ELOC approach. This inside developed scan enable sign can be referred to as LSEN (Local Scan Enable). Key is always to deserted global scan enable signal following your shift function and develop actual LSEN sign over launch along with capture cycle from evaluation information.

Within this case, actual pattern shifted can be improved for you to 1010[C] 0110, exactly where C may be the search within permit manage tad and that is stored with search within f-flop A new at conclusion from scan function. Single particular added scan f-flop (A) in addition to an OR gate generally combined in with regard to the generation of LSEN sign. The result can be using global scan enable to build actual LSEN sign (Fig. 5b). Note GSEN just isn't an at speed sign. The GSEN sign asynchronously regulates the shift operations. The valuations on the scan f-flops throughout several shift cycles generally demonstrated below individual and every f-flop. GSEN can be deserted following your n^{th} shift routine n can be range of scan sequence later by implanting brand-new cell A. Towards end on the capture routine, the actual LSEN sign can be asynchronously collection to 1 by simply GSEN with regard to scan out actual answer. Figure 5c demonstrates actual accurate process of switching the actual test style to the have a look at sequence as well as the timing waveforms. In general:

$$LSEN = (GSEN + A) = \begin{cases} 1 \text{ if } GSEN = 1 \\ A \text{ if } GSEN = 0 \end{cases}$$

Table 1: LSEG cell performance

GSEN	FF	LESEN	Operation
1	X	1	Shift
0	1	1	Shift-launch
0	0	0	funcational-launch

Local Scan Enable Generator (LSEG): As told previously, through capture course as well as launch of pattern, guidance bit changed directly to scan f-flop A can be used because scan enable control. The LSEG cell structure is displayed in Fig. 6. Launch as well as capture course are used to control essential info. The port description is compared to new scan cell and productivity of f-flop raised on time for the functional feedback port of the use flop. That is made up of the SEN in (scan in) pin which catches GSEN indicate because feedback. An extra scan-out (SEN-out) pin (GSEN -Q) serve as the LSEN sign. For that reason, immediately after going to a new manage talk about (C) in the conclusion of the adjust procedure (GSEN is de-asserted), LSEN stays within this talk about so long as it's asynchronously established to at least 1 simply by GSEN. Table 1 displays different modes of procedure of LSEG cell.

LSEG cell procedure: Scan chain is infused with LSEG cell which is shown in Fig. 7. LSEG f-flop with weighted value is symbolized by test pattern with C (1110(C) 0110). Timing wave form and the pattern of regular LOC approach is shown in Fig. 8a GSEN (SEN in) sign is de-asserted towards end with shift transaction. Particular LSEN (SEN out) sign can be earned through the boolean equation SENout=Q_FF1+ SENin. Your GSEN signal is usually high in the course of the full shift

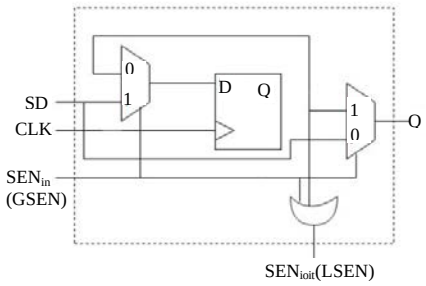

Fig. 7: Modified LSEG cell

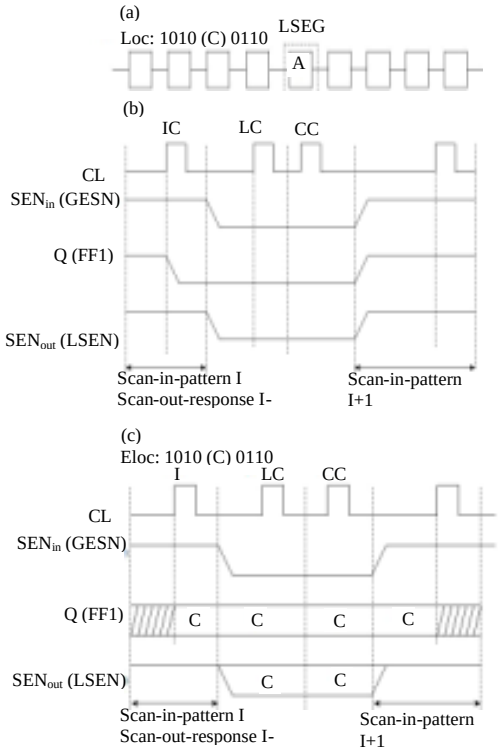

Fig. 8: Operation of local signal enable generator cell: a) Scan chain; b) General launch off capture; c) Enhanced launch off capture

procedure. By the end in the shift procedure, the actual GSEN sign is usually asynchronously deserted and LSEN sign must be logic 0. For this reason, actual LSEG cell f-flop must be confined in order to 0 in course of ATPG. Later capture course, actual LSEN signal is usually asynchronously proclaimed returning with simply GSEN (Fig. 8a-c).

For enhanced LOC a lot like conventional LOC this GSEN sign can be high over the total shift operations. At end with shift operations this LSEN sign is determined by this control part (C) transferred in to the LSEG cell f-flop over pattern shift. Enhanced launch off capture with

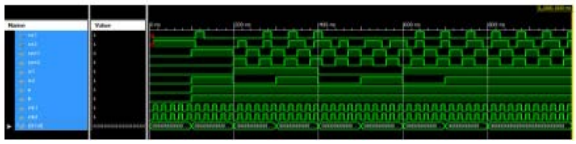

Fig. 9: ELOC result

Fig. 10: Scan enables cell result

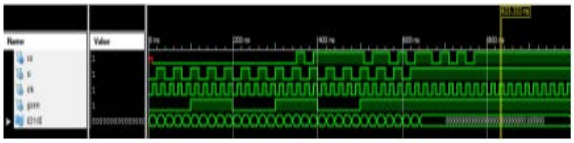

Fig. 11: Scan chain result

Table 2: ATPG results

Variables	LOC	Enhanced LOC	LOS
Detected faults	275843	284456	280216
Test coverage	87.34	90.67	91.30
Fault coverage	88.09	89.96	91.11
Pattern count	2254	2124	1214
CPU time (sec)	784.84	912.64	341.20

timing waveform along with pattern is shown in Fig. 8c. Your LSEN sign can be frequent with logic value of C over the launch in addition to capture cycle. It may be realized that this LSEN transitions are not at-speed. Following capture course this LSEN can be declared to asynchronously through GSEN.

Experimental results: LSEG cell can be placed in each of scan chain of all the bist designs. The (Dpatt) column is formed for thee max fault coverage obtained by Launch off capture approach. Controllability of the enhanced launch off capture approach which creates minute patterns at the transition is increased:

$$\Delta Part = \left\{\frac{LOC - ELOC}{LOC}\right\} FC_{LOC\,max}$$

Fine fault coverage is provided by the LSEG based result and the scan path is easily controlled by the LSEG cell for the pattern count And ATPG results are shown in (Table 2). The enhanced launch off capture gains the higher fault coverage when compared to the general LOC method. Here, the experiment is done by using the Xilinx ise design and the verilog programming method and the results are shown below in the Fig. 9-11.

CONCLUSION

The presented study is on the BIST designs for testing the new method called the enhanced launch off capture method for finding the transition faults. This method can actually best at the controllability when compared the general launch off capture method. Fault coverage and pattern count are very less in the LOC method and launch off shift technique is not used in the designs because of the SEN signal. BIST architecture is used in this study in order to find the better transition fault in the BIST designs and for the better transition fault coverage we opted the ELOC method then the loc method. By this method better control over the transition path can be achieved by generating the LSEN's. These signals are generated by a special cell known as LSEG cell and it is very easy to design which is better than the scan flop. High controllably and high accessibility over the transition fault pattern generation can be achieved by the LSEG cell. Diagnosis and the debugging can be done by the BIST architecture for locating the BIST failures. But still much more work has to done in order to increases the transition fault coverage in the BIST designs for higher acceptance and to find the BIST failures accurately during the debug and diagnosis

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