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Comparison of Modified Russian Peasant Multiplier based 12-Tap FIR Filter and Multiplierless 12-Tap FIR Filter

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Abstract: Digital FIR filter plays a significant role in today's world of communication and computation. FIR filter is used in digital signal processing applications because of its stability, linear phase, low cost and simple structure. In MAC unit, both multiplication and accumulation functions are involved but the performances of MAC unit is mostly depends on dataflow structure of accumulation unit. Russian Peasant Multiplication (RPM) is the best multiplication algorithm which is based on "Multiply-divide" principle. In this study, multiplierless 12-tap FIR filter with and without optimized coefficients are compared with modified Russian Peasant Multiplier using 12-tap FIR filter in terms of area. The result analysis shows that proposed MRPM using MCSLA based 12-tap FIR filters are better than multiplierless 12-tap low pass FIR filter.

Key words: Modified Russian Peasant Multiplier (MRPM), Finite Impulse Response (FIR), Multiplication and Accumulation (MAC) unit, functions, optimized, coefficients

INTRODUCTION

In a digital signal processing system, the Finite Impulse Response (FIR) filter is one of the most essential elements and it can assure a strict linear phase frequency characteristic with any type of amplitude frequency characteristic. Digital Signal Processors (DSPs) integrate a multiplication unit to execute algorithms such as filtering and convolution. Digital filters process is digitized or sampled signals. A digital filter determines a quantized time-domain representation of the convolution of sampled input time function and a representation of the weighting function of the filter. They are recognized by an extended sequence of multiplications and additions carried out at a uniformly spaced sample interval. It is used to execute mathematical operations on sampled and discrete time signals to enhance a certain aspect of the signals.

Adders are used in the arithmetic logic unit and also used in several types of processors. And it is used to determine table indicates addresses and related applications. Multiply-Accumulate (MAC) structures is one of the important adders in several applications. In multipliers, adders are also used. High speed integrated circuits and in digital signal processing to execute various algorithms like fast fourier transform, finite impulse response and infinite impulse response. In current, design of area efficient and high speed data path logic systems are the most important areas in the research of VLSI design. The main factors in the digital signal processing are area and speed. Fundamentally, area power and speed are interconnected factors. It means that a change in one of the factor may affect the others. In this research, we have given more priority to the area consumption. The circuit considered is of an adder in this research. One of the fastest adders is the carry select adder.

Multiplication and Accumulation (MAC) unit plays an important role in every digital signal processing operations. Three main operations involved in MAC functions are to find the multiplication results such as Partial Product Generation (PPG), Wallace tree reduction and Partial Product Addition (PPA). These have been designed by using Russian Peasant Multiplier (RPM). Carry Select Adder (CSLA) is used in the design for performing addition operation of MAC unit. In this study, the modified Russian Peasant Multiplier using CSLA based 12-tap FIR filter has been designed to reduce the area, power and delay consumption. Proposed modified Russian Peasant Multiplier using SQRTCSLA based 12-tap FIR filter gives better performance than the multiplierless 12-tap FIR filter.

Literature review: Gowrishankar *et al.* (2013) described the design of FIR filter. Multiplier unit is completed using XOR-XNOR column by column reduction compressors using full adder. Multiple pairs of Ripple Carry Adders (RCA) are used in CSLA structure. Carry select adder equally divides the word size of the adder into blocks of 4 bit each. FIR filter is designed to increase the speed of addition and decrease the power taken by the multiplier unit. The carry propagation delay and area of carry select adder is decreased by splitting carry select adder into equal bit groups.

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Patel and Mohanty (2014) explained the CS operation is scheduled before the computation of final-sum which is different from the traditional approach. Carry words identical to input-carry '0' and '1' generated by the CSLA based on specific bit pattern which is used for logic optimization of the CS unit. For logic optimization, fixed input bits of the CG unit are also used. An optimized design for CS and CG units are obtained. An efficient design is obtained for the CSLA by using these optimized logic units. CSLA design involves less area and delaying the BEC based CSLA (Patil *et al*., 2015).

Kadam *et al.* (2015) presented the parallel and pipeline processing architectures of FIR filter for efficient FPGA implementation. This structure shows 25% improvement in area. The parallel processing architecture shows 20% improvement in frequency of operation. To increased the sample rate, reduced area and improved speed in the FPGA implementation of FIR filter.

Thingom and Khundrakpam (2016) explained the design of FIR filter. By using Radix-2^r recoding technique, the filter coefficients have been recoded. The purpose of multiplier less technique based on Radix-2^r results in enhanced resource utilization over implementation using generic multipliers. It also reduces the power consumption.

Low-power and area-efficiency carry select adder has been explained by Ramkumar and Kittur (2012). In this study, method of sharing the common resources is used to reduce the area and power of SQRT CSLA architecture. The number of gates is reduced in this research.The great advantage is the reduction of area and power consumption. Wallace (1964) suggested for a fast multiplier, that design is used for a multiplier which generates the product of two numbers using combinational logic. The equipment cost is almost halved and the multiplication time almost doubled. Reciprocal times would not be affected, half-sized adder tree would be large enough to do in one step the largest multiplication required in the repetition.

Waters and Swartzlander (2010) explained changes to the second phase reduction used in Wallace multipliers. The modified Wallace tree reduction should be decreases the number of half adders needed by atleast 80% compared to the traditional Wallace tree reduction with slight increase in the number of full adders. Dangra and Gawande (2016) presented the multiplierless FIR filter which is used to reduce the hardware cost by minimizing the number of sign power of two terms in filter coefficient. In the multiplierless FIR filter with and without optimized coefficients (Dangra and Gawande, 2016) and their performances are taken and compared with our proposed method in terms of area and power consumption. When compared with this reference (Dangra and Gawande, 2016) the proposed method gives better performances in terms of area consumption.

MATERIALS AND METHODS

Multiplierless FIR filter: The shift-adds design of FIR filter can be realized not only by sharing the common sub expressions with the constant multiplications but also by sharing of previous values of the filter input. Although, the number of operations can be decreased slightly, the number of registers may be increased extensively. The multiplications of filter coefficients (Dangra and Gawande, 2016) by the latest N filter input values and their summations are regarded as a constant array vector multiplication operation where these latest N filter input values are assumed as CAVM operation of input variable and the CAVM operation of output is the filter output. The number of CAVM operation inputs is equal to [N/2] and the number of adders outside the CAVM operation is equal to [N/2] which is due to the odd or even number of filter coefficients. These adders always create an output with a bit width equal to the bitwidth of the filter input plus 1. Then the filter is explained including the CAVM operation as well as the necessary circuit consisting of registers and adders outside the CAVM operation if the filter is symmetric.

The fundamental operations in digital signal processing are addition, multiplication and delay. Multiplier element is very costly in terms of area in hardware implementation. FIR filter consists of two ways. The implementation of N = 4 FIR filter with multiplier and multiplierless structure shown in Fig. 1 and 2.

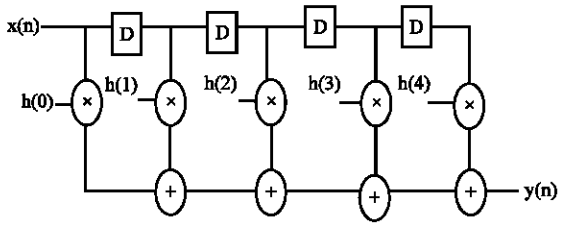

Fig. 1: Direct form of multiplier FIR filter

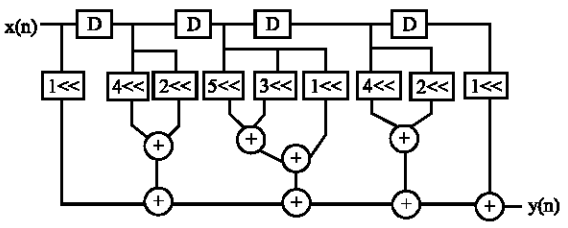

Fig. 2: Direct form of multiplierless FIR filter

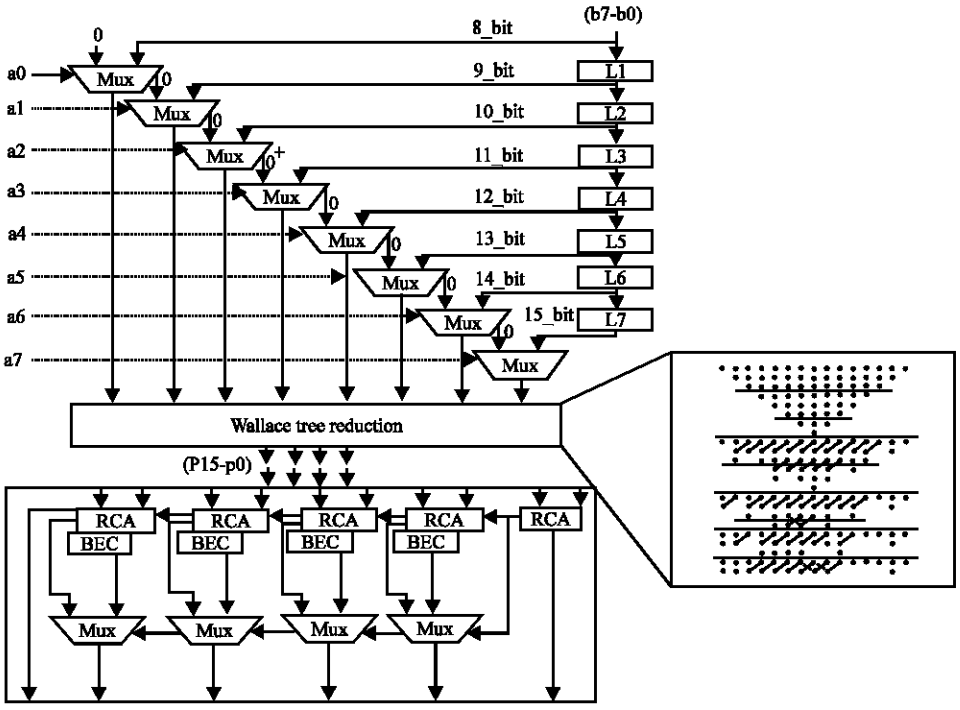

Fig. 3: Structure of modified digital Russian Peasant Multiplier

To reduce the area either by sharing the multipliers or by operating the coefficients so as to reduce the number of multiplications in the implementation of multiplier FIR filter where as in multiplierless FIR filter implementation, coefficients are transformed to other numeric representations whose hardware implementation is more capable than the traditional binary representation. The coefficients are represented by a combination of Power of Two (POT) terms in such a way that multiplication can be implemented simply by adder and shifter (Tyagi, 1993; Prasad *et al*., 2016).

Modified Russian Peasant Multiplier: Russian Peasant Multiplication (RPM) is an important and fast method to multiply the two 'n' bit multiplication. Russian Peasant Multiplier based on multiplying and dividing by two. Russian Peasant Multiplier consists of shifters, 2:1 multiplexer and adder unit.

Russian Peasant Multiplication (RPM) which is based on "Multiply-divide" principle, right shifters and left shifters are used to multiply and divide 'n' bit binary data. Hence, shifters based digital circuit is to perform the multiplication operation by using Russian Peasant Multiplication algorithm (Aksoy *et al*., 2014). The structure of MDRPM has been illustrated in Fig. 3. Only one shifter is used to provide the PPG results in DRPM to re-schedule the PPG results, Reduced Wallace Tree Generation (RWTG) pattern has been developed. In final stage of RWTG, an efficient accumulation structure is essential for implementing 'n' bit addition operation. The reduced Wallace tree multiplier architecture uses a combination of 5-2, 3-2, 4-2 compressors and half adders in four different stages of partial product products reduction step. Finally, the 16 bit MSQRTCSLA adder has been used to add two 'n' bit binary data.

The sums obtained from the series of compressors and a half adder in the first stage is linearly fed to the compressors or half adders of the next stage. The carry bits generated from the first stage columns are propagated to the next following column of next stage.

Similarly, the sum bits from the further stages are fed to the compressors in the column of subsequent stage similar to the previous while carry bits are propagated to the consequent column, respectively of the next stage in the sequence. The design of MSQRTCSLA has been incorporated into DRPM multiplier. Hence, proposed multiplier architecture is named as Modified Digital Russian Peasant Multiplier (MRPM or MDRPM).

Proposed 12-Tap fIR filter based on MRPM using MSQRTCSLA: In proposed design, 12-tap Direct Form Finite Impulse Response (DF-FIR) filter has been designed with the help of modified digital Russian

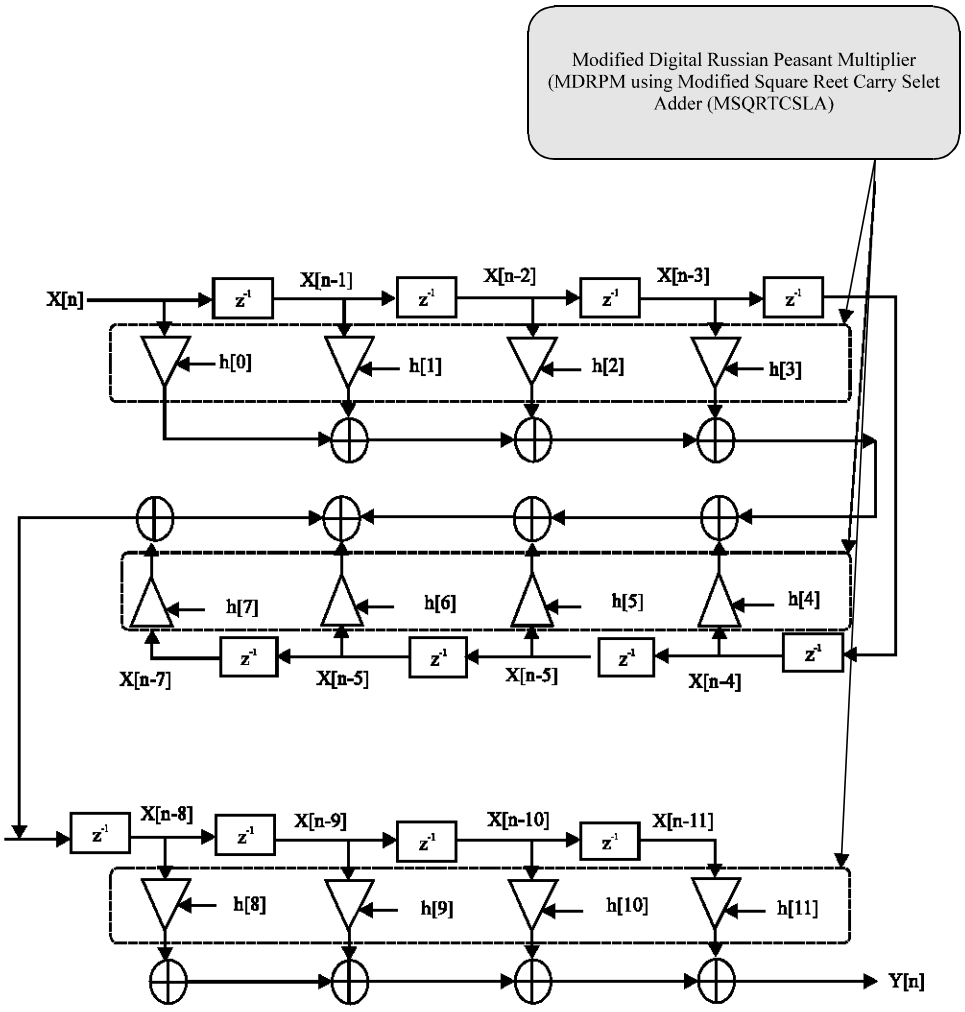

Fig. 4: Architecture of proposed 12-tap FIR filter based on MDRPM using MSQRTCSLA

Peasant Multiplier using MSQRTCSLA accumulation structure. The architecture of proposed MDRPM using MSQRTCSLA based 12-tap FIR filter has been illustrated in Fig. 4.

As shown in Fig. 4, 12-tap FIR filter uses 12 MAC units to find the permitting and blocking frequency path. The z-1 indicates the delay elements, X[n-k] indicates the delayed version of input samples, h[1, 2, 3, ..., n] indicates filter coefficients and Y[n] indicates the output sample. The dotted line of Fig. 4 indicates the incorporation of proposed MAC unit into direct form FIR filter.

RESULTS AND DISCUSSION

Synthesis result of proposed modified Russian Peasant Multiplier using MCSLA based 12-tap FIR filter has been evaluated by using Xilinx 10.1 ISE (Family: Spartan 3, Device: XC3S50, Package: PQ208, Speed: -5).

Figure 5-7 show the synthesis result of proposed MRPM based CSLA to determine the area, delay and power consumption.

When compared to optimized and unoptimized with multiplier based 12-tap FIR filter (Dangra and Gawande, 2016) optimized and unoptimized with multiplierless based 12-tap FIR filter the proposed MRPM using MSQRTCSLA gives better performance. Performance evaluation of modified Russian Peasant Multiplier based 12-Tap FIR filter and multiplierless 12-tap FIR filter is shown in Fig. 7 and 8.

From Table 1, it is clear that proposed MRPM using MSQRTCSLA based 12-tap FIR filter offers 90.5% reduction in no of occupied slices, 95.8% reduction in No. of 4 input LUTs, 90% reduction in No. of slice flip-flops, 91.3% reduction in power than the unoptimized with multiplier based 12-tap FIR filter. The proposed method offers 80.6% reduction in No. of occupied slices, 90%

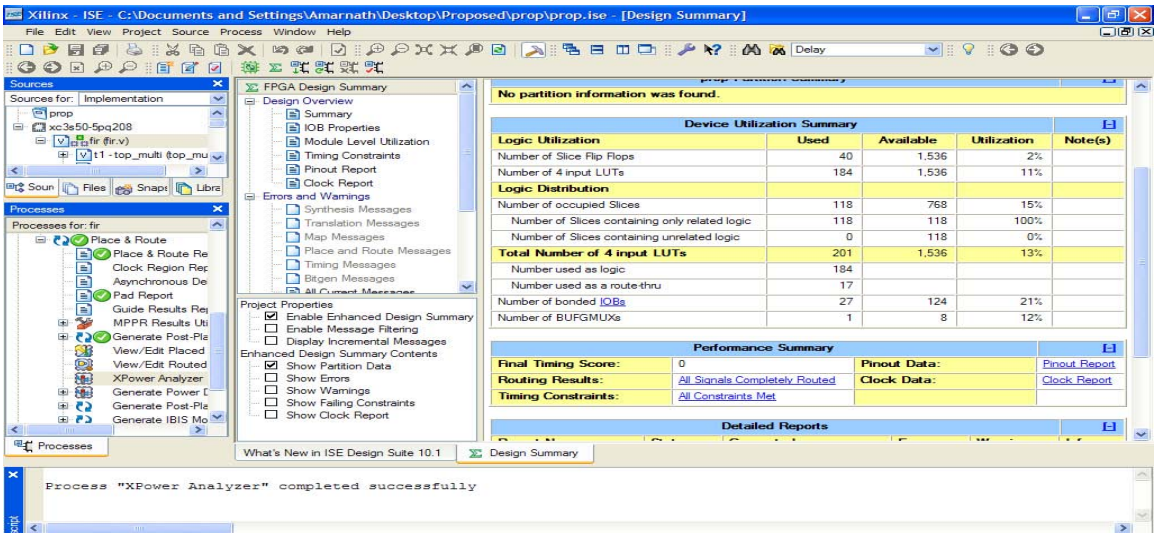

Fig. 5: Synthesis result of proposed MRPM using MCSLA based 12-tap FIR filter to determine the area

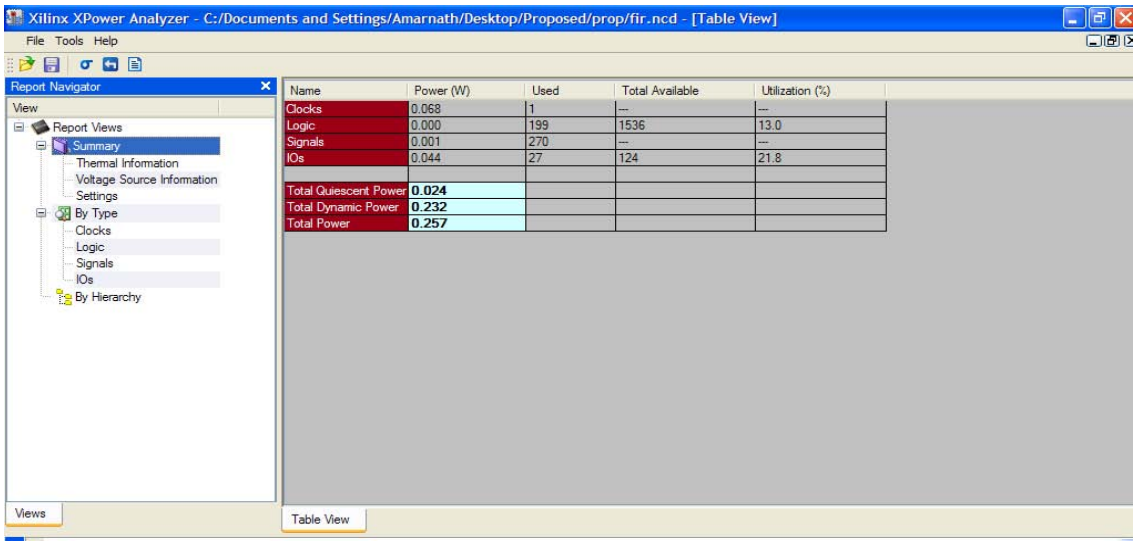

Fig. 6: Synthesis result of proposed MRPM using MCSLA based 12-tap FIR filter to determine the power

Table 1: Comparison analysis of optimized and unoptimized with multiplier based 12-tap FIR filter, optimized and unoptimized with multiplierless based 12-tap FIR filter (Dangra and Gawande, 2016), proposed MRPM using MSQRTCSLA based 12-tap FIR filter

Parameters	Unoptimized with multiplier (Dangra and Gawande, 2016)	Optimized with multiplier (Dangra and Gawande, 2016)	Unoptimized with multiplierless (Dangra and Gawande, 2016)	Optimized with multiplierless (Dangra and Gawande, 2016)	Proposed method based 12-tap FIR filter
No. of occupied slices	1251	611	695	221	118
No. of 4 input LUTs	4480	1850	2146	773	184
No. of slice flip flops	400	400	192	192	40
Power (W)	2.978	0.177	0.182	0.176	0.257

reduction in No. of 4 input LUTs, 90% reduction in No. of slice flip-flops, 31.1% increased in power than the optimized with multiplier based 12-tap FIR filter. The proposed MRPM using MSQRTCSLA based 12-tap FIR filter offers 83.02% reduction in No. of occupied slices, 91.4% reduction in No. of 4 input LUTs, 79.1% reduction in No. of slice flip-flops, 29.1% reduction in power than the unoptimized with multiplierless based 12-tap FIR filter.

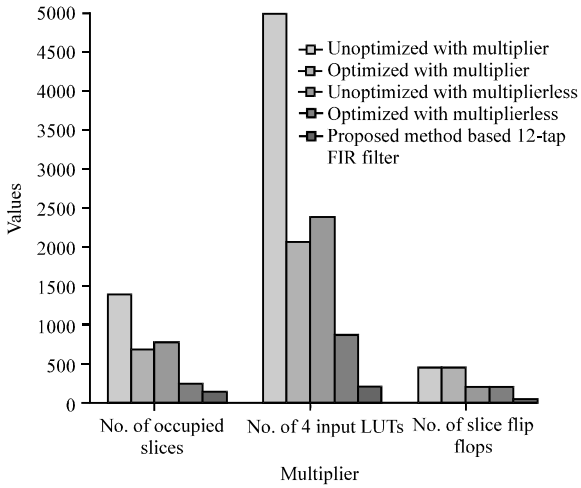

Fig. 7: Performance evaluation of modified Russian Peasant Multiplier based 12-tap FIR filter and multiplierless 12-tap FIR filter

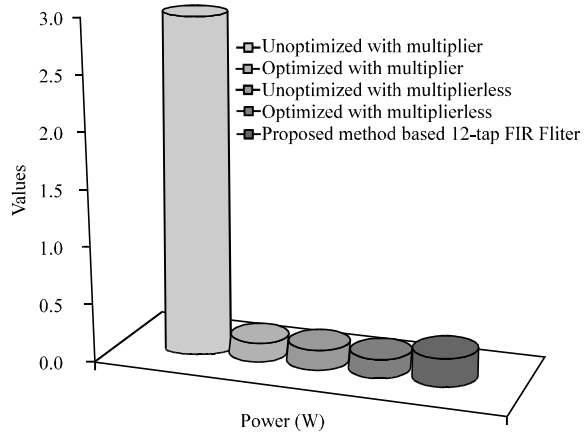

Fig. 8: Power comparison of modified Russian Peasant Multiplier based 12-tap FIR filter and multiplier less 12-tap FIR filter

The proposed MRPM using MSQRTCSLA based 12-tap FIR filter offers 46.6% reduction in no of occupied slices, 76.1% reduction in no of 4 input LUTs, 79.1% reduction in No. of slice flip-flops, 31.5% reduction in power than the optimized with multiplierless based 12-tap FIR filter.

CONCLUSION

In this study, comparison analysis of proposed modified Russian peasant multiplier using modified SQRT carry select adder and multiplierless based 12-tap FIR filter in terms of area and power consumption. Many electronic applications are required carry select adder of higher number of bits which helps their process very faster. The delay is reduced to a great extent with the modified RPM. Thus, the results shows that using modified method the area will decrease thus leads to good alternative implementation for many processors. The proposed method is very efficient in terms of area than the multiplierless based 12-tap FIR filter. The proposed MRPM using MSQRTCSLA based 12-tap FIR filter gives better performances than the multiplierless 12-tap FIR filter (Dangra and Gawande, 2016).

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