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Design of Novel Square Root Carry Select Adder (SQRT-CSLA) for Digital Fir Filter

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Abstract: In this study, an efficient adder for reducing the delay of the circuit is designed. Here, designed a modified SQRT-CSLA for high speed applications. BEC overcome the carry propagation delay of the CSLA adder and also it takes small number of gates to implement the design. In the circuit Ripple Carry Adder (RCA) is changed to BEC for achieving the efficiency the design is done by using verilogHDL and verifies the simulation results by ModelSim 6.3c. Finally the designed adder is compared with conventional carry select adder for differentiate the adder performance. The designed adder is applied into the FIR filter for high speed application.

Key words: BEC, RCA, SQRT-CSLA, ModelSim, application, India

INTRODUCTION

Digital filters are used to sampling the signals. They are recognized by an extended sequence of multiplications and additions carried out at a uniformly spaced sample interval. The sampled discrete time signal is used to find the mathematical operation of the signals is presented in (Abeysekera *et al*., 2003). A High performance digital FIR filters are similar to the analog passive filter. The digital filter consists of an analog to digital converter block to convert the analog form of signal to digital form of signal. To perform the numerical operations on the sampled data, digital signal processors are used. This processor is used in general purpose processor such as PC or a microprocessor or a DSP chip is discussed in AlJuffri *et al.* (2015). Field Programmable Gate Array (FPGA) is used instead general purpose processor or specialized DSP with specific parallel architecture for performing operations such as filtering, in high performance applications. It carries the numerical calculations on sampled data is approached by Anandi *et al.* (2013). These calculations involve input values are multiply by constants and the product values are added together. Memories are used to store the data. Finally, a digital to analog converter block is used to convert the processed digital signal to corresponding analog signal.

In digital signal processing, Finite Impulse Response (FIR) filter are known as non-recursive digital filter. The term digital filter arises because this filter operates on discrete-time signals are explained by Bakalis *et al.* (2000). They do not have the feedback for filter operation; hence, it is called as a non-recursive digital filter. Even though recursive algorithm can be used for filter realization.

Adders and multipliers are used to provide efficient FIR filter implementation. The modifications in adders and multipliers provide the same functionality with improving efficiency in various aspects.

An efficient approach for the removal of bipolar impulse noise using median filter is discussed by Kadali and Rajaji (2015). Energy efficient voltage conversion range of multiple level shifter design in multi voltage domain. Level shifter is inserted between two modules when low voltage drives high voltage modules. Multi supply voltage is used to reduce the static and dynamic power consumption is described by Sinthuja (2014).

Literature review: Wey explained an area-efficient carry select adder by sharing the common Boolean logic term; they can remove the duplicate adder cells in the carry select adder. In this manner, the transistor count in a 32 bit carry select adder can be greatly decreased from 1947-960. Moreover, the power consumption can be decreased from 1.26-0.37 mw as well as power delay product decreased from 2.14-1.28 mw(*NS). After logic simplification and sharing partial circuit, need one XOR gate and one inverter gate in each summation operation as well as one AND gate and one inverter gate in each carry-out operation.

Manju described an efficient carry select adder by sharing the Common Boolean Logic (CLB) term. In this study, after logic simplification they need one OR gate and one inverter gate for carry and summation operation. The normal SQRT CSLA has the disadvantage of more power consumptions and occupying more chip p-0 area. A regular CSLA used two copies of the carry evaluation blocks, one with block carry input is zero and other one

with block carry input is one. The modified SQRT CSLA reduces the area and power when compared to regular CSLA with increase in latency by the use of binary to excess-1 converter.

Mohanty briefly explained and analyzed the logic operations involved in the conventional and BEC-based CSLAs to studied data dependence and to identified redundant logic operations. The BEC based CSLA adder reduces the propagation delay because it contains only BEC based adder. The BEC unit completely reduces the propagation delay of the circuit. Based on the Cin input the operation strarts and perform the actions in proper.

MATERIALS AND METHODS

Proposed adder design: In general the Carry Select Adder (CSLA) is used to get a fast and efficient output. The efficient adder is used for data processing. CSLA is called an efficient adder because of less delay and reduced size. First of all they used a high speed compact CSLA as half of the adder in each block, then a Block Carry Generator (BCG) circuit is used for faster carry propagation and at last we interchanged multiplexer gate with a XNOR gate. The modified SQRT-CSLA is designed for low area utilization. Because it contain less number of RCA adders. The main goal of the SQRT-CSLA is used to reduce the carry propagation delay by separately execute and then select a carry to generate the sum '0' or sum'1'.

The structure of 16 bit traditional BEC based SQRT CSLA is shown in Fig. 1. The input signal is divided into 5 Groups and each group can be executed in a parallel manner. Each and every group has RCA and BEC pairs for Cin = 0 and Cin = 1. It provides partial sum and carry results. Finally, multiplexer circuits are used to evaluate the final sum results. Every group structures have FAs, HAs, Basic logic gates and Multiplexers for compute the final sum results. For instance, Group 2 and 3 structures for 16 bit traditional BEC based SQRT CSLA.

RESULTS AND DISCUSSION

Proposed modified SQRT-CSLA design in Fig. 1 is simulated by using ModelSim 6.3c simulation environment. The simulated output is shown in Fig. 2.

After the completion of simulation, performance of the proposed SQRT-CSLA adder is analyzed by using Xilinx 10.1 ISE simulation environment. Evaluated results shown in Table 1 and Fig. 3.

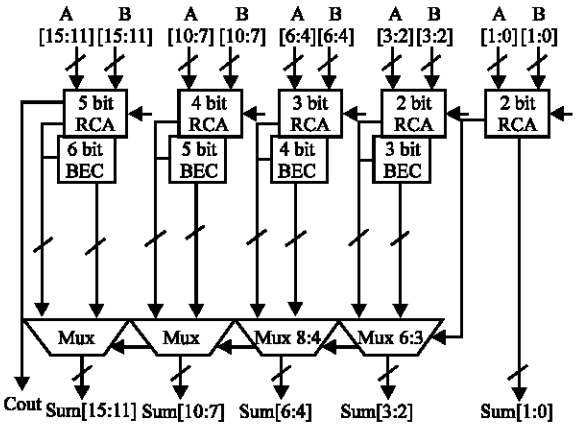

Fig. 1: Modified SQRT-CSLA using BEC

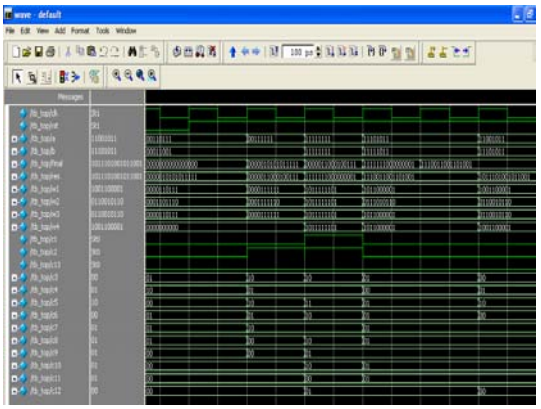

Fig. 2: Simulation output of modified SQRT-CSLA

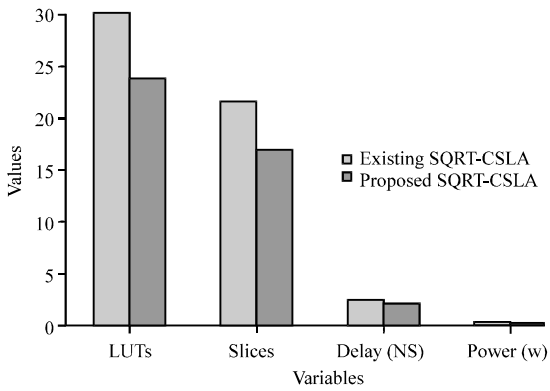

Fig. 3: Graphical representation of existing and proposed SQRT-CSLA

Table 1: Comparison of existing and proposed SQRT-CSLA

Parameters	Existing SQRT-CSLA	Proposed SQRT-CSLA
LUTs	25	20
Slices	18	14
Delay (NS)	2.023	1.87
Power (W)	0.278	0.231

CONCLUSION

Modified SQRT-CSLA using BEC was designed for low power and high speed applications. The designed adder is applied into the FIR filter, to get an efficient MAC unit. The proposed design reduced 20% of LUT and slices counts. Delay reduced upto 7.5%, similarly 17% of power is reduced in the proposed square root carry select adder using BEC. The complete design was simulated by using verilog HDL language with ModelSim simulation tool. The analysis results taken from Xilinx ISE tool.

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