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Minimum Number of Logical Elements Used Encoder/Decoder Technique for Wireless Communication Systems

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Abstract: Orthogonal Frequency Division Multiplexing (OFDM) based wireless communication system has source encoder and source decoder and channel encoder and channel decoder. Source encoder and source decoder is used to convert the analog signal into digital signal and digital to analog signal, respectively. The main advantages of channel encoding a channel decoding are detecting and correcting a single error as well as detecting more double and triple adjacent errors. To fulfill the OFDM requirement, different types of encoding and decoding techniques such as hamming, Cyclic Redundancy Check (CRC), Low-Density Power Check (LDPC) and some other linear codes are used. In the part of encoding technique, parity bits are added to detect and correct a single error. Similarly, in the decoder side, single bit errors are detected and corrected successfully. In convolutional encoding technique, single bit data is converted into second-bit data sequentially. To detect the data output, convolutional encoder is implemented in this research.

Key words: Ortho gonal frequency division multiplexing, encoder, decoder, cyclic redundancy check, low-density power check, adaptive white Gaussian noise

INTRODUCTION

Error detection and correction mechnaishms: Error detection and correction codes provide reliable delivery of information signals. In every hardware system, the small size of transistors and capacitors are combined with radiation effects from cosmic rays. Hence these cause occasional errors in a large storage of information A survey on FFT processors is discussed by Angeline and Ponraj (2013). In general, these types of errors are generated in RAM chips [Error detection] SRAM interleaving distance selection with a soft error failure model is discussed by Baeg *et al.* (2009). These errors can be detected and corrected by employing the error-detecting and error-correcting codes in RAMs. The most generalized scheme for detecting the error in error detecting technique is parity bit modified hamming codes with double adjacent error correction along with enhanced error detection is explained by Antony and Divya (2015). The parity of the information word is checked after reading the data from either memory or registers. The data word is correct when the even parity of 1's arrived in same information word; similarly, the information word is incorrect when the odd parity of 1's came in same information word.

Different types of Error Detection and Correction (EDC) codes are available to transmit the information data from source to destination without any error optimized dispersion compensation using orthogonal frequency-division multiplexing is determined by Barros and Kahn (2008). All those different types of EDC codes are bounded from two types of binary systems named as:

- Block codes
- Convolutional codes

Block codes are the combination of both linear and circular code which encodes the data into blocks. In linear block codes, input bits are partitioned into blocks traditionally improved power loading scheme for orthogonal frequency division multiplexing based cognitive radio is illustrated by Bepari and Mitra (2015). Linear block codes are used in Forwarding Error Correction (FEC) in which symbols are transmitted on a communications channel, so that, if errors occur in the transmission that can be detected or corrected by the parity of block codes. Cyclic codes are also blocked regulations in which circular shifts of each code word produces another circular code comparison

of fast Radix 2 ACS with adaptive fast Radix 2 ACS in Viterbi decoders illustrated by Bobby *et al.* (2013).

Design and performance analysis of the MIMO-OFDM System using different antenna configurations is presented by Agarwal and Mehta (2016). Fuzzy C strange points clustering algorithm and generating a digital signature based on the new cryptographic scheme for user authentication and security is described by Johnson and Singh (2016). The design of enhanced half ripple carry adder for VLSI implementation of two-dimensional discrete wavelet transform is approached.

MATERIALS AND METHODS

Convolutional encoder also one of the encoding techniques in which every single bit is encoded to two bits. Hence, 'n' bit data is encoded into '2*n' bit data. Convolutional coding and block coding are the two principal forms of channel coding of OFDM System. Convolutional codes operate on serial data, one or a few bits at a time. Unlike block codes, convolutional codes do not map individual blocks of bits into blocks of code words. Instead, convolutional codes accept a continuous stream of bits and map them into an output stream by introducing redundancies in the process. The convolutional codes have some "memory" that remembers the stream of bits that flow by. The number of preceding bits used in the encoding process is called as the constraint length m (that is similar to the memory in the system). The circuit diagram of the convolutional encoder for rate k/n = ½ is illustrated in Fig. 1-3. The state diagram of the convolutional encoder is shown in Fig. 2. Each state is labeled by two bits. Each transition is labeled s/vv2 where w output bits. The state transition of each state is shown Table 1. The top view of an adaptive viterbi decoder is shown in Fig. 3.

The Branch Metric Unit (BMU) determines the number of different bits between output symbol and input symbol. The output of BMU unit is given to Add Compare Select (ACS) unit. In ACS unit, branch metrics and previous path metrics are added and this compared with other track groups. Finally, a decision was made by comparing the weight of all nodes. The output symbol of smallest path node is stored in the path memory. Finally, Survivor Memory Unit (SMU) gives the desired decoded output symbols.

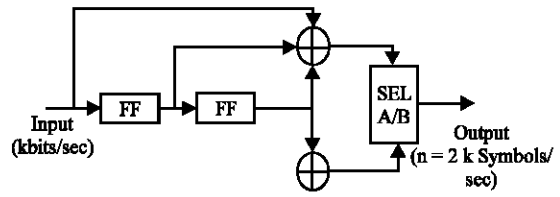

Fig. 1: Convolutional encoder for rate k/n = 1/2

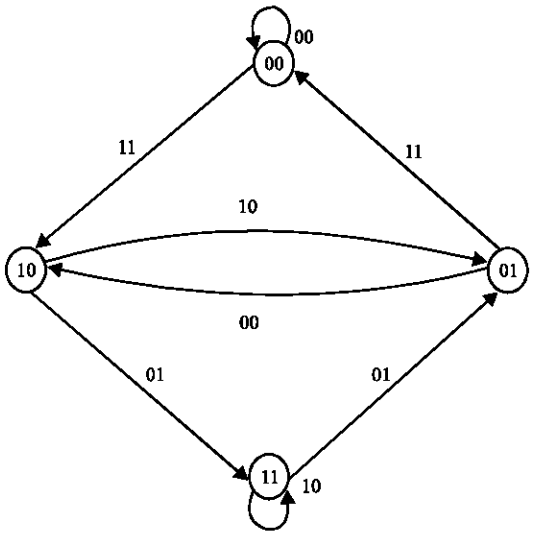

Fig. 2: State diagram for convolutional encoder

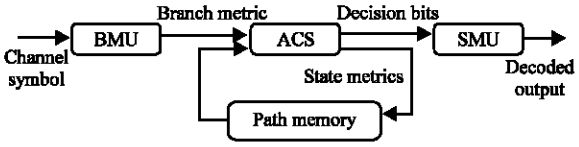

Fig. 3: Top view of decoder

Table 1: State transition table for convolutional encoder

	Next state/output symbol, if	
Current state	Input = 0	Input = 1
00	00/00	10/11
01	00/11	10/00
10	01/10	11/01
11	01/01	11/10

RESULTS AND DISCUSSION

To validate the proposed adaptive encoder and adaptive decoder model, ModelSim 6.3c is used in the present research. The simulation result of proposed adaptive encoder model for establishing high-speed operation is shown in Fig. 4 and 5. In Fig. 4, mode of the signal is assigned to logical '0'. The input width is considered as '8 bit' [01011100]. Similarly, the output

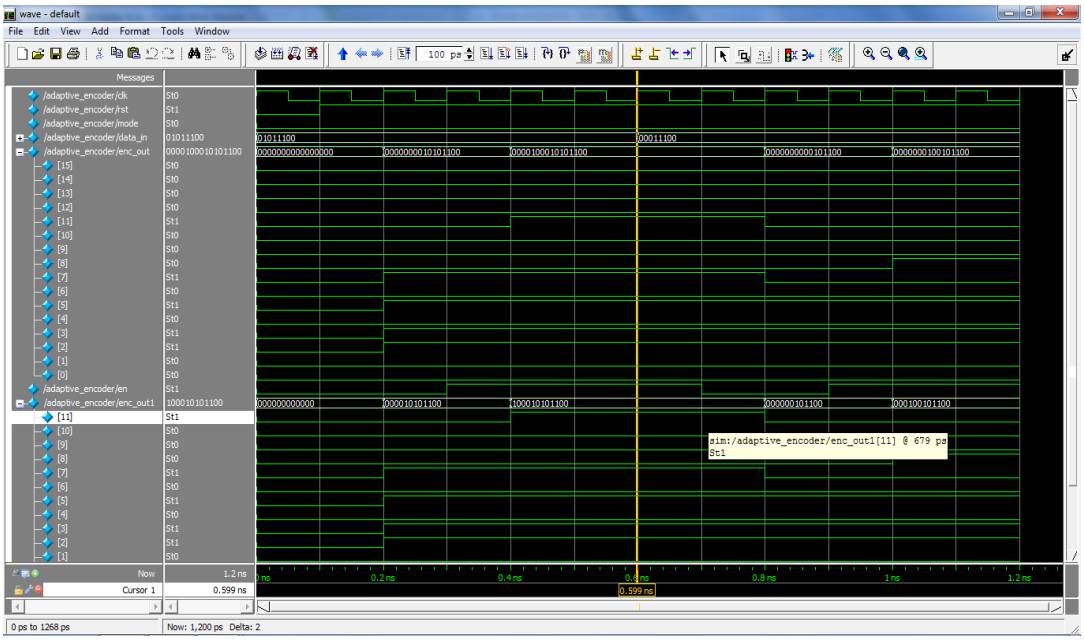

Fig. 4: Simulation result of proposed adaptive encoder model

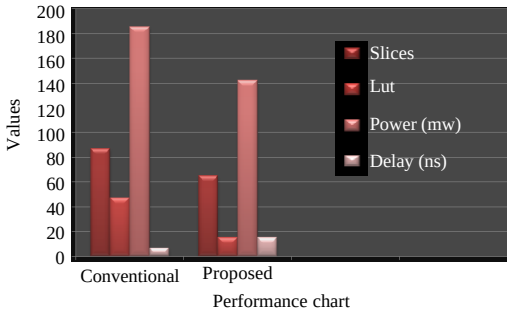

Fig. 5: Performances of encoder and decoder in graphical view

Table 2: Comparison results of both conventional and proposed encoder and decoder

Types	Slices	LUT	Delay (NS)	Power (mW)	Application
Hamming decoder	87	47	6.45	185	High speed
Convolutional	65	15	15.26	142	Low area and low power

width is considered as '12 bit (Data bits+Parity bits)' [000100101100]. Similarly, the simulation result of proposed adaptive encoder model for establishing little area and lower power consumption requirement (Convolutional encoder) is shown in Fig. 4. According to convolutional encoder logic, the input width is considered as '8 bit' [01011100] and output obtained is in '16 bit' (2*8) [0011100001100111] (Table 2).

From these analyzed results, it is clear that hamming based encoder and decoder technique has the high-speed operation than convolutional operation. Similarly, adaptive viterbi decoder process has better architectural performances regarding hardware and power reductions than hamming based encoder and decoder structure.

CONCLUSION

In this research, an adaptive encoder and adaptive decoder model are designed by using two powerful encoder and decoder techniques such as convolutional encoder hamming encoder/hamming decoder. Verilog hardware description language (Verilog HDL) is used to design a convolutional encoder model. It is a synthesizable language. Thus the synthesized results of proposed encoder and decoder techniques are compared through xilinx ISE design tool.

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