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Protraction of Bartlett Bisection Theorem to Cross Coupled Circuits

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Abstract: This study presents an extension to Barlett's bisection theorem that can be used for analysing balanced and symmetric circuits only. It is shown that the extended theorem could be used for both differential-mode and common-mode analysis of symmetric circuits that contain unbalanced cross-coupled structures. It is also shown that the new approach not only simplifies the analysis of complex circuits but also provides better insight.

Key words: Bisection theorem, common-mode analysis, cross-coupling, differential amplifiers, structures mode analysis, approach

INTRODUCTION

The Bartlett's bisection theorem is a powerful tool which can be used to analyze two-input, balanced and symmetrical circuits. Balanced symmetrical circuits can be divided into two identical parts where they are identical in topology, components, variables and values. These circuits are often decomposed into differential and common-mode equivalent circuits. The differential-mode and common-mode responses can then be determined independently applying proper inputs. Main advantage of applying the Barlett's bisection theorem is in simplifying the circuit for the differential-mode and common-mode analysis reducing number of circuit elements for hand calculation. These circuits are often termed as differential-mode and common-mode half-circuits. In both, half-circuit is analyzed and the results are expanded to whole circuit.

The bisection concept was first introduced by Bartlett and expanded by Brune (1932) and Iyer (1985) that geometrically symmetrical circuits were treated. In 1941 Cauer published his work on circuit theory titled "Theory of Linear AC circuit Leipzig". Cauer (1958) had an extended edition of his research where he discussed Barlett's and Brunes's theorems. In Cauer's research an extension to symmetric 4-ports was presented. Cauer was also able to extend the theorem to electrically symmetrical circuits where the response of each half is symmetrical and the physical implementation of the half-circuit is not required (Belevitch, 1962). Barlett's theorem gives parallel and series impedances when only there is direct connection between the two halves (Matheau, 1965). Matheau (1965) was able to prove that even the two-terminal-pair network exhibits only vertical symmetry it is always possible to find the parallel impedance Z_j of the equivalent symmetrical lattice assuming the current in both halves are equal.

There are many other circuits that are similar to balanced-symmetrical circuits except for the existence of cross-coupling between two halves where each half has a dependency found in the other half making them ineligible for application of the bisection theorem. An example of a balanced and symmetrical circuit with cross coupling can be identified in basic building blocks of a 4 bit quantizer shown in Briseno-Vidrios *et al.* (2017). Another example one is the non-overlapping cross coupled level shifter (Abouzied *et al.*, 2017). Cross coupling can also be found in many other balanced-symmetrical circuits such as the cross coupled oscillator circuit (Bostani *et al.*, 2017), dynamic comparator circuits (Chen *et al.*, 2017) in LNA circuits (Lin and Hsieh, 2017) and many other circuits (Sharma, 2012; Oathman *et al.*, 2016). Even though some end results in the form of equations and figures exist for these types of circuits, the reasoning and means to those ends have never been fully discussed by Wu *et al.* (2017) or has the Bisection theorem been applied or discussed.

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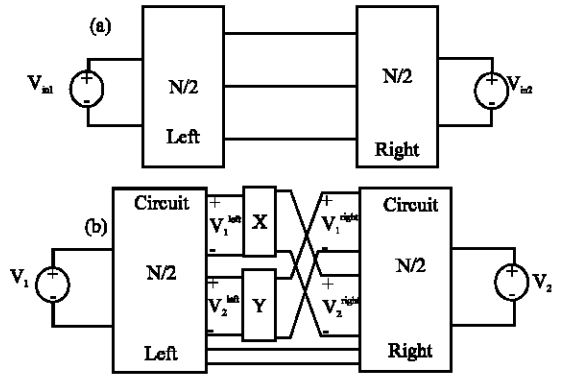

Fig. 1: A depiction of both type of circuit: a) A depiction of a balanced symmetrical circuit and b) A depiction of a circuit where two identical sections are connected by a set of cross-coupling circuits and by wires

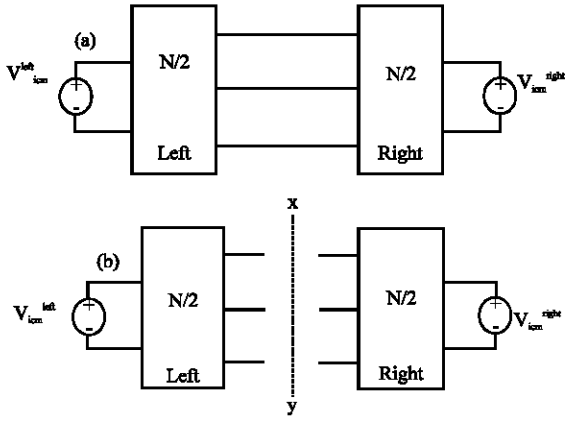

Fig. 2: Common-mode: a) A schematic depicting the case where the common-mode response is desired and b) Common-mode circuit bisected into two equivalent, independent halves

Moreover, common-mode analysis of these circuits has never been discussed or presented in the literature. Thus, the main contribution of this study is to show that the bisection theorem can be extended, so that, it could be applied to a wider class of circuits than balanced-symmetrical circuits including circuits with identical cross-coupling which is often found in the literature.

MATERIALS AND METHODS

Barlett's bisection theorem: A review of the bisection theorem is presented in this study following the structure presented by Iyer (1985).

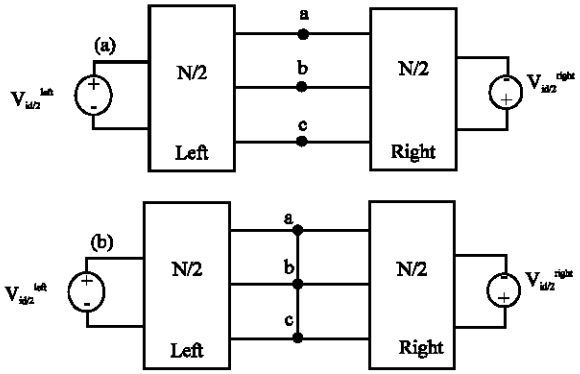

Fig. 3: Differential-mode: a) A schematic depicting the case where the differential-mode response is desired and b) Differential-mode circuit bisected into two equivalent, independent halves

Consider symmetrical circuits depicted in Fig. 1a. A circuit is considered symmetrical if it can be divided into two mirror-image schematics. Only the case where a direct connection between the two halves exists is considered. In Fig. 1, the input signals can be decomposed into their differential-mode and common-mode components. That is:

$$V_{in1} = V_{icm} + \frac{V_{id}}{2}$$
$$V_{in2} = V_{icm} + \frac{V_{id}}{2} \quad (1)$$

Figure 2a depicts the case where only the common-mode response is desired. $V_{id} = 0$ and $V_{in1} = V_{icm} = V_{in2}$. To determine the common-mode response, superposition may be applied and the analysis is done in two steps: $V_{icm}^{right} = 0$ and the response to V_{icm}^{left} is determined, $V_{icm}^{left} = 0$ and the response to V_{icm}^{right} is determined.

In step 1 current flows from the left half to the right half through each of the connecting wires. In step 2 current flows from right half to the left half. This current is equal in magnitude and 180° out of phase with the previous step. Thus, the total current that flows between the two halves is in each of the wires is 0.

Based on the results of the previous analysis, the circuit in Fig. 2a can be transformed to an equivalents circuit shown in Fig. 2b. In this case, the halves are bisected along the vertical defined by x-y and the connections between the two halves are opened, decomposing the circuit into two equivalent, independent circuits. There introduces a significant reduction in the analysis complexity as only one half of the circuit needs to be analyzed and the results of the analysis are applicable to the second half. Next, the case where the differential-mode response is considered. For this case, $V_{icm} = 0$ and $V_{in1} = V_{id}/2 = -V_{in2}$ (Fig. 3a).

Superposition is applied the schematic in Fig. 3a to determine the differential-mode response in two steps: 1 $V_{id}^{right}/2 = 0$ and the response to $V_{id}^{left}/2$ is determined, 2 $V_{id}^{left}/2 = 0$ and the response to $V_{id}^{right}/2$ is determined.

In Case 1, V_{ab}^{left}, V_{bc}^{left} and V_{ac}^{left} are determined. In Case 2, the source sees the same circuit as the source in Case 1. Since, the sources are equal in magnitude but 180° $V_{ab}^{right} = -V_{ab}^{left}$, $V_{bc}^{right} = -V_{bc}^{left}$, $V_{ac}^{right} = -V_{ac}^{left}$. Thus, $V_{ab} = V_{ab}^{right} + V_{ab}^{left} = 0$. Likewise, $V_{bc} = V_{cb} = 0$ and in summary and any branch voltage that can be defined based on any pairing of wires is zero. Thus, all of the connecting wires can be treated as though they are bound by a virtual short circuit. This can be extended to the case of "n" branches that will result $\sum_{i=1}^{n-1} n-i$ in wire pairings and so all branch voltages are zero. In practice, one of the connecting wires is often at ground, resulting in all node voltages defined with reference to ground. Thus, the voltages at the connecting wires are at zero and be treated as a virtual ground.

Based on the results of the previous the circuit can be transformed to the equivalent circuit of Fig. 3b. For this case, the halves are bisected and the connections between the two halves are connected with a dotted line that symbolizes a virtual short. As with the common-mode analysis, there is an enormous reduction in complexity since only one half the circuit needs to be analyzed with the results of the analysis now applicable to the second half by setting all voltages and currents 180° out of phase with the counterpart halve.

RESULTS AND DISCUSSION

Protraction of the Barlett's bisection theorem: To extend the bisection theorem to where cross-coupling exists it is first shown that this type of circuit can be transformed into a symmetrical circuit where two identical halves for both the common-mode and differential-mode exist. Once the transformations are complete. For convenience, a two-port network described using Y-parameters models each individual cross-coupling circuit in the set. For each individual cross-coupling circuit, one independent voltage resides in one section and the second independent voltage resides in the other study.

Consider the schematic show in Fig. 1b for the case where two identical sections that are mirror images of each other exist and each section has identical cross-coupling from the other. Cross-coupling is taken to mean that the section on the left has a dependency on the section on the right via a cross-coupling circuit and vice versa.

Since, the topology of each section is identical, every branch voltage in the left-hand sign has a counterpart branch voltage in the right-hand side. For example, if a

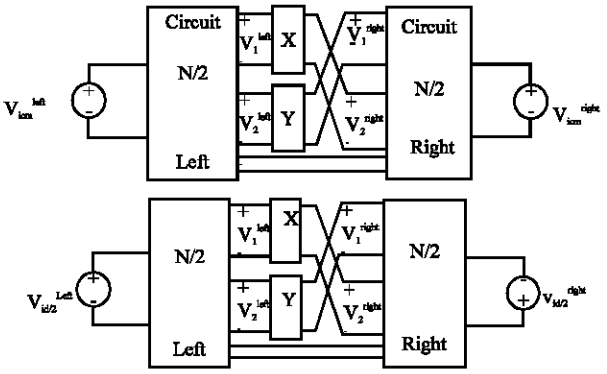

Fig. 4: A schematic depicting a cross-coupled circuit: a) The case where the common-mode response is desired and b) The case where differential-mode response is desired

branch voltage is defined across a single resistor in the left section that resistor has a mirror image in the right section and there is a branch voltage across that resistor that corresponds to the voltage across the resistor in the left section. In general if V_i^{left} exists in the left hand side, there is a counterpart V_i^{right} in the right hand side.

For convenience, the cross-coupling circuits are modelled with Y-parameters. The general set of equations that models the cross-coupling circuits is:

$$\begin{aligned} I_1 &= y_{11}V_1 + y_{12}V_2 \\ I_2 &= y_{21}V_1 + y_{22}V_2 \end{aligned} \quad (2)$$

For each cross-coupled circuit, the branch voltage V_1 is found in one symmetrical halve original and the branch voltage V_2 is found in other. Thus, port relationships for the cross coupling circuit labeled "X" can be expressed as:

$$\begin{aligned} I_1 &= y_{11}V_1^{left} + y_{12}V_2^{right} \\ I_2 &= y_{21}V_1^{left} + y_{22}V_2^{right} \end{aligned} \quad (3)$$

The port relationships for the cross-coupling circuit labelled "Y" can be expressed as:

$$\begin{aligned} I_1 &= y_{11}V_1^{right} + y_{12}V_2^{left} \\ I_2 &= y_{21}V_1^{right} + y_{22}V_2^{left} \end{aligned} \quad (4)$$

Figure 4a depicts the schematic used for the common-mode analysis. Superposition is applied to determine the response in two steps: 1 $V_{icm}^{right} = 0$ and the response to V_{icm}^{left} is determined, 2 $V_{icm}^{left} = 0$ and the

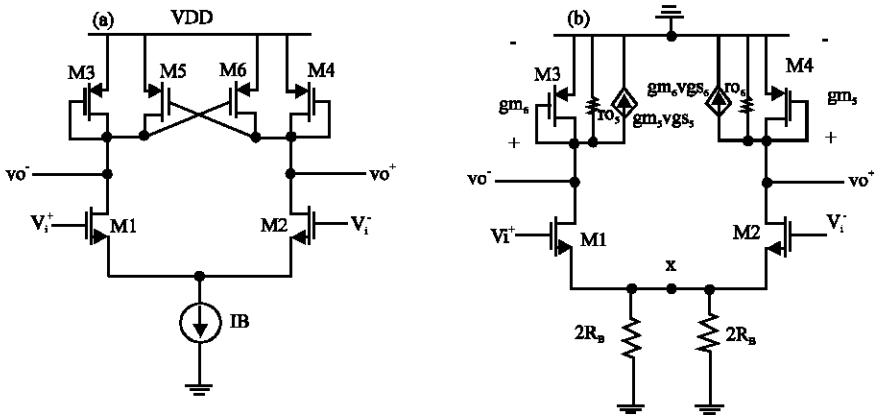

Fig. 5: A differential amplifier with cross-coupling: a) The schematic and b) AC equivalent circuit

response to V_{icm}^{right} is determined. V_1 will be considered first. In step 1, $V_1^{left,\ I}$ and $V_1^{right,\ I}$ are determined. In step 2, $V_1^{left,\ ii}$ and $V_1^{right,\ ii}$ because both sources see identical circuits $V_1^{left,\ I} = V_1^{right,\ ii}$ and $V_1^{right,\ I} = V_1^{left,\ ii}$. Thus, $V_1^{left} = V_1^{left,\ I} + V_1^{left,\ ii} = V_1^{nitht,\ ii} + V_1^{right,\ I} = V_1^{right}$. Thus V_1^{left} is equal to its counterpart voltage V_1^{right}. Likewise, V_2^{left} is equal to its counterpart voltage V_2^{right} and in general, all counterpart voltages and currents are equal. This means for the case of a common-mode input voltage that the two-ports can be described with the Eq. 5 and 6:

$$\begin{aligned} I_1 &= y_{11}V_1^{left} + y_{12}V_2^{left} \\ I_2 &= y_{21}V_1^{left} + y_{22}V_2^{left} \end{aligned} \quad (5)$$

$$\begin{aligned} I_1 &= y_{11}V_1^{right} + y_{12}V_2^{right} \\ I_2 &= y_{21}V_1^{right} + y_{22}V_2^{right} \end{aligned} \quad (6)$$

The dependencies for each cross coupling circuit have been moved to a single half. The circuit now meets the criteria for a symmetrical circuit and the analysis shown in study can be applied. For practical circuits, the movement from Eq. 3-6 can be achieved by performing operations on the schematic that effectively achieve the same end.

Figure 4b depicts the schematic for the case where the differential-mode analysis. Superposition is applied to determine the response in two steps: 1 $V_{id}^{right}/2 = 0$ and the response to $V_{id}^{left}/2$ is determined, 2 $V_{id}^{left}/2 = 0$ and the response to $V_{id}^{right}/2$ is determined.

V_1 will be considered first. In step 1, $V_1^{left,\ I}$ and $V_1^{right,\ i}$ are determined. In step 2, $V_1^{left,\ ii}$ and $V_1^{right,\ ii}$ because both sources see identical circuits $V_1^{left,\ I} = -V_1^{right,\ ii}$ and $V_1^{right,\ I} = -V_1^{left,\ ii}$. Thus, $V_1^{left} = V_1^{left,\ I} + V_1^{left,\ ii} = -V_1^{nitht,\ ii} + -V_1^{right,\ I} = -V_1^{right}$. Thus, V_1^{left} is equal in magnitude but opposite in phase to its counterpart voltage V_1^{right}.

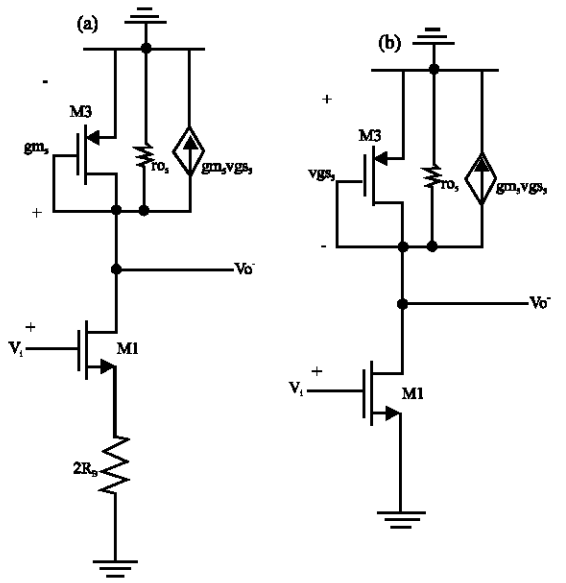

Fig. 6: AC equivalent half-circuit: a) Common-mode and b) Differential-mode

Likewise, V_2^{left} is equal in magnitude but opposite in phase to its counterpart voltage to its counterpart voltage V_2^{right} and in general, all counterpart voltages and currents are equal in magnitude and opposite in phase. This means for the case of a differential-mode input voltage that the two-ports can be described with the Eq. 7 and 8:

$$\begin{aligned} I_1 &= y_{11}V_1^{left} - y_{12}V_2^{left} \\ I_2 &= y_{21}V_1^{left} - y_{22}V_2^{left} \end{aligned} \quad (7)$$

$$\begin{aligned} I_1 &= y_{11}V_1^{right} - y_{12}V_2^{right} \\ I_2 &= y_{21}V_1^{right} - y_{22}V_2^{right} \end{aligned} \quad (8)$$

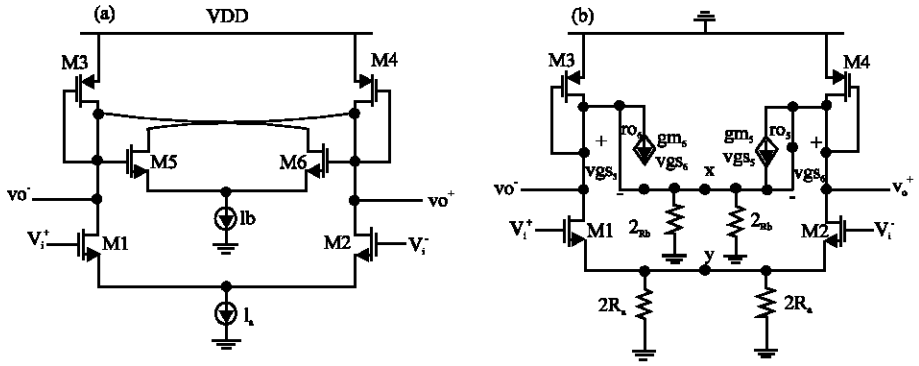

Fig. 7: A differential amplifier where the cross-coupling is achieved with a second differential pair; a) The schematic and b) AC equivalent circuit

The circuit now meets the criteria for a symmetrical circuit and the analysis shown in study can be applied. For practical circuits, the movement from Eq. 3 and 4 to Eq. 7 and 8 can be achieved by performing operations on the schematic that effectively achieve the same end.

Examples: An example of a circuit with cross-coupling is provided in Fig. 5a (Pei and Kan, 2004). In this schematic M_1 and M_3 form the study and M_2 and M_4 form a mirror image. M_5 forms one cross-coupling circuit and M_6 forms the other.

An AC equivalent circuit is shown in Fig. 5b. The output resistance of the current source has been split into two resistors, so that bisection at node "x" can be performed. M_5 and M_6 are replaced with small-signal models.

The ideal common-mode gain when the output is taken differentially is zero. However, it has been shown that when there is mismatch the common-mode gain is no longer zero and a common-mode half circuit can still provide useful qualitative and quantitative information about the common-mode response (Amourah and Geiger 2001). For the common-mode response, $V_i^+ = V_{icm} = V_i^-$. The connecting wire at "x" can be cut and opened. V_{gs5} has a counterpart voltage V_{gs6} and so, they are equal. The dependency of M_5 is moved to the left half and the dependency of M_6 is moved to the right half. The circuit can now be bisected. A resulting AC schematic for a half-circuit is shown in Fig. 6a.

The voltage controlled current source can be replaced with a resistor with a value of $1/gm_5$. The common-mode half-circuit forms a common-source amplifier with source degeneration. The drain resistance of M_1 is significantly reduced by M_5 due to the cross coupling. The expression for the drain resistance of M_5 is: the single-ended common-mode gain is expressed as:

$$R_D = (1/gm_3 \| ro_3 \| 1/gm_5 \| ro_5) \quad (9)$$

$$A_{cm,\,se} = \frac{-gm_1 \times R_D}{1+2(gm_1+gmb_1+1/ro_1)R_B+R_D/ro_1} \quad (10)$$

Equation 10 can be simplified to:

$$A_{cm,\,se} = \frac{1}{2(gm_3+gm_5)R_B} \quad (11)$$

For the differential-mode response, $V_i^+ = V_{id}/2 = -V_i^-$. The connecting wire between the R_B can set to zero. Vgs_5 has a counterpart voltage Vgs_6, so, they are in magnitude but opposite in phase and so $Vgs_5 = -Vgs_6$. The dependency of M_5 is moved to the left half and the dependency of M_6 is moved to the right half. The circuit can now be bisected. A resulting AC schematic for a half-circuit is shown in Fig. 6b.

The voltage controlled current source can be replaced with resistors with a value $-1/gm_5$. The differential-mode half-circuit forms a common-source amplifier. The drain resistance of M_1 can be made significantly larger since the overall drain resistance can be increased significantly due to the cross-coupling transistor M_5 acting as a negative resistance. The differential-mode gain for the single-ended out is:

$$A_{dm,\,se} = -\frac{1}{2}gm_1\left(ro_3 \| 1/gm_3 \| ro_5 \| -1/gm_5\right) \quad (12)$$

The differential-mode gain for the differential output is:

$$A_{dm,\,do} = gm_1\left(ro_3 \| 1/gm_3 \| ro_5 \| -1/gm_5\right) \quad (13)$$

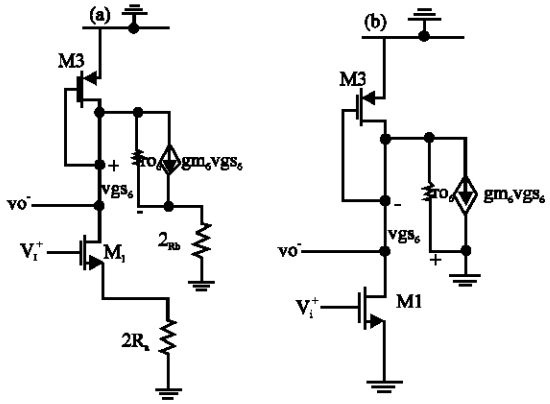

Fig. 8: AC equivalent half-circuit: a) Common-mode and b) Differential-mode

An example of a more complicated circuit with cross-coupling is shown in Fig. 7a (Razavi, 2002). The AC equivalent circuit is shown in Fig. 7b. The output resistance of I_a and I_b have been represented by two resistances rather than one in order to bisect the circuits. Figure 7b does not fit the case depicted by Fig. 1b since, there are not two identical cross-coupled circuits but a single cross-coupling circuit formed by a differential pair.

For the common-mode analysis, the schematic in Fig. 7b can be transformed to a half-circuit by cutting the connecting wire at "x" and "y" and opening both by the line of reasoning found in study. V_{gs5} has a counterpart voltage V_{gs6} and so, they are equal. The dependency of M_5 is moved to the left half and the dependency of M_6 is moved to the right half. The circuit has now been can now be bisected. A resulting AC schematic for a half-circuit is shown in Fig. 8a. The result is a common-source amplifier with source degeneration.

The drain resistance for M_1 is M_3 which is diode connected in parallel with the resistance looking into the drain of M_6, which behaves like a cascode. Thus, the drain resistance of M_1 is approximately:

$$R_D \approx 1/gm_{3\,3} \tag{14}$$

The single-ended common mode gain is expressed is:

$$A_{cm,\,se} = -\frac{gm_1 \times R_D}{1+2\times(gm_1+gmb_1)\times R_a + R_D/ro_1} \tag{15}$$

This can be simplified to:

$$A_{cm,\,se} = -\frac{1}{2\times gm_1 \times R_a} \tag{16}$$

For the differential-mode analysis, the schematic in Fig. 7b can be transformed to a half-circuit by cutting the connecting shorting the connecting wires at "x" and "y" by the line of reasoning found in study. Vgs_5 has a counterpart voltage Vgs_6, so, they are in magnitude but opposite in phase and so, $V_{gs5} = -V_{gs6}$. The dependency of M_5 is moved to the left half and the dependency of M_6 is moved to the right half. The circuit is now be bisected. A resulting AC schematic for a half-circuit is shown in Fig. 8b.

The circuit in Fig. 8b is topologically identically to that in Fig. 6b so, those results apply for this case. The differential-mode gain for the single-ended out is:

$$A_{dm,\,se} = -\frac{1}{2}gm_1\left(ro_3 \| 1/gm_3 \| ro_5 \| -1/gm_5\right) \tag{17}$$

The differential-mode gain for the differential output is:

$$A_{dm,\,do} = gm_1\left(ro_3 \| 1/gm_3 \| ro_5 \| -1/gm_5\right) \tag{18}$$

Both examples shown in Eq. 15 are simulated using cadence simulation tools in order to verify the equations developed for both circuits. Going back to Eq. 13, it can be seen that when gm_1 and gm_2 are increased, the gain of the differential amplifier with cross coupling shown in Fig. 5a. is accordingly increased as shown in Fig. 9a. gm_1 and gm_2can be increase by increasing W_1 and W_2 or by increasing the tail current. W_1 and W_2 are set to be equal to 10 μm where the gain for low frequencies is equal to 46 dB as shown in solid line in Fig. 9a and when W_1 and W_2 are set to be equal to 100 μm, the gain for low frequencies is equal to 53.2 dB as shown in dots line in Fig. 9a.

Similarly, going back to Eq. 18 it can be seen that when gm_1 and gm_2 are increased, the gain of the circuit shown in Fig. 7a is accordingly increased as shown in Fig. 9a. gm_1 and gm_2 can be increase by increasing W_1 and W_2 or by increasing the tail current. W_1 and W_2 are set to be equal to 10 μm where the gain for low frequencies is equal to 18.2 dB as shown in solid line in Fig. 9a and when W_1 and W_2 are set to be equal to 100 μm, the gain for low frequencies is equal to 28dB as shown in dots line in Fig. 9b.

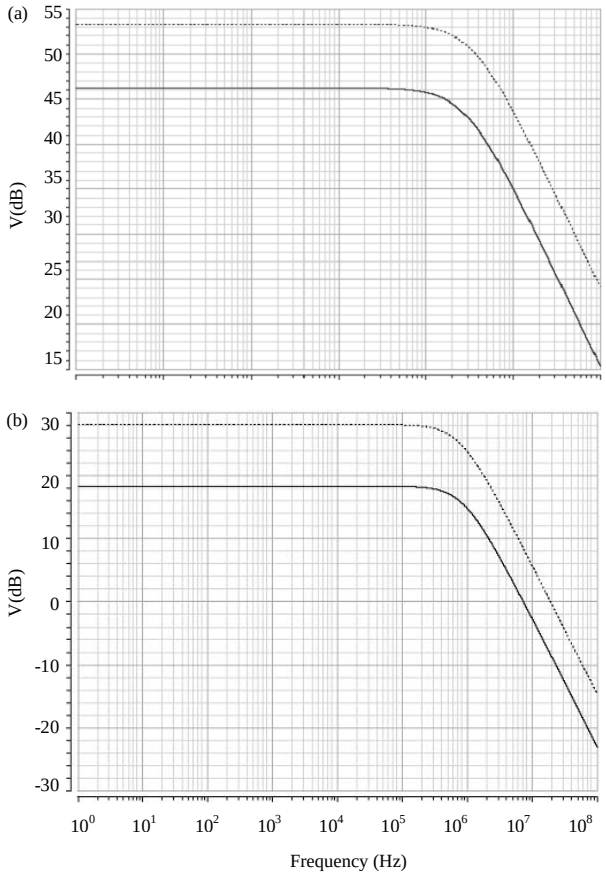

Fig. 9: Simulation: a) Gain simulation for the differential amplifier with cross coupling where W1 = 10 μm and W2 = 10 μm in solid line and W1 = 100 μm and W2 = 100 μm in dot line and b) Gain simulation for the differential amplifier where the cross-coupling is achieved with a second differential pair. W1 = 10 μm and W2 = 10 μm in solid line and W1 = 100 μm and W2 = 100 μm in dot line

CONCLUSION

It has been shown that the bisection theorem can be extended to include to the case of a balanced circuit with cross-coupling for any number of cross-coupling sets and any level of complexity as long as each set of cross-coupling circuits contains individual cross-coupling circuits that are equal. The results of the extension have been applied to two differential amplifiers with cross-coupling that are currently found in the literature to do a differential and common-mode analysis. The method made clear the steps in determining the half-circuits and provided insight while reducing complexity of the analysis.

REFERENCES

Abouzied, M.A., K. Ravichandran and E. Sanchez-Sinencio, 2017. A fully integrated reconfigurable self-startup RF energy-harvesting system with storage capability. IEEE. J. Solid State Circuits, 52: 704-719.

Amourah, M.M. and R.L. Geiger, 2001. A high gain strategy with positive-feedback gain enhancement technique. Proceedings of the 2001 IEEE International Symposium on Circuits and Systems (ISCAS'01) Vol. 1, May 6-9, 2001, IEEE, Sydney, New South Wales, pp: 631-634.

Belevitch, V., 1962. Summary of the history of circuit theory. Proc. IRE., 50: 848-855.

Bostani, R., G. Ardeshir and H. Miar-Naimi, 2017. Analysis of Millimeter-Wave LC oscillators based on two-port network theory. IEEE. Trans. Circuits Syst. II. Express Briefs, 64: 239-243.

Briseno-Vidrios, C., A. Edward, A. Shafik, S. Palermo and J. Silva-Martinez, 2017. A 75-MHz continuous-time sigma-delta modulator employing a broadband low-power highly efficient common-gate summing stage. IEEE. J. Solid State Circuits, 52: 657-668.

Brune, O., 1932. Note on Bartlett's bisection theorem for 4-terminal electrical networks. London Edinburgh Dublin Philos. Mag. J. Sci., 14: 806-811.

Cauer, W., 1958. Synthesis of Linear Communication Networks. McGraw-Hill Education, New York, USA., Pages: 866.

Chen, L., K. Ragab, X. Tang, J. Song and A. Sanyal *et al*., 2017. A 0.95-mW 6-b 700-MS/s single-channel loop-unrolled SAR ADC in 40-nm CMOS. IEEE. Trans. Circuits Syst. II. Express Briefs, 64: 244-248.

Iyer, T.S.K.V., 1985. Circuit Theory. McGraw-Hill Education, New York, USA., Pages: 521.

Lin, J.Y. and C.C. Hsieh, 2017. A 0.3 V 10-bit SAR ADC with first 2-bit Guess in 90-nm CMOS. IEEE. Trans. Circuits Syst. I. Regul. Pap., 64: 562-572.

Matheau, J.C., 1965. Two-terminal-pair network bisection. Electron. Lett., 1: 131-131.

Oathman, J., P.S. Tahseen and N. Khan, 2016. Design and implementation of dynamic track and latch comparator using CMOS in 0.18 um technology. Intl. J. Adv. Trends Comput. Sci. Eng., 5: 10-12.

Pei, G. and E.C. Kan, 2004. Independently driven DG MOSFETs for mixed-signal circuits: Part I-quasi-static and nonquasi-static channel coupling. IEEE. Trans. Electron. Devices, 51: 2086-2093.

Razavi, B., 2002. Dsign of Analog CMOS Intgrtd Circuits. McGraw-Hill Education, New York, USA., ISBN-13:978-0-07-052903-8, Pages: 685.

Sharma, M., 2012. Design and analysis of CMOS cells using adiabatic logic. Intl. J. Netw. Syst., 1: 52-57.

Wu, L., H.F. Leung, A. Li and H.C. Luong, 2017. A 4-element 60-GHz CMOS phased-array receiver with beamforming calibration. IEEE. Trans. Circuits Syst. I. Regul. Pap., 64: 642-652.