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A Comparison of Low Noise Amplifires Design and Techniques

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Abstract: Low noise amplifier is used in many applications, especially in wireless communication. It is used in the front and end of the radio system. The design of the amplifier depends on many criteria such as the gained power, chip size and noise ratio. This research is a review of common known techniques that are used to design and implement the low noise amplifier. This research is focusing on noise ratio, gained power and chip size of different topologies for low noise amplifiers.

Key words: Amplifiers, power gain, noise ratio, low noise amplifier, electronic design, power

INTRODUCTION

Nowadays most of components are based on electrical systems. In many countries and places around the world the voltages and currents are not stable. This instability of the voltages and current cause noise. There are several kinds of noise in the electrical circuits. Many algorithms are applied to reduce these noises. The electrical signal that is traveling for long distance became weaker. To retain its power, it should by amplifying using amplifiers. This kind is known as low noise amplifier. The low noise amplifier is working on reducing the effect of the noise that is appearing in consecutive stages of the circuit by multiplying the signal by again. Higher gain such as -25 dB means higher quality of a low noise amplifier and low gain means more compression points. The low noise amplifier is used in many applications such as wireless LAN and mobile communication systems. In these applications which are wireless, Signal to Noise Ratio (SNR) is used to measure and maintain the quality of the signal in both transmitters and receivers.

Generally, the low noise amplifier can be defined as the combination of high gain, stability of the system and low noise over an entire signal path or signal frequency. The low noise amplifier is not a constant value, it is implemented per what is needed that means there are a variety of parameters in developing. The parameters that are monitored or represent the low noise amplifier behavior are the high gain, power consumption and low noise. The low noise amplifier is widely used in communication systems. It is used to receive an amplified signal with low noise as possible. For example, in radio systems the receiver's frequencies are a combination of amplifiers and mixer. There are two main kinds of amplifiers which are the normal devices and S parameters. The low noise amplifiers are designed based on S parameters. From electronic point of view both the normal device and S parameters are built from transistors. External bias can be applied to the normal devices but in S parameters which is built in its fixed (Kim *et al*., 1998). Every designed system has an exact specification. In a low noise amplifier, the specifications are shown as:

- Gain (dB)
- Proper biasing
- Noise (dB)
- Bandwidth (Hz)
- Sensitivity
- Linearity
- Proper transistor selection

MATERIALS AND METHODS

Low noise amplifier methods

Spiral inductor: The low noise amplifier is implemented using CMOS integrated circuit from metal with 0.8 μm thickness. Silicon is used as a semiconductor material in implementation because of its high resistivity. Spiral inductors with quality factor of 8.5-12.5 is used to reach the higher performance of the low noise amplifier

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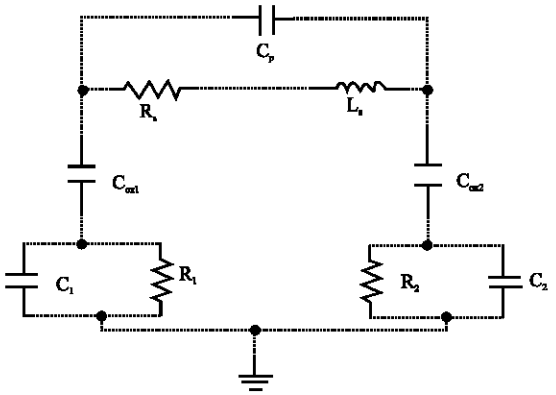

Fig. 1: Spiral inductor circuit

(Sackinger and Ficsher, 2000). The higher optimization of the low noise amplifier is reached when the active device is in bias condition. With 3.6 V of power supply the gain is 15 dB and the noise is 2.8 dB. Figure 1 shows the electrical circuit design of the spiral inductor low noise amplifier.

Shunt peaking: The shunt peaking technique is the process of providing active load at each gain stage. This type of amplifier is implemented using CMOS chip with 0.25 μm that means it's smaller than spiral inductor. It needs 2.5 V power supply to work. The lower power that is needed to turn on the amplifier is because of using inverse scaled stages. To provide insensitive DC gain and more boosting amplifier, the active inductors with low voltage drop is used. This amplifier is giving 16 dB noise measurement, 3 GHz of bandwidth and 32 dB gain (Cha and Lee, 2002). Figure 2 shows the simple design of shunt peak electrical circuit.

Current reuse: Two stages amplifier is used to gain high current depending on the series of inter stage resonance. The two-stage high performance amplifier design is based on a combination of a series of inter stage resonance and 0.35 μm CMOS chip. This optimization will give high performance that can reach to 5.2 GHz. To reduce the signal loss, increase the gain and make the amplifier more stable, the common source is implemented in first stage and the cascode amplifier is the second stage. The power gain that is provided by the 5.2 GHz evaluation of the amplifier and the noise is 2.45 dB. Figure 3 shows the basic design of current reuse amplifier.

Plug and play: With years, the performance of the amplifiers is increasing. With plug and play amplifier that is a fully functional integrated low power can go up to 5.5 GHz. This low noise amplifier is based on 90 nm

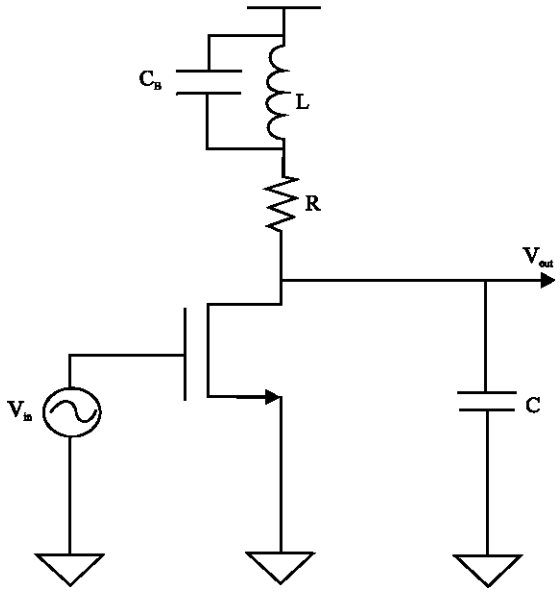

Fig. 2: Shunt peaking amplifier

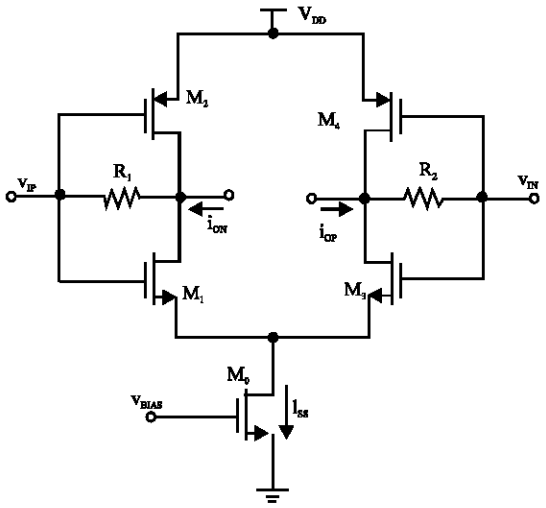

Fig. 3: Current reuse amplifier design

COMS chip that is used ESD protection in RF. A plug and play is working as Bidirectional ESD protection device that has been implemented by integrating inductor. This amplifier gives a power gain of 13.3 dB and consume power of 9.7 mW. With 14 dB input signal, the losses in this amplifier are only 2.9 dB (Liscidini *et al*., 2006).

Positive current, voltage feedback: The architecture of this low noise amplifier is based on a CMOS chip that has a front-end receiver with multiband positive feedback and linear mixer. A new technology which is narrow band tunable is used in this amplifier which depends on the

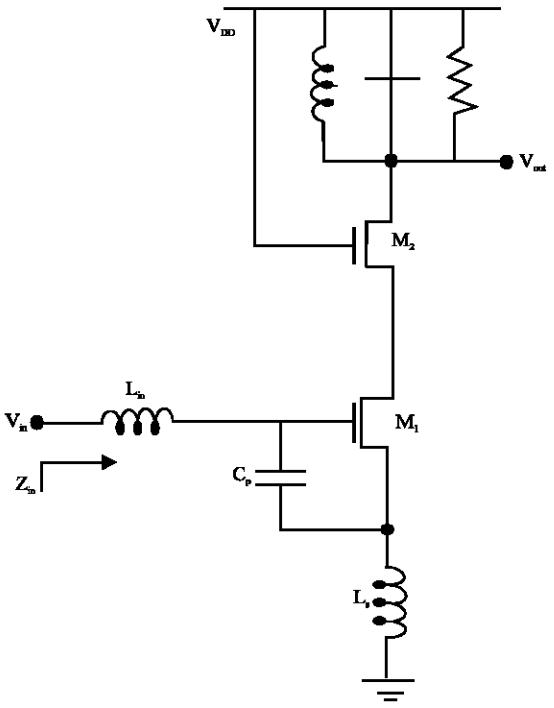

Fig. 4: Inductive degenerative basic design

positive feedback on voltage current. This technique allows the low noise amplifier to use a common input for all standard while selecting the frequency. The big improvement of this type of amplifier over the other topologies is in term of the value of the gain which higher than other low noise amplifier topologies and its present lower noise. In the other hand, using the high linearity mixer gives an advantage of avoiding the off-chip filter after the low noise amplifier usage. The gain value that is measured by using this technique is 13.5-28.5 dB depending on different criteria and the noise ratio is 5.2 dB (Yu *et al*., 2007).

Inductive degenerative: The inductive degenerative amplifier is implemented based on distributed amplifier to improve the noise performance by reducing the broadband noise during low power operation. This amplifier is designed on 0.18 μm COMS chip with 0.6 V of power consumption. The cascade is the common source power for this kind of amplifier. The reason of using cascode is to extend the bandwidth and improve the gain. The inductive degenerated amplifier provides 10 dB of gain, 3 dB of bandwidth and 4.6 dB of noise ratio (Fan *et al*., 2008). Figure 4 shows the basic design of the inductive degenerative amplifier.

Linearity improvement and noise reduction: The new technique is proposed to reduce the noise. This technique is called linearity improvement and noise reduction which is based on differential cascodes of a low noise amplifier. This technique is a combination of inductor connected and cross coupling capacitance of the cascode transistor to reduce the noise in nonlinearity way. The cross coupling capacitive is working on increasing the effective transmission while the cascode transistors is reducing the impedance and improve the linearity. The result of using this combination is to gain higher voltage. This amplifier is implemented on 0.35 μm CMOS chip that is providing 8.4 dB of gain and 1.92 dB of noise ratio (Chen and Lin, 2009).

Self-biased resistive feedback: A self-biased resistive feedback is proposed. A 90 nm CMOS chip is used to fabricate a low power wideband of the proposed low noise amplifier. To enhance the bandwidth of the amplifier, a shunt peaking inductor is used with two extra inductors inside the feedback. MOSFET was used as the load with the inductive degeneration while the main inductor related to the input transistor in series mode in the feedback loop. To achieve the self-bias, the DC capacitor was removed. This amplifier produces 12.7 dB of gain power and 3.3 dB of noise ratio (Yeh *et al*., 2011).

Noise reduction transformer: The new low noise amplifier is implemented based on any technology that is presented. This technology is using noise reduction transformer with multicascode configuration. These two transformers are with different design. One of them is designing at V-band which is a triple cascode transformer and the other is a quadruple cascode transformer. This amplifier is fabricated on 90 nm CMOS chip. The noise reduction is staged before the triple and quadruple cascode. The main goal of this amplifier is to minimize the chip size, increase the gain and reduce the noise. The gained power and noise of this amplifier is divided on the V and Q band where the gain of Q band is 20.3 dB, the noise ratio is 4.6 dB and the V band's gain is 12.7 dB and the noise ratio is 4.7 dB (Yu and Neihart, 2013).

Decoupling capacitor: Based on high linearity wideband low noise amplifier, new topology is proposed which is modified from that one. Two tone signals and high immune of frequency offset is achieved by adding decoupling capacitors and connecting the PMOS transistor to the input rather than biasing. This amplifier is implemented on 0.13 μm COMS chip. The gained power from this amplifier is 12.4 dB and the noise ratio is 1.6 dB (Feng *et al*., 2013).

Multimode match input network: Using single band rather than multiband sometimes gives its

Table 1: Comparison results

Amplifier	Chip size	Gained power (dB)	Power consumption (mW)	Noise ratio (dB)
Plug and play inductor	90 nm	13.3	9.72	2.9
Distributed amplifier	0.18 μm	10	7	3.8-6.9
Self-biased resistive amplifier	90 nm	12.7	12.6	3.3
One stage triple cascode with noise reduction	90 nm	12.7	18	4.7
Inductively degeneration	130 nm	14.7-16.4	6.40	1.9-4.7
Three stages cascode resistive feedback	65 nm	11.5	25.5	4.5

advantages. The low noise amplifier that is proposed can concurrent ultra-wide band operation. This amplifier has the largest bandwidth over all kinds that are reviewed in this study. Novel reconfigurable of multimedia input matching is achieved with this amplifier. Based on the 0.13 μm CMOS chip, multi tap transformer based reconfigurable Multimode low noise amplifier is implemented (Yu and Neihart, 2013).

Multistage inductive series peaking: Multi stage inductive series peaking is used to reach higher power gain with small variations. To achieve excellent input matching over a wide bandwidth, a parallel tuning capacitor is used in the feedback network with compact inductor. Three stages resistive feedback cascode provides power gains of 11.5 and 4.5 dB noise ratio (Feng *et al*., 2013).

RESULTS AND DISCUSSION

The reviewed kinds of amplifiers in this study. There is a huge improvement in terms of gaining power and noise ratio over the years. From 1998 until now many researches have been done to enhance the low noise amplifiers capabilities. All the reviewed amplifiers are implemented on CMOS chip but with different chip size. in some cases, the size is more important than the gain or noise ratio. Overall the best one that can balance between the size, gain and noise ratio. Table 1 shows the compression of later generations of low noise amplifier with the chip size, gained power, power consumption and noise ratio for each one of them.

Table 1 shows it is easily concluded that there are advantages of each amplifier over others because each one is used for different purposes. The main point of selecting amplifier is the noise ratio. Lower noise is better. Figure 5 shows the noise ratio performance of the reviewed amplifiers over the years. Figure 5 is can be easily noticed the growth of amplifiers, noise performance where at 2000 the noise ratio was around 16 dB and at 2013 the noise ratio is <2 dB.

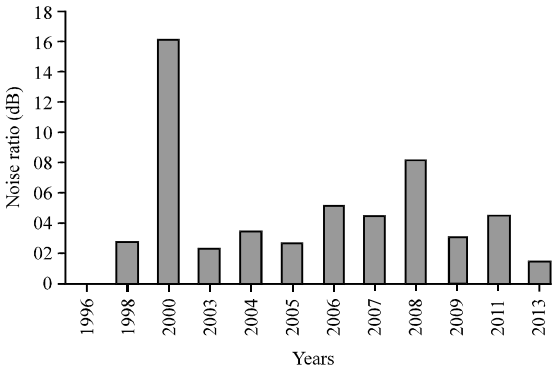

Fig. 5: Noise ratio performance over years

CONCLUSION

This study is a review of different types of low noise amplifiers in terms of design, implemented chip size, gain power and noise ratio. Different techniques are used over the years to increase the gained power and reduce the noise ratio of the low noise amplifiers. A group of these amplifiers is studied and reviewed in this research.

IMPLEMENTATIONS

The implementation of these amplifiers is different depends on the design but all of them are sharing that implemented on a CMOS chip with different sizes. From the results this review, it can be noticed that over the years there is increasing in the gained power and reducing the noise ratio. This because of technology. For future research, there is a proposed technique that we research on it to reduce the noise ratio even more and increase the gained power from the amplifier.

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