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Simulation of the Process of LDMOS Transistor Manufacture and Optimizing it to Increase the Current of Work

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Abstract: This study presents the simulation of the process of LDMOS transistor manufacturing by using Silvaco Software and by relying on the ability of calculating the basic parameters of transistor dependencies, focusing on the optimization of the manufacturing process in order to increase the current of research. The simulation of manufacturing process of this type of transistor which is a base for its real manufacturing is of the utmost importance. By using this simulation and reviewing each parameter, we can achieve the optimized manufacturing process by focusing each basic parameter and by paying attention to its required application. In order to design, we first define the construction procedures and the necessary processes using the Athena simulator and then we use the ATLAS device simulator to acquire electrical parameters.

Key words: LDMOS transistor, current operating point, threshold voltage, transconductance, breakdown voltage, cut-off frequency

INTRODUCTION

The application of high power radio frequencies is growing, respectively due to demands for wireless equipment market. Transistors with metal oxide semiconductor field effect have been used in high power radio frequency systems due to their high-speed switching (Nemati *et al*., 2009; Kumar and Bansal, 2012). This type of transistors also has a wide range of maximum voltage rating between 10-1500 V for power application. We require a short channel length and low impurity level in drain area for power applications (Kwon *et al*., 2002). Having low impurity level guarantees the spread of channel into the area in drain association (Haynie *et al*., 2010; Kwon *et al*., 2009; Sithanandam and Kumar, 2009; Son *et al*., 2016; Wu *et al*., 2014). Current depends on different parameters such as gate oxide thickness, threshold voltage width and length of channel and channel voltage. Threshold voltage also depends on the gate oxide thickness and the surface concentration of the channel. Therefore, by changing the thickness of the oxide, implanting channel and adjusting channel length in simulation process, we can increase current without causing change in other default parameters (Ramarao *et al*., 2013; Kim *et al*., 2003; Baliga, 2010; Zhou and Calster, 1994; Kim *et al*., 1999). The breakdown voltage of the device depends on the thickness and resistance of epitaxy layer the shape of the junction and structure of the area in which junction reaches to the semiconductor surface (Minasian, 1983). It is predicted that by increasing the thickness of epitaxy layer and resistance of epitaxy layer, breakdown voltage will increase (Zeghbroeck, 2007; Baliga, 2010).

MATERIALS AND METHODS

In this study, we describe physical structure and manufacturing processes of the Laterally Diffused Metal Oxide Semiconductor (LDMOS) transistor. We determine parameters that affect the device current of research. Also, optimizing the current of the transistor by changing the thickness of oxide, thickness of the epitaxy layer, channel length and impurity concentration of the channel is investigated using the Silvaco device simulator. Furthermore, the threshold voltage, breakdown voltage, transconductance and cut-off frequency of the optimized device are calculated.

RESULTS AND DISCUSSION

Simulation and results: A 100 silicon substrate doped with boron impurity concentration of 10^{14} cm^{-3} was selected at selection stage to build the device. The growth of the epitaxy layer with a thickness of 4.5 μ at 1173 K is

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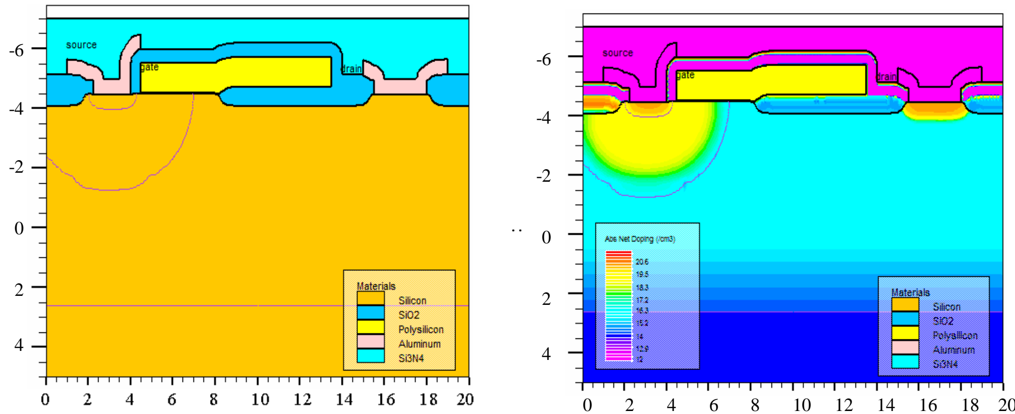

Fig. 1: The structure of LDMOS transistor

performed and next doped with arsenic concentration of 10^{16} cm^{-3}. An extra oxide layer was used for LDMOS transistor known as Field Oxide (FOX) which helps the control of breakdown voltage and on-state resistance of the device. This operation is known as Local Oxidation of Silicon (LOCOS) which is performed after epitaxial processes. After the completion of LOCOS process, we will reach to the process of building the gate. The oxidation of the gate takes place in two stages. For building the gate, first, wafer will be placed into a dried furnace for 10 min at 1308 K and 1 atmosphere pressure. Then a poly-silicon layer with a thickness of 1 μ will be implanted on the substrate, phosphorus atoms with a concentration equal to 3×10^{16} cm^{-3} and 20 keV energy will be added. At this stage, it is time to build the p-type well. To do this, first we will create a window at the desired place for the well and then boron with impurity of 5×10^{15} cm^{-3} and energy equal to 20 keV will be added to build the well. The diffusion process is performed by entering wafer into 1373 K furnace for 150 min in the presence of nitrogen to help the penetration of boron. Doing this, the well building process will finish and time for the second oxidation of the gate will arrive. For this purpose, first the silicon in the desired location will be removed and then a thickness equal to 0.05 μ will be removed from the existed oxide layer (Kim *et al*., 1999). Then a 0.5 μ-thick oxide layer will be added to the device and finally the oxide layer will be removed from those places that source and drain are going to locate there. The second stage of gate oxidation will come to an end by putting the device into a dried furnace with a temperature of 1308 K and 1 atmosphere pressure for 10 min (Zeghbroeck, 2007). After the completion of the second stage, manufacturing process of n-type will take place. For this purpose, first arsenic with an impurity equal to 5×10^{15} cm^{-3} and 50 keV energy will be implanted. The

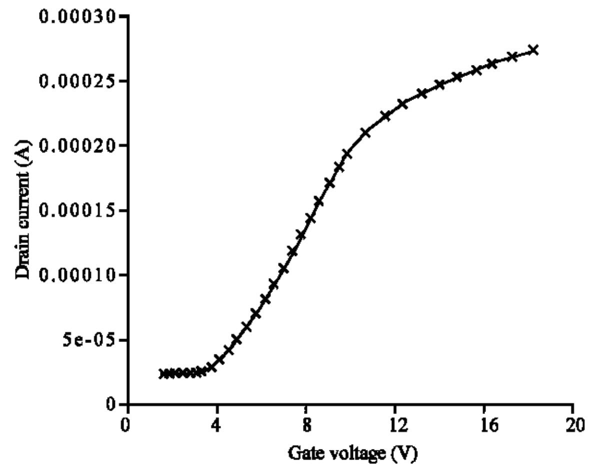

Fig. 2: Drain current versus gate voltage in order to obtain the threshold voltage; ATLAS data IdsVgs.log

diffusion process is done for arsenic penetration. This will be done by putting the device into the 1273 K furnace for 180 min in the presence of nitrogen. Then a 0.03 thick micron layer of extra oxides will be removed. The metallization process will carry out, manufacturing operation will come to an end by isolating the device.

Figure 1 shows structure of the device which is simulated using Athena simulator. Moreover, some of the output parameters of the device are calculated using Atlas simulator. A diagram of drain current versus gate voltage was plotted to obtain threshold-voltage. We assume threshold-voltage as the gate voltage in which drain current reaches at 1 μA. Figure 2 shows that threshold voltage of the device is about 1.8 V.

In order to calculate breakdown voltage of the device, we should change gate voltage to zero. Figure 3

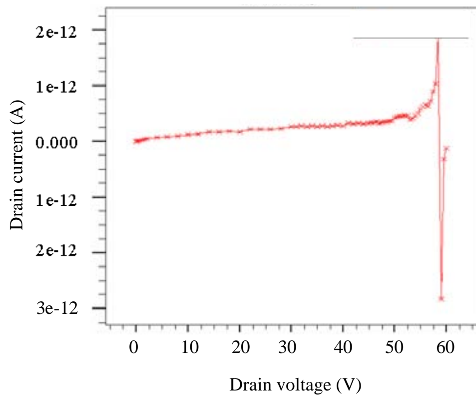

Fig. 3: Drain current versus drain voltage for V_g = 0 in order to obtain breakdown voltage; ATLAS data from break.log

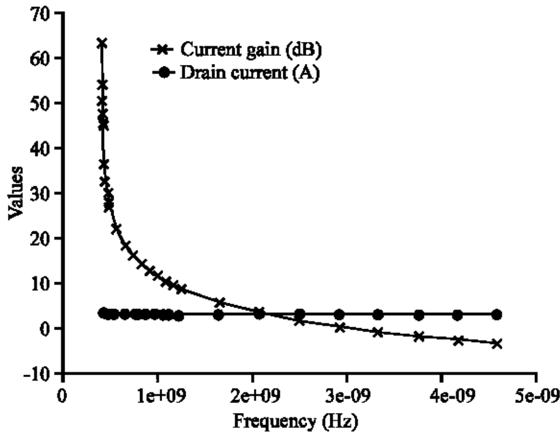

Fig. 4: Current gain diagram in terms of frequency in order to obtain cut-off frequency; ATLAS data from freg.log

shows the drain current versus drain voltage for V_g = 0. As can be seen, the current drain increases with increasing voltage. Also, by paying attention to this figure, it is clear that after a while current starts to diverge and reaches to an unstable situation. The starting point of this instability is known as breakdown voltage. The results obtained from this graph shows that breakdown voltage of the device is about 59 V.

We have drawn current gain diagram in terms of frequency in order to find cut-off frequency. Figure 4 shows current gain versus frequency for the device. The point, in which current gain is equal to zero is known as cut-off frequency. As one can see, the cut-off frequency of the device is about 2 GHz.

We need to calculate the slope of the drain current diagram in terms of gate voltage to calculate transconductance. Figure 5 shows drain current versus gate voltage for the device. We have extracted the slop of

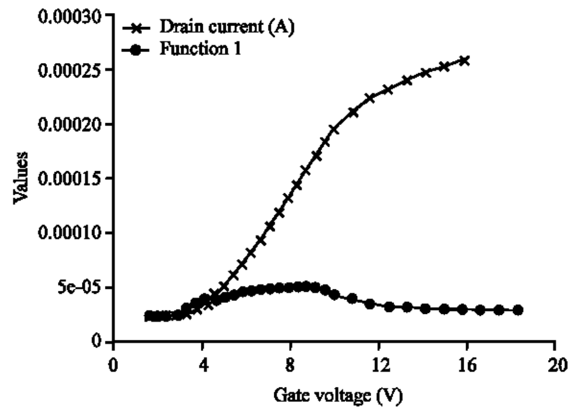

Fig. 5: Current changes diagram in terms of gate voltage changes in order to obtain transconductance; ATLAS data from IdsVgs.log

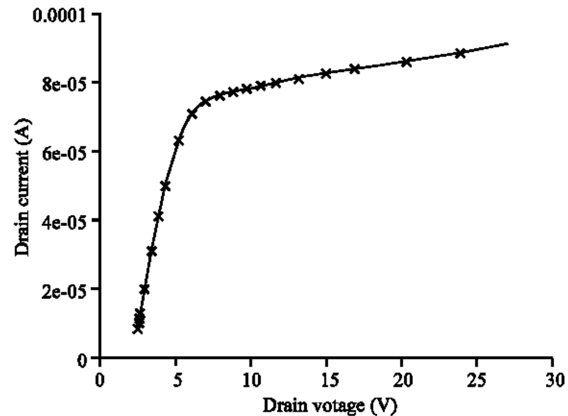

Fig. 6: Drain current versus drain voltage; ATLAS data from IdsVgs.log

the curve as the transconductance of the device. The results show that maximum transconductance of the device is $4\times10^{-6}\ \Omega^{-1}$ corresponding to gate voltage of 8 V. Figure 6 illustrates the drain current versus drain voltage. The current of transistor operating point is obtained from this diagram. According to Fig. 6, drain current of the transistor is 8.3×10^{-5} A corresponding to drain voltage of 8 V. Now, we want to increase the value of transistor current by changing effective factors whereas other parameters such as threshold voltage, breakdown voltage, cut-off frequency and transconductance should not deviate from the desired value. As mentioned before, the value of current depends to various parameters. Therefore, by changing the thickness of oxide, implanting channel and adjusting channel length in simulation process we try to increase current while preserving other presumed parameters which were obtained in the previous stage. First we increase the thickness of the epitaxy layer

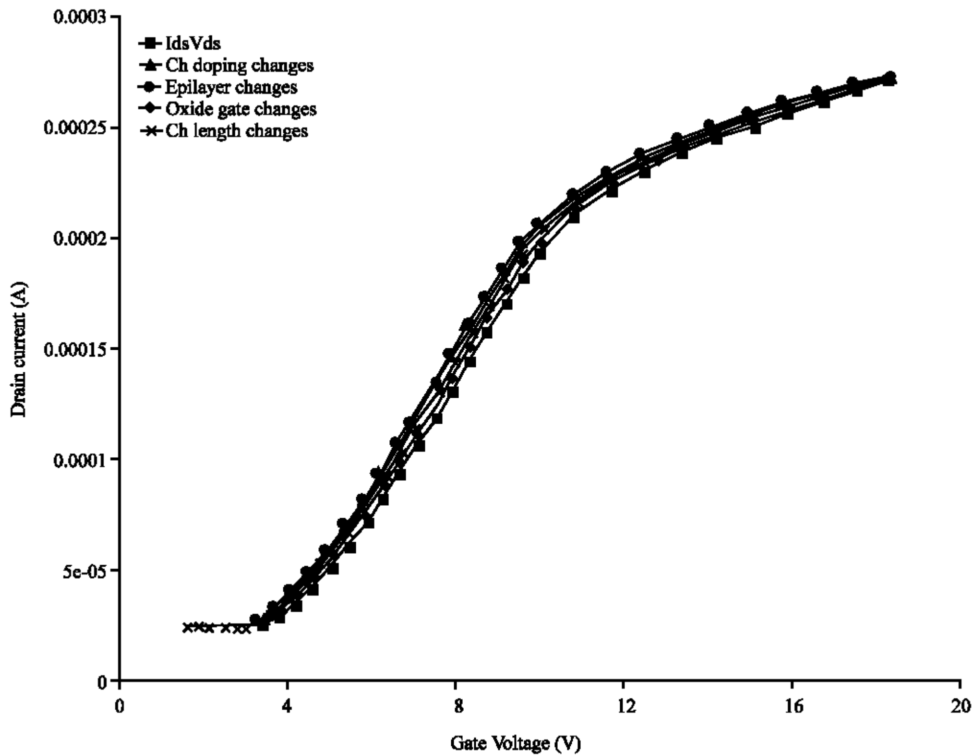

Fig. 7: The results of changes in threshold voltage; ATLAS overlay data from multiple files

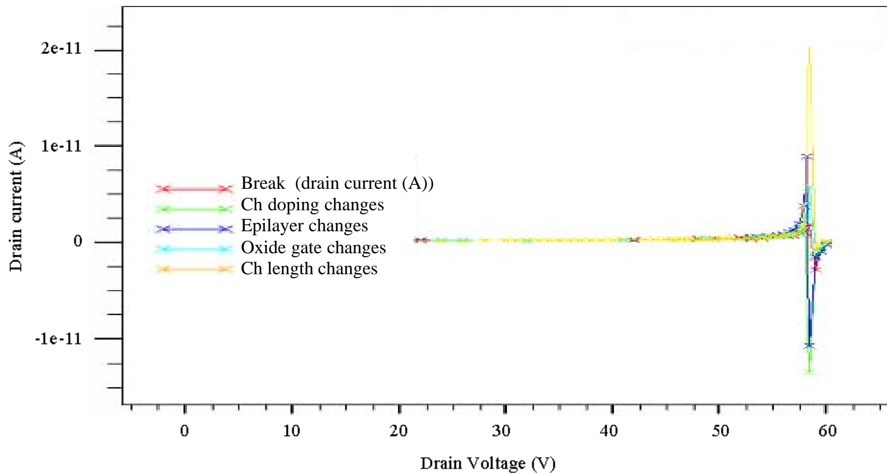

Fig. 8: The results of changes in breakdown voltage; ATLAS overlay data from multiple files

and from 4.5-7 μ. Then, we change the thickness of the gate oxide. As we know, a decrease in gate oxide thickness will cause an increase in the current of the device. We reduce the time of oxidation process from 50-45 min in order to decrease gate oxide thickness. Hence, we can increase current of the device without other parameters of the transistor have changed considerably. The channel length reduction is achieved by reducing time of diffusion boron impurity in stage of the channel formation. Therefore, we reduce channel length by reducing diffusion process time from 150-100 min or even less. Doing this, channel length will decrease and current of the device will increase. Finally, it is to increase boron concentration in the channel formation. This operation causes a reduction in voltage drop across channel, reduction in threshold voltage and hence an increase in current of the device. The obtained results with these changes are shown in Fig. 7-11.

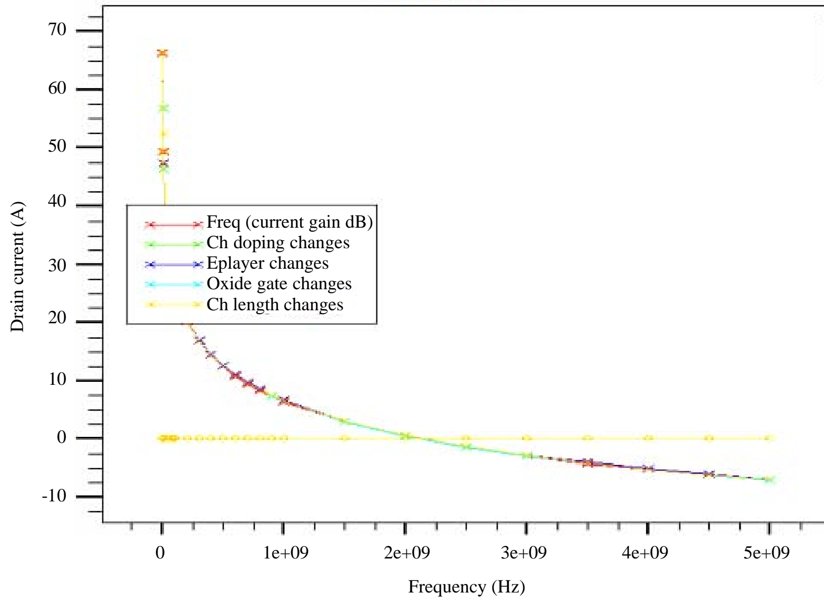

Fig. 9: The results of changes in cut-off frequency; ATLAS overlay data from multiple files

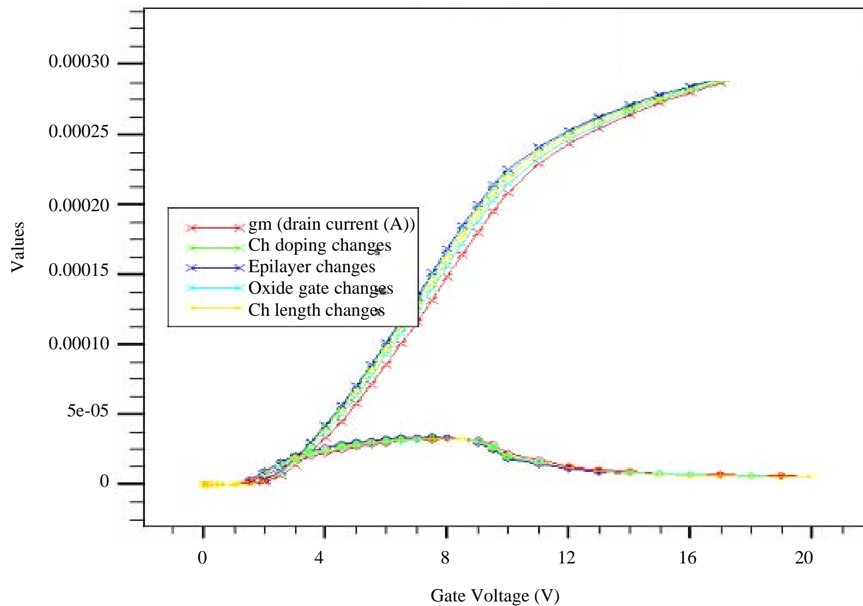

Fig. 10: The results of changes in transconductance; ATLAS overlay data from multiple files

As it is shown in Fig. 7 the mentioned changes in the manufacturing process of the device not have significant effect on threshold voltage of the transistor. According to Fig. 8 after applying changes, breakdown voltage remains nearly constant and is equal to 59 V. Figure 9 illustrates cut-off frequency after applying the changes which is constant and equal to 2 GHz. Figure 10 shows that the transconductance parameter is also constant, its maximum change value is at $V_{gate} = 8$ V and is equal to 4×10^{-6} Ω^{-1}. However, as shown in Fig. 11 by reducing gate oxide thickness, the current of research reached to 9×10^{-5} A in $V_D = 8$ V. On the other hand the current of the transistor increased to 9.4×10^{-5} A corresponding to $V_D = 8$ V by means of reducing channel length. Also, current of the transistor reached to 9.65×10^{-5} A in $V_D = 8$ V by an increase of doping concentration in channel. And finally by increasing the thickness of epitaxy layer, the current of research will

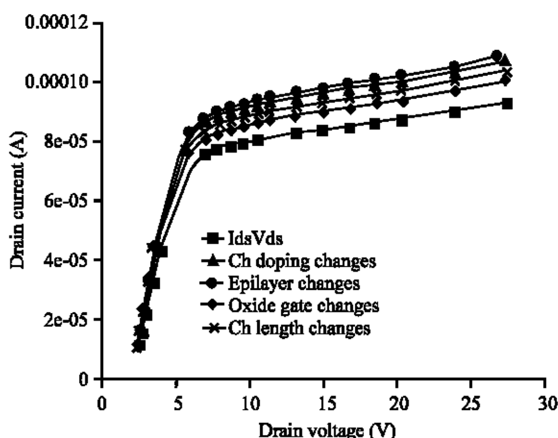

Fig. 11: The results of changes in current operation point; ATLAS overlay data from multiple files

reach to 1×10^{-4} A. Therefore, by optimization of manufacturing processes, we were able to increase current of the transistor compared to the initial structure which had 8.3×10^{-5} A current corresponding to drain voltage of 8 V.

CONCLUSION

In this study, our goal was optimizing of the LDMOS transistor to increase the current of research using numerical simulation. For this purpose, we tried to increase current by changing oxide thickness, implanting channel and adjusting channel length in manufacturing process while preserving other parameters of the transistor. First, we designed an initial structure of LDMOS transistor and calculated important parameters of the device such as threshold voltage, drain current, breakdown voltage, transconductance and cut-off frequency of the transistor. Then, we determined parameters that affect the current of the transistor. We tried by changing of characteristics of the manufacturing processes to increase current of the transistor without considerably changing other parameters of the device. We increased thickness of expitay layer and an increase in the current of the device was seen. Therefore, the current of the transistor has a direct relationship with expitay layer thickness. In the next stage, gate oxide thickness was reduced and an increase in the value of the current was seen. Indeed by decreasing oxide thickness, the channel formation improves and as a result the current of the transistor increase occurred. Therefore, current of work of the device has an indirect relationship with gate oxide thickness. The next parameter was channel length; we reduced channel length by reducing diffusion time of boron impurity in stage of the channel formation. By this doing, an increase in current of the transistor occurred. Therefore, current of the device has an indirect relationship with channel length. The reason for this phenomenon is the fact that a reduction in channel length causes a reduction in resistance of the channel and as a result an increase occurs in the value of current. Finally, the doped concentration of the channel was increased and an increase in the value of the current was seen. Hence, the current of the designed transistor structure has an indirect relationship with channel surface concentration. This phenomenon was predictable, because an increase in channel surface concentration cause an increase in transconductance and a reduction in its voltage drop.

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