

Efficient Code Converter Circuits Design and Implementation in QCA Technology

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Abstract: In this study, we proposed the realization of binary to gray code and gray to the binary code converter using Quantum dot Cellular Automata (QCA). The QCA converters used in a nano electronic circuits and communication applications. The method behind used is based on the interaction of electrons with the quantum dots and utilizes the quantum phenomena. The quantum method may be shown highly complex in next generation integrated circuits. These converters modeled with QCA design software. We have calculated designed comparator area $0.06 \mu\text{m}^2$ with 45 cells for binary to gray code converts and $0.08 \mu\text{m}^2$ area with 55 cells of gray to binary code converter for 4 bit and also designed these converters 8, 16, 32 bits.

Key words: Integrated circuits, converters modeled, calculated, communication applications, complex, designed

INTRODUCTION

CMOS technology is accomplishing its physical limits while at the same time power consumptions and size of circuits are increasing at an alarming pace (Schaller, 1997; Lent *et al.*, 1993; Orlov *et al.*, 1997; Tahoori *et al.*, 2004). In order to reduce these problems in CMOS technology, different new technologies suggested in recent years (Snider *et al.*, 1999; Lakshmi and Athisha, 2010). Present CMOS technology facing problems delay, power consumption, there are the major matters. The problems generated by that technology can overcome by one of the new and emerging technology Quantum Dot Cellular Automata (QCA). The main characters of this technology are logical states representation not in terms of voltage levels alternately represented in terms of logic cells. QCA technology uses less device coulomb interaction to perform the calculation. In IC technology transfer of electrons named as current flow in the devices but in QCA does not involve any transfer of electron in the gates and circuits only charge transformation that's why extremely low power computing even below regular temperature 300°K . QCA designer is the one of layout tool for Quantum-dot Cellular Automata (QCA). The QCA logic gates and QCA circuits are carried out by a group of basic parts are named as QCA cells.

QCA designer basics: A cell is a nanometer structure like a square that has four quantum dots and these quantum dots are placed in four corners of the cells. The quantum

dot is a nanometer sized conductive materials which walled by a nonconductive material (Shahidinejad and Selamat, 2012). So, this structure could drain the electrons in three-dimensional space and if an electron comes into a quantum dot, without enough electrical potential electrons cannot escape from the quantum dot. By injecting two additional electrons into a QCA cell by applying an external potential force, these electrons have might tunneling between quantum dots. In these quantum dots has a polarity and these polarities represent the electrical charge of the quantum dot. External inserted two electrons in the cell have coulombic interaction two different possibilities of arrangements named as negative polarity and positive polarity represents the binary 0 and 1 for the cell. QCA cell four quantum dots together using tunnel junctions and we can control the external input supply of the tunnel junction to lock the position of charge or enable signal that allows controlling the state of QCA cells to binary 0 or 1 position (Mardiris and Karafyllidis, 2010; Sarkar and Mukhopadhyay, 2014; Ahmad *et al.*, 2015).

By applying binary 0 or 1 at one side of the wire another side of the wire same logic levels reached hence this arrangement of QCA cells works as QCA wire. Three different simulation engines are available in latest Version 2.0.3 of QCA design Software.

Digital logic simulator: Which conceives the quantum cell to be either fully polarized or zero polarization also known as a bistable simulator.

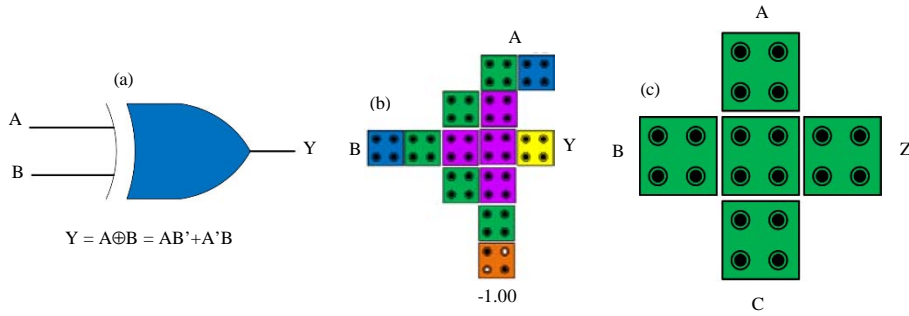


Fig. 1: a) Exclusive OR gate symbol; b) XOR gate QCA design and c) Majority voter QCA design

Non-linear approximation engine: Which uses the nonlinear cell-to-cell response function and stable state condition of the quantum cell in a QCA design (Fig. 1).

Two state Hamiltonian: Which utilizes quantum mechanical model approximation. The main troubles in the design of simulation engine more accurately need but very less practical observation of results less available in QCA design if it is constructed with more number of cells (Srikanth and Sharan, 2015). However, different experimental groups developed small QCA Systems for proof of concept experiments (Misra *et al.*, 2016). As a result, the objective of this cause is to furnish need of future research on QCA designs.

MATERIALS AND METHODS

Proposed designing approach: The primary making block of QCA Circuit is XOR Gate is implemented with a minimum number of cells equal to 12. In the previous work, designed code converters (Liu *et al.*, 2012; Graunke *et al.*, 2005; Ellenbogen and Love, 2000; Das and Bauwens, 2007) implemented with the 3 input majority gate with other logic gates, we are going to design approach employed the two input XOR gate with less number of cells and show output timing graph in 2(d). In this approach, some other functional combinational circuits implemented but here presented only code converters.

Exclusive OR gate: As shown in Fig. 1 input of XOR gate labeled as the A&B output of the gate labeled as Y. Most of the QCA layouts are designed using majority gate (or) voter (MV). This gate is a fundamental logic unit of most of QCA designs. There are different types of majority gate such as 3 input 5 input and 7 input majority gate (Cabe and Das, 2009). But 3 input majority gate is popular gate easy to implement and fundamental logical gates can be designed with 5 cells. $Z = MV(ABC) = AB+BC+CA$ whereas A, B, C are inputs of majority gate and Z as the output of majority gate.

Code converter: Two electronic systems using different codes for same data in that situation code converter are useful. Thus, a code converter is a logic circuit whose inputs are bit patterns representing numbers in one code and whose output is the corresponding representation in a different code. Both electronic systems use different binary codes but code converter generates compatible binary code to both systems. Normally code converters output has many numbers of output circuits.

Binary to Gray code converter: The binary to gray code converter has a regular structure designed using XOR gates, a 4 bit binary to gray code converter circuit is a 4 bit binary input and 4 bit gray output bits all are valid output combinations here no don't care (Chaudhary *et al.*, 2007; Bishnoi *et al.*, 2012; Srivastava *et al.*, 2011). In this study, we are presented 4 bit binary to gray code QCA layout, designed with minimum area. It utilizes a 3 XOR gates and total area is $0.06 \mu m^2$. The expression for the binary to gray code converter as:

- $G3 = \Sigma m(8, 9, 10, 11, 12, 13, 14, 15)$
- $G2 = \Sigma m(4, 5, 6, 7, 8, 9, 10, 11)$
- $G1 = \Sigma m(2, 3, 4, 5, 10, 11, 12, 13)$
- $G0 = \Sigma m(1, 2, 5, 6, 9, 10, 13, 14)$

After simplification minimal expression for the outputs obtained:

- $G3 = B3$
- $G2 = B3 \oplus B2$
- $G1 = B2 \oplus B1$
- $G0 = B1 \oplus B0$

Gray to binary code converter: It shows a circuit diagram of 4 bit gray to binary code converter and shows QCA layout of gray to binary converter. This, 4 bit converter takes 3 clock cycles to convert and in general, it takes n-1 clock cycles to take conversion as the number of bits increases gray to binary conversion time also increases.

Table 1: Area, over all size, number of cells, delay results of proposed QCA converter

Name of the logic circuit	Area (nm)	Overall size (μm^2)	Cells	Delay (Clk)	Number of clock phases
Binary to gray code converter (bit)					
4	370.00×172.00	0.06	45	½	2
8	873.88×175.88	0.15	107	½	2
16	1816.88×183.30	0.33	227	½	2
32	1939.00×340.89	0.66	477	½	2
Gray to binary code converter (bit)					
4	355.88×224.89	0.08	55	1	4
8	755.88×224.89	0.17	122	1	4
16	919.39×404.89	0.37	265	1	4
32	991.35×784.89	0.78	550	1	4

The following equation is used for a gray to binary code conversion (Table 1):

- $B_3 = G_3$
- $B_2 = G_3 \oplus G_2$
- $B_1 = B_2 \oplus G_1$
- $B_0 = B_1 \oplus G_0$

RESULTS AND DISCUSISON

Simulation results and analysis report: In this proposed, code converters design utilized basic gate used XOR gate designed with a minimum number of cells and zero majority gates. We have designed the code converters of 4, 8, 16 and 32 bit with less area and less number of cells. The binary to gray code converter and gray to binary converter QCA layout uses zero crossovers. The proposed binary to gray takes 2 clock phases for any number of bits and it takes $0.06 \mu\text{m}^2$ area with 45 number of cells with ½ clock delay for 4 bit binary to gray converter. Whereas gray to binary converter for 4 bit operation takes $0.08 \mu\text{m}^2$ with 55 cells, 1 clock phase taken. Remaining designed converters 8, 16 bit and 32 bit details listed. It is expected that the newly designed scheme for QCA of code converter introduced in this study significant improvement in the nano-electronic circuits and reduces area and delay of future QCA architectures.

CONCLUSION

Majority gate is one of basic QCA gate with inverter gate together possible to design of XOR gate and and or gate by applying one input of majority gate is -1 or 1 polarization to the majority gate. We designed modified majority gate work as a XOR gate or full adder with a minimum number of cells compared to earlier QCA layouts. These proposed circuits distinguish oneself earlier reported designs in terms of overall size, logic gate count, delay and number of cells. Moreover, the main advantage of the presented implementation is in asingle

layer with zero cross over the wiring. This research study can be carried to design the quantum cellular automata layouts in nano-electronic applications.

REFERENCES

Ahmad, F., P.Z. Ahmad and G.M.D. Bhat, 2015. Design and analysis of odd-and even-parity generators and checkers using Quantum-dot Cellular Automata (QCA). Proceedings of the 2nd International Conference on Computing for Sustainable Global Development (INDIACom), March 11-13, 2015, IEEE, New Delhi, India, ISBN:978-9-3805-4415-1, pp: 187-194.

Bishnoi, B., M. Giridhar, B. Ghosh and M. Nagaraju, 2012. Ripple carry adder using five input majority gates. Proceedings of the 2012 IEEE International Conference on Electron Devices and Solid State Circuit (EDSSC'12), December 3-5, 2012, IEEE, Bangkok, Thailand, ISBN:978-1-4673-5694-7, pp: 1-4.

Cabe, A.C. and S. Das, 2009. Performance simulation and analysis of a CMOS/nano hybrid nanoprocessor system. *Nanotechnol.*, 20: 1-12.

Chaudhary, A., D.Z. Chen, X.S. Hu, M.T. Niemier and R. Ravichandran *et al.*, 2007. Fabricatable interconnect and molecular QCA circuits. *IEEE. Tran. Comput. Aided Design Integr. Circuits Syst.*, 26: 1978-1991.

Das, S. and M.F. Bauwens, 2007. Clocking nanocircuits for nanocomputers and other nanoelectronic systems. Proceedings of the IEEE International Symposium on Nanoscale Architectures (NANOSARCH'07), October 21-22, 2007, IEEE, San Jose, California, ISBN:978-1-4244-1790-2, pp: 123-128.

Ellenbogen, J.C. and J.C. Love, 2000. Architectures for molecular electronic computers. I. Logic structures and an adder designed from molecular electronic diodes. *Proc. IEEE.*, 88: 386-426.

Graunke, C.R., D.I. Wheeler, D. Tougaw and J.D. Will, 2005. Implementation of a crossbar network using quantum-dot cellular automata. *IEEE. Trans. Nanotechnol.*, 4: 435-440.

- Lakshmi, S.K. and G. Athisha, 2010. Efficient design of logical structures and functions using Nanotechnology based quantum dot cellular automata design. *Int. J. Comput. Appl.*, 3: 35-42.
- Lent, C.S., P.D. Tougaw, W. Porod and G.H. Bernstein, 1993. Quantum cellular automata. *Nanotechnol.*, 4: 49-57.
- Liu, W., S. Srivastava, L. Lu, M. O'Neill and E.E. Swartzlander, 2012. Are QCA cryptographic circuits resistant to power analysis attack?. *IEEE. Trans. Nanotechnol.*, 11: 1239-1251.
- Mardiris, V.A. and I.G. Karafyllidis, 2010. Design and simulation of modular $2n$ to 1 Quantum-dot Cellular Automata (QCA) multiplexers. *Intl. J. Circuit Theory Appl.*, 38: 771-785.
- Misra, N.K., S. Wairya and V.K. Singh, 2016. Optimized Approach for Reversible Code Converters using Quantum Dot Cellular Automata. In: *Frontiers in Intelligent Computing: Theory and Applications (FICTA)*, Das, S., T. Pal, S. Kar, S. Satapathy and J. Mandal (Eds.). Springer, India, ISBN:978-81-322-2693-2, pp: 367-378.
- Orlov, A., G. Amlani Bernstein, C. Lent and G. Snider, 1997. Realization of a functional cell for quantum-dot cellular automata. *Science*, 277: 928-930.
- Sarkar, A. and D. Mukhopadhyay, 2014. Improved quantum dot cellular automata 4: 1 multiplexer circuit unit. *SOP. Trans. Nano Technol.*, 1: 37-44.
- Schaller, R.R., 1997. Moore's law: Past, present and future. *IEEE. Spectr.*, 34: 52-59.
- Shahidinejad, A. and A. Selamat, 2012. Design of first adder/subtractor using quantum-dot cellular automata. *Adv. Mater. Res.*, 403: 3392-3397.
- Snider, G.L., A.O. Orlov, I. Amlani, X. Zuo and G.H. Bernstein *et al.*, 1999. Quantum-dot cellular automata. *J. Vac. Sci. Technol.*, 17: 1394-1398.
- Srikanth, P.C. and P. Sharan, 2015. A novel quantum dot cellular automata for parity bit generator and parity checker. *Intl. J. Emerging Technol. Comput. Sci. Electron.*, 14: 107-111.
- Srivastava, S., A. Asthana, S. Bhanja and S. Sarkar, 2011. QCAPro-an error-power estimation tool for QCA circuit design. *Proceedings of the 2011 IEEE International Symposium on Circuits and Systems (ISCAS)*, May 15-18, 2011, IEEE, New Delhi, India, ISBN:978-1-4244-9473-6, pp: 2377-2380.
- Tahoori, M.B., M. Momenzadeh, J. Huang and F. Lombardi, 2004. Defects and faults in quantum cellular automata at nano scale. *Proceedings of the 22nd IEEE Symposium on VLSI Test*, April 25-29, 2004, IEEE, Napa County, California, pp: 291-296.