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Design of Low Pass FIR Filter for FPGA Implementation Using Xilinx System Generator

[1, 2]Jamshid M. Basheer and [2]V. Murugesh
[1]Manonmaniam Sundaranar University, Tirunelveli, India
[2]Department of Computer Engineering, College of Computer Science,
King Khalid University, Abha, Kingdom of Saudi Arabia

Abstract: Noise reduction in images or signals is the important process in image processing and signal processing applications. Most of the cases, filter is used to eliminate the noise in the images. Different filters are available in the image processing for noise reduction. In this study designed a 19-tap low pass FIR with reduced MAC unit. The filter is efficiently designed by using MATLAB Simulink and Xilinx system generator. Reduced MAC unit reduces the hardware utilization of the device. The noisy input signal is applied into the filter for noise elimination. After the completing the Simulink simulation, start to generating the verilog HDL code using Xilinx system generator. In the time of code generation the device specifications are selected for Field Programmable Gate Array (FPGA) implementation. System generator is used to implement the filter into the FPGA hardware. The device utilization and timing summary of the filter can be evaluated using Xilinx 12.4 simulation tool.

Key words: Filter, MATLAB Simulink, Xilinx system generator, Field Programmable Gate Array (FPGA), Multiplication and Accumulation Unit (MAC), device

INTRODUCTION

In any signal processing element, filter is one of the main devices used to remove the unwanted noise signals. The basic function of the filter is to allow the selective signals and stop the particular signals. A filter system consists of analog to digital converter used to sample the input signals. It mainly classified into analog filter and digital filter. Analog filter is used in the electronic circuits to reduce the noise and to enhance the audio and video signals. Main drawback of the analog filter is follows, at high frequencies analog filtering is not possible. Also, it gives less accuracy and variations. Because of the drawbacks circuit prefer digital filter, it overcome the drawback of analog filter.

Digital filter process the sampled signals. Digital filter consists of and analog to digital converter, it is used to convert analog signal to digital signal. Field Programmable Gate Array (FPGA) is used as a processor to perform the mathematical operation of sampled data. Finite Impulse Response (FIR) filter and Infinite Impulse Response (IIR) filter are the 2 types of digital filter widely used in the processor. FIR filter is also called as Recursive filter. It contains feedback the latest output is send back to the input for processing the present state input. The word recursive means running back. Adder, multiplier and delay unit are the components used in the FIR filter. The components are improving the performance of the FIR filter. Infinite Impulse Response (IIR) filter is another type of digital filter, it have higher frequency response than FIR filter. One of the main drawbacks is phase characteristics. IIR does not have linear phase characteristics that are the reason IIR filter is not preferred for filtering operations. If suppose the circuit does not concentrate the phase characteristics means, IIR is the best to give the perfect output. Noise characteristics is difficult to model in the IIR filter, the model is easy in the FIR filter. FIR filter is easy and simple to implement (Singh and Saini, 2017).

Literature review: Nair *et al.* (2017) explained the operation of digital FIR and IIR filters. Normally filter is a time based design, it uses a multiplier for performing the mathematical operation. This operation same in IIR filter to perform the calculations. The simplicity of the architecture is used in many digital circuits. Khan *et al.* (2017) proposed the multi-output first order digital filter. The filter structure consists of delay element, adders and multipliers. In a first order structure the zero input and the overflow is completely eliminated. It is perfectly suitable for VLSI implementation (Naik and Gupta, 2017).

Corresponding Author: Jamshid M. Basheer, Department of Computer Engineering, College of Computer Science, King Khalid University, Abha, Kingdom of Saudi Arabia

Kumar and Rabi (2016) described the low pass filter with FIR. The operating frequency of the filter is 15.37 MHz clock frequency, it realizes the cascaded structure of an FIR and IIR filters. The MAC unit of the FIR filter is built by using carry select adder with efficient multiplier circuit. The shift register in the circuit is used in the circuit for shifting the data to the next stage for further processing. Dempster explained the concept of VLSI digital filter complexity using the fixed point binary multiplier.

Mathew and Mehra (2017) described the concept of hardware optimization method based on the minimum adder CSD multiplier. This technique reduces the hardware requirement and latency of the circuit. In order to increase the order of the filter, the coefficients of the filter are shortened to B bits. Order of the filter can be increased by adding delay element to the circuit and to decreasing the bits by reducing the adders in the filter circuit. So, the filter can be easily adjustable to produce the output of the filter.

Singh and Saini (2017) designed a 1 bit full adder using hybrid CMOS design. The full adder design with XNOR gate uses clock gating to minimize the power consumption of the circuit. Researcher proposed the 24 transistor based full adder, it is operated at 1.8 V power supply. Performance of the proposed full adder is compared with various full adders and find out the power delay product. Xu, proposed an algorithm to design a low complexity FIR filters. The fixed point FIR filters decoupled the filter coefficients.

Park proposed the low power and high performance FIR filter, it's depends on Computation Sharing Multiplier (CSHM). This multiplier focuses the vector-scalar products. Multiplier uses a new carry select adder and flip-flops to enhance the power and the performance of the circuit. Main components of the FIR filter implementation is adders and flip flops. So, the proposed CSHM is to achieve low power and high performance of the FIR filter.

MATERIALS AND METHODS

Discrete Wavelet Transform (DWT): Discrete wavelet transform is the process of the wavelets is discretely sampled. Advantage over fast fourier transform is it captures both the frequency and location, location is mentioned in time. Wavelets are used to avoid or reduce noise in the 2D signals. In most cases DWT is used to remove the unwanted white Gaussian noise from the noisy image. Filters are often used in the noise reduction process (Fig. 1).

DWT represents the data in the form of low pass coefficient and high pass coefficients. The input data from the image is entered into the low pass and high pass filter. After the processing of the data, the output data from the filter is collected, the output data is down sampled by 2. Output contains two types of coefficients, from low pass filter is called as average coefficient and the output from high pass filter is called as detailed coefficient. Likewise, 2D DWT the input data is processed in 2 directions, one is row wise and another one is column wise. The process is start like 1D DWT process. After the results from 1D DWT, the samples again divided into two sets and continue the process is same as one dimensional DWT (Fig. 2). The output data have four set of coefficients named as LL, HL, LH and HH. L represents low pass filter

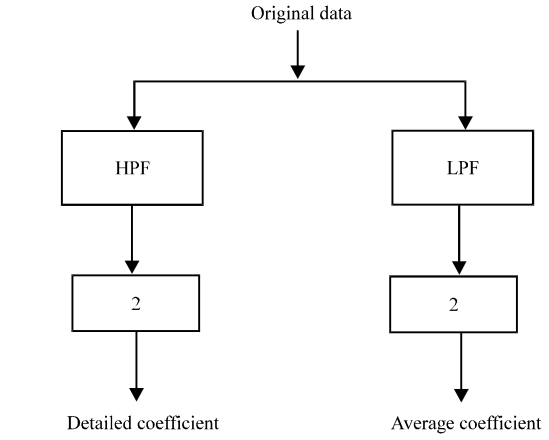

Fig. 1: One-dimensional DWT

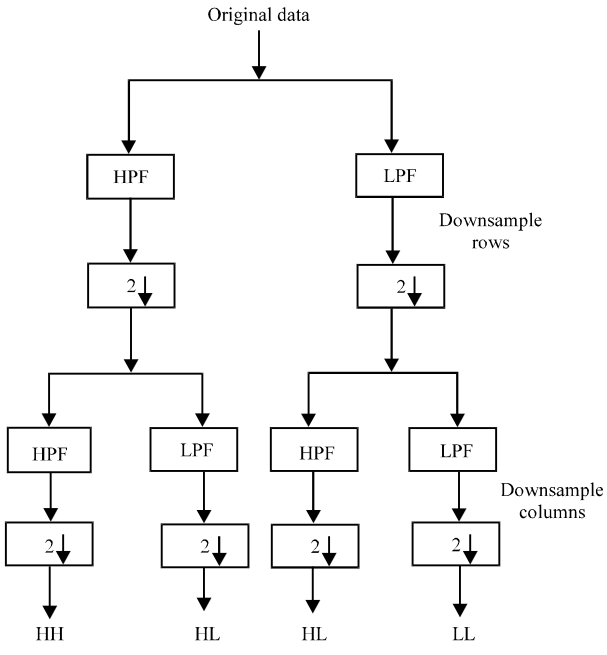

Fig. 2: Two-dimensional DWT

signal and H represents high pass filter signal. The data from the filters are down sampled by 2. The sampling is done by both the row and columns.

Filter design for noise reduction: Different filters are available to reduce the noise in the signals and images. FIR filter and IIR filter are the most commonly used filters. Other name of the FIR filter is recursive and the IIR filter is non-recursive filter. FIR filter contain finite set of input and outputs. The output of the previous stages is sending to process the filtering operation. The feedback input is stored in the processor memory. The input value of the FIR filter is represented as x_n, x_{n-1}, x_{n-2} likewise the feedback input is represented as y_{n-1}, y_{n-2}.

The input and output relation of the linear time invariant Finite impulse response filter is represented as Eq. 1:

$$z(n) = \sum_{k=0}^{N-1} C_k \, x(n-k) \qquad (1)$$

Where:

$z(n)$ = The output signal
$x(n)$ = The input signal
c_k = The filter coefficients

The basic characteristics of the FIR filter are linear phase, higher order and good stability. The digital filter shown in Fig. 3, operates only the discrete time signal. The wavelet samples are entered into the filter for removing the noise. Add Gaussian noise to the samples for processing the image wavelets.

Filter design using matlab system generator: The Gaussian noise filter is designed by using MATLAB Simulink system generator. It automatically creates the verilog file or VHDL file. FPGA device selection, speed and preferred languages are selected by users. The simulink model of 19-tap FIR low pass filter shown in Fig. 4. Number of tap increases in the filter achieves greater noise reduction in the images or signals. It

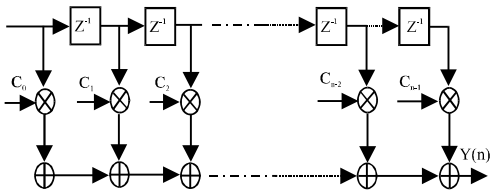

Fig. 3: Structure of digital filter

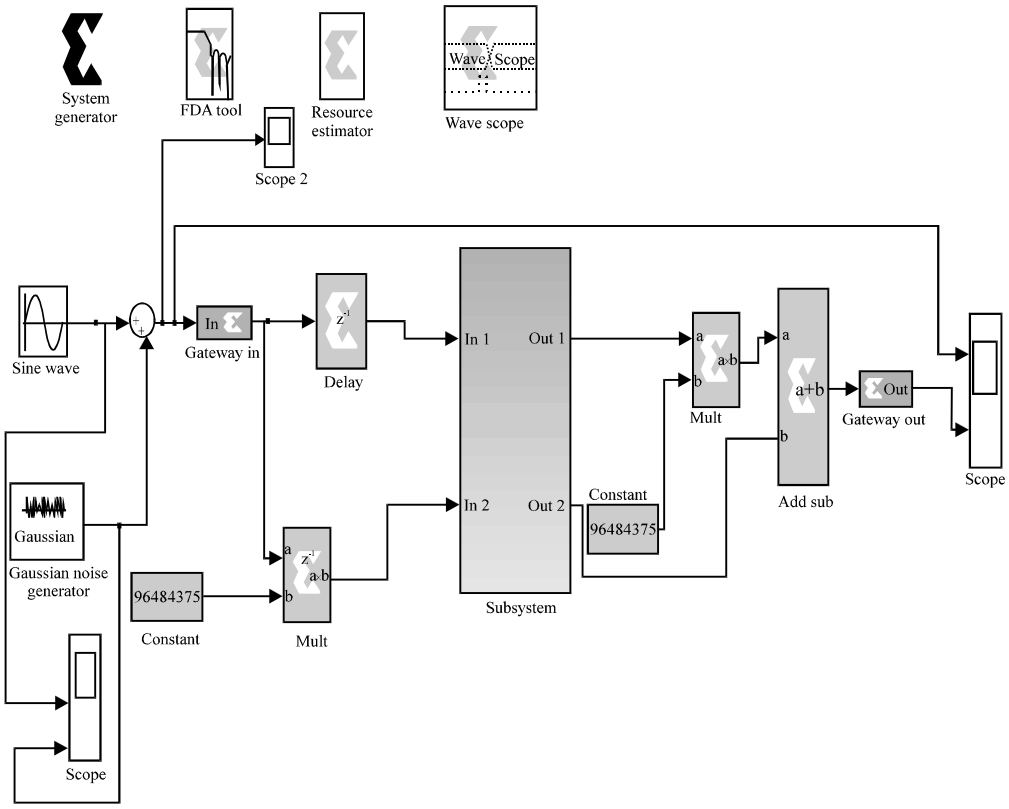

Fig. 4: Simulink model of 19-tap filter design with reduced MAC unit

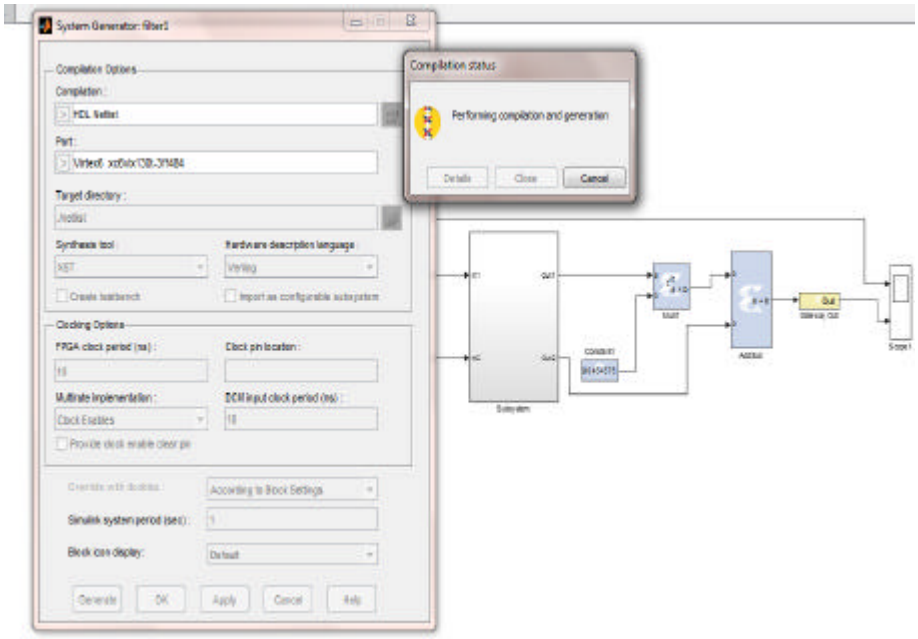

Fig. 5: Generating verilog HDL code for designed filter

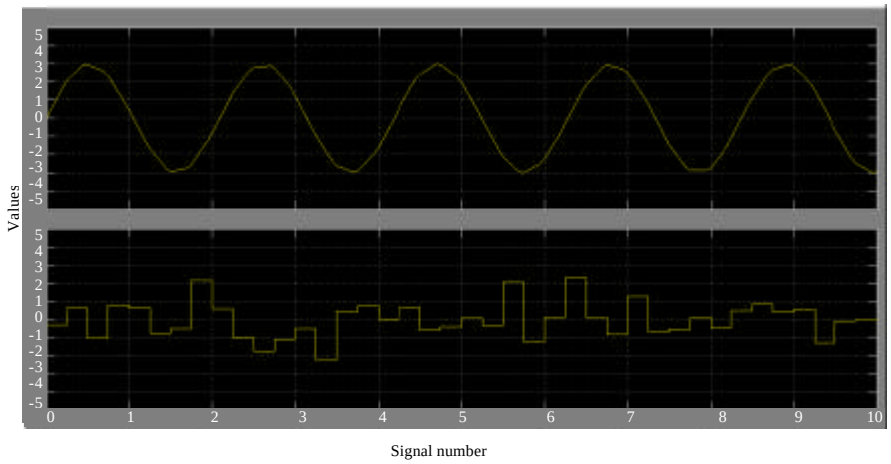

Fig. 6: Clearly show the input signal and the Gaussian noise signal, the added signal is enter into the further filtering process.

consists of original signal and noise signal both the signals are added and start the next process. Xilinx components are present in-between the gateway in and gateway out. MAC unit is present in the system to perform the mathematical operation of the filter (Table 1).

Figure 5 and 6, the code generation step for designed filter. The device specification for code generation is Virtex-6, xc6vlx130, speed3. After generating the verilog code, it is implemented into the selected FPGA device for analyze the LUT and slices utilization. Also, find the time taken for execution of code in the FPGA device. This method is very easy to implement the code into the hardware for real time applications.

Table 1: Comparison of low pass FIR filter with conventional MAC and reduced MAC unit

Parameters	FIR with conventional MAC	FIR with reduced MAC
Number of slice register	305	241
Number of IOs	69	66
Number of bonded IOs	68	65
Delay (NS)	0.428	0.418

```
Selected Device : 6vlx130tff484-3


Slice Logic Utilization:
 Number of Slice Registers:             241  out of  160000     0%

Slice Logic Distribution:
 Number of LUT Flip Flop pairs used:    241
   Number with an unused Flip Flop:       0  out of    241     0%
   Number with an unused LUT:           241  out of    241   100%
   Number of fully used LUT-FF pairs:     0  out of    241     0%
   Number of unique control sets:         2

IO Utilization:
 Number of IOs:                          66
 Number of bonded IOBs:                  65  out of    240    27%

Specific Feature Utilization:
 Number of BUFG/BUFGCTRLs:               1  out of     32     3%
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Fig. 7: Logic utilization of filter on FPGA device

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Timing Summary:
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Speed Grade: -3

   Minimum period: 0.559ns (Maximum Frequency: 1787.949MHz)
   Minimum input arrival time before clock: 0.282ns
   Maximum output required time after clock: 0.559ns
   Maximum combinational path delay: 0.428ns
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Fig. 8: Timing summary of the designed filter in FPGA

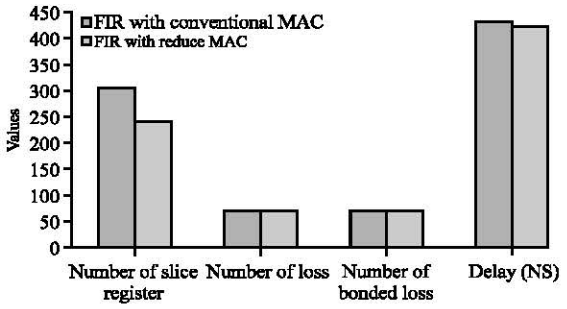

Fig. 9: Camparison between conventional and reduced MAC

RESULTS AND DISCUSSION

The simulation results are taken from MATLAB Simulink and Xilinx ISE simulation tools. The filter was designed using simulink and the code is generated by using system generator. Finally, the generated code is implemented into the Xilinx ISE tool for find out the hardware utilization summary and delay time.

Figure 7 and 8 show the FPGA device logic utilization and timing summary of the designed filter. This information is useful for hardware implementation. Based on the logic information the user can implement the device for noise reduction in image, signal, etc. (Fig. 9).

CONCLUSION

FPGA hardware implementation of the filter with reduced MAC was done using Xilinx system generator. It is easy process to implementing the design into the hardware, also, find the device utilization summary for reducing the complexity of the device. Time delay is also measured for efficient usage of hardware. The designed filter implemented into Virtex- 6 FPGA platform based on a state machine. MAC unit present inside the filter perform the mathematical operation during the computation of noise reduction. The simulation of the designed filter was measured using Simulink Software after the verification, generated the verilog HDL code for implementation. This can be effectively reducing the noise in the image or signals.

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