Journal of Engineering and Applied Sciences 12 (Special Issue 12): 9425-9429, 2017
ISSN: 1816-949X

Low Power Multiplier and Divider Circuit Using Full Swing Gate Diffusion Input

[1]Sujatha Hiremath and [2]Deepali Koppad
[1]Department of ECE, RVCE, Bengaluru, India
[2]Department of ECE, PESIT, Bengaluru, India

Abstract: As the number of transistors are increasing day by day, it is important to reduce the power consumption of the overall system. Hence, low power techniques are becoming more important and useful in a system design. It is necessary to reduce the power dissipation for long life, more reliable and high performance systems. Gate Diffusion Input (GDI) is one of the low power technique to achieve less power dissipation. GDI cell consists of only two transistor nMOS and pMOS. The number of transistors required to implement basic gates are less than using CMOS logic. There are three inputs, one is at the gate of both the transistor, other two are from diffusion of nMOS and pMOS. Hence, it is named as gate diffusion input. Output is taken from drain/source of both the transistors. GDI technique also has the advantage of high speed, less area. But the limitation of GDI is the output does not have a full swing of logic 1 and logic 0. In this study, basic GDI cell is modified to get a full swing of logic 1 and 0. This modified GDI cell is used to implement the arithmetic circuits such as adder, multiplier and divider circuits. Comparison results of modified full swing GDI, CMOS circuits are shown. These results are obtained from Cadence Virtuoso based on 45 nm technology with the supply voltage of 1.2 V.

Key words: Low power, full adder, multiplier, divider, gate diffusion input, results

INTRODUCTION

For high performance of the system as the complexity of the electronic circuits increase, the power dissipation becomes one of the crucial factors that need to be considered. Hence, there is a need for a design that reduces the complexity and also helps to reduce the power dissipation. There are many techniques which are used to reduce the both dynamic power dissipation and static power dissipation without degrading the design performance.

Gate diffusion input is one of the low power technique used to reduce the overall power dissipation of the digital design. The basic GDI cell consists of only two transistors such as nMOS and pMOS with three inputs. With the help of this GDI cell basic logic functions can be implemented. The basic GDI cell has 3 inputs named as G, P and N as shown in Fig. 1 (Morgenshtein *et al*., 2002). Using these 3 inputs any digital circuit can be designed. Since, nMOS produces weak logic 1 and pMOS gives weak logic 0 (Neil and Kamran, 1993), the output will be degraded whenever the input passes through these transistors. Hence, the limitation of the GDI technique is reduced swing at the output.

In this study, degraded swing will be improved by using additional transistors to achieve full swing voltage at the output. Each GDI gate is modified to obtain full swing with the help of additional transistors. Adder, multiplier and divider circuits are important in arithmetic circuits. These circuits are implemented using GDI cell with improved swing. To implement the multiplier and divider full adder is the basic circuit. Full adder circuit is implemented using XOR and OR gate using full swing GDI

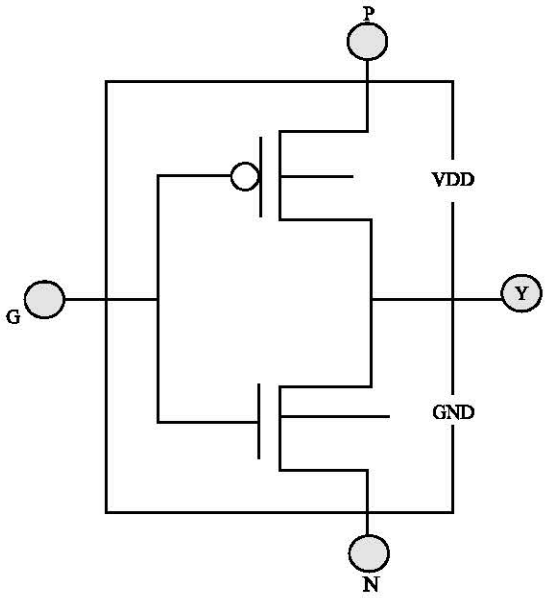

Fig. 1: Basic GDI cell

Corresponding Author: Deepali Koppad, Department of ECE, RVCE, Bengaluru, India

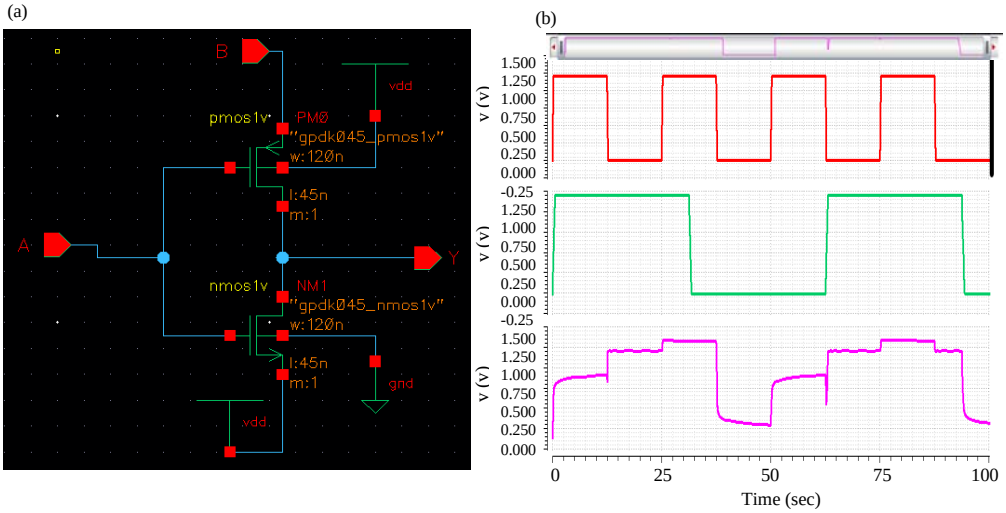

Fig 2: a) OR gate using GDI (2 Tr) and b) Waveform of GDI OR gate (2 Tr)

logic. The 1 bit full adder is implemented using GDI with 10 transistor (Singh and Kumar, 1892) but it gives weak logic 0 and 1. Hence, it is modified to obtain full swing with additional 7 transistor. But the average power of full swing adder is still lesser than CMOS full adder.

Full adder is the basic block for the arithmetic circuits such as divider and multiplier. Similarly, XOR or AND gates are important for adder circuit. Hence, designing basic gates such as XOR or AND with less power dissipation provides reduced overall power dissipation of the circuit. The basic GDI cell gives very less power consumption but voltage swing will be reduced at the output. Hence, modified full swing GDI cells are used with an additional transistors but average power is still lesser than CMOS logic.

The 4×4 Vedic multiplier and 7×4 divider circuit is implemented using full adder. Comparison of full swing GDI and CMOS designs for arithmetic circuits are performed using Cadence Virtuoso based on 45 nm technology.

GDI basic functions: The GDI three inputs are used implement AND or XOR, gate. Using these 3 inputs it is easy to implement any Boolean expression with less number of transistors. For example to implement OR gate in CMOS, the number of transistors required are six. Using GDI technique only two transistors are required as shown in Fig. 2a. G input of GDI cell is used as a A input of OR gate P input as a B. N input is connected to V_{dd} to get OR expression. The output Y = A'B+A.1 = A'B+A = A+B. But the output of this circuit provides degraded voltage. Considering an example: when A = 0, B = 0, then pMOS conducts and passes B input, i.e., logic 0 to output. Since, pMOS does not pass good logic 0, the output will not go to 0 V. Similarly, when A = 1, nMOS turns on and passes Vdd to the output. Since, nMOS produces weak logic 1, hence, the output is weak logic 1. The simulated waveform of OR gate is shown in Fig 2b.

Table 1: GDI AND, OR, XOR gate output

A	B	OR output	OR (2 Tr)	AND (2Tr)	XOR (4Tr)
0	0	0	Weak 0	Weak 0	Weak 0
0	1	1	1	Weak 0	1
1	0	1	Weak 1	0	Weak 1
1	1	1	Weak 1	Weak 1	0

Using additional 3 transistor both logic 0 and 1 are improved at the output. The proposed full swing GDI OR gate is as shown in Fig 3a. The simulated output is shown in Fig 3b. The output of proposed full swing OR gate output is at strong logic 1 and 0.

Similarly GDI AND gate can be designed using only 2 transistors as shown in Fig 4a. Simulated waveform of GDI AND gate is shown in Fig 4b.

To overcome the degraded output voltage, additional 3 transistors are used which compensate the reduced voltage swing at the output. The modified full swing GDI AND gate with 5 transistor and its simulation waveform is shown in Fig. 5a, b, respectively.

Similarly , XOR with 4 transistor is modified to get full swing using additional 2 transistor (Koppad and Hiremath, 2016).The output of GDI OR, AND gate with two transistor and XOR with 4 transistor output is listed in Table 1.

Use of additional transistors helped to improve the output swing of GDI gates as equivalent to the CMOS logic output. The average power of the proposed full swing GDI gates are still lesser than the CMOS gates. The comparison of average power of proposed full swing

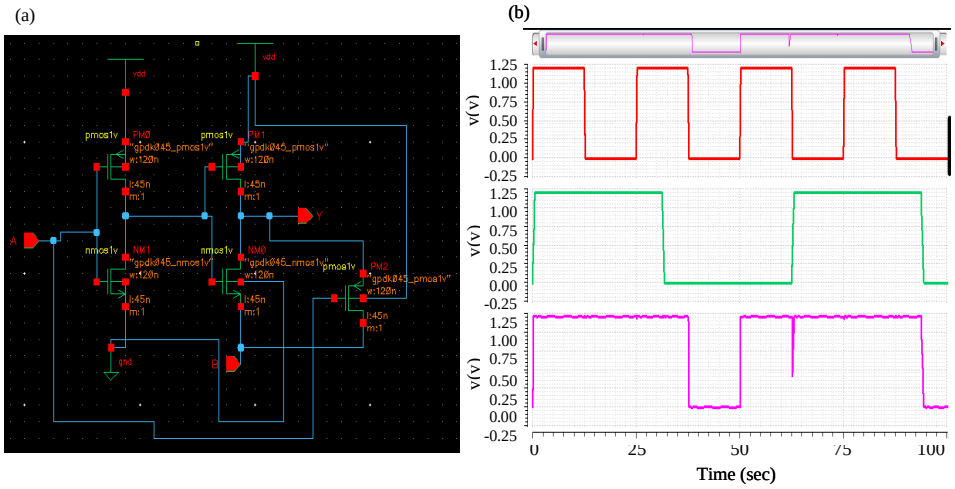

Fig. 3: a) OR gate using full swing GDI (proposed 5 Tr) and b) Wave form of full swing GDI OR gate (proposed 5 Tr)

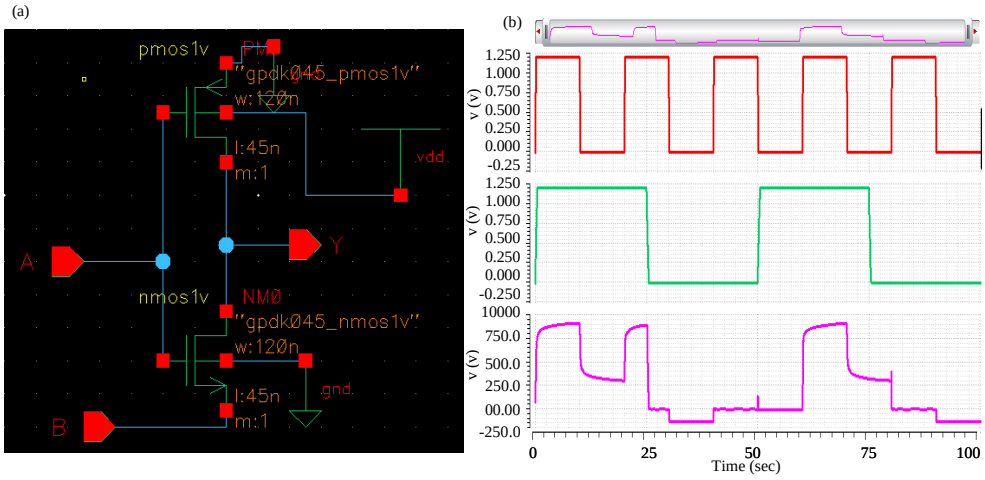

Fig. 4: a) GDI AND gate (2 Tr) and b) Wave form of GDI AND gate (2 Tr)

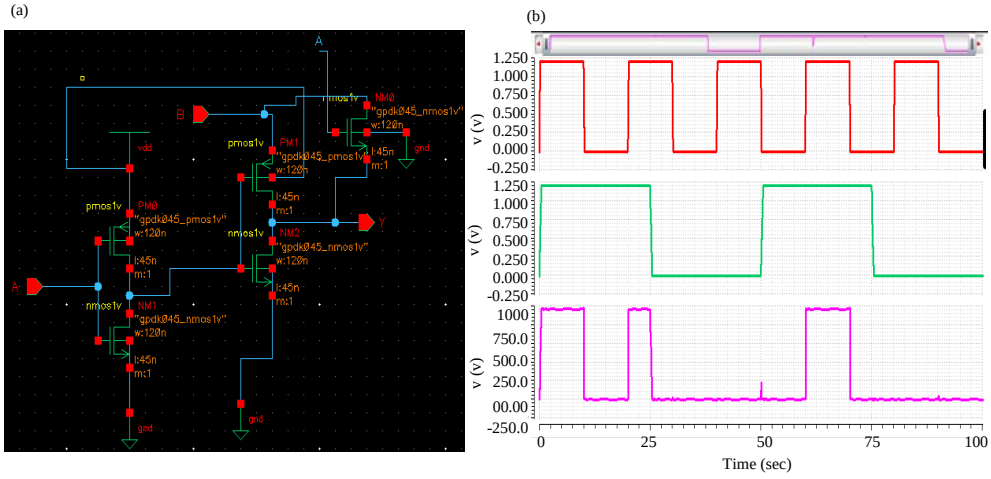

Fig. 5: a) Full swing GDI AND gate (proposed 5 Tr) and b) Waveform of full swing GDI AND gate (proposed 5 Tr)

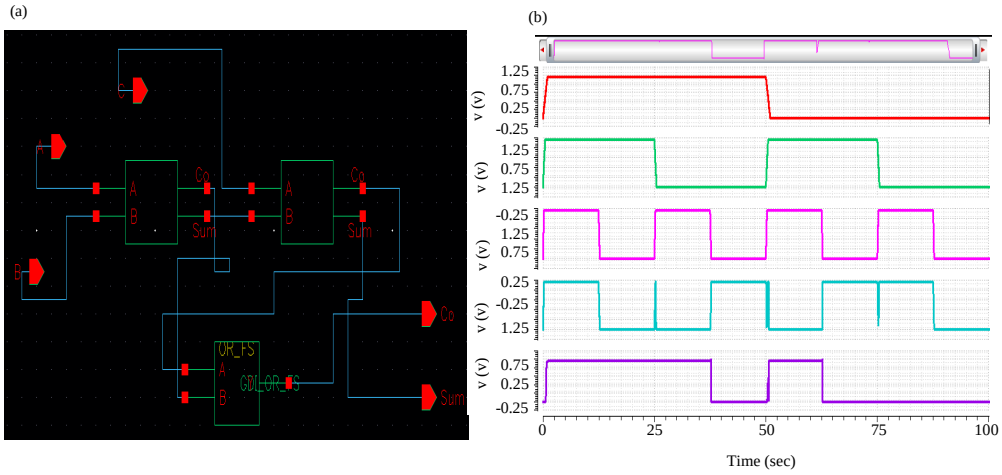

Fig. 6: a) Full swing GDI adder and b) Waveform of full swing GDI adder

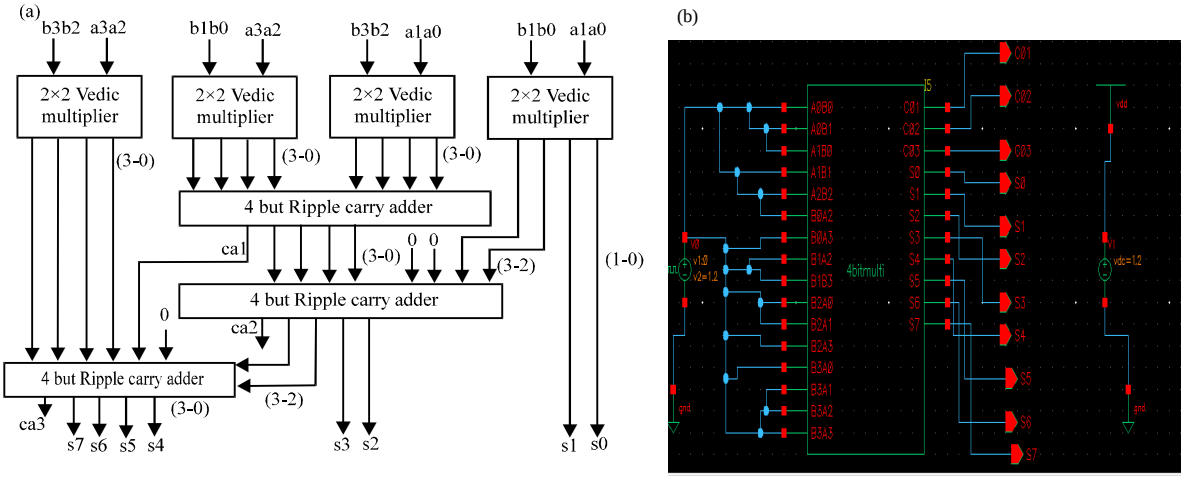

Fig. 7: a) Block diagram of 4×4 Vedic multiplier (Subudhi *et al*., 2014) and b) 4×4 multiplier using Cadence Virtuoso

GDI logic and CMOS are shown in Table 2. The average power of proposed OR gate is little more than CMOS logic. But using proposed AND, XOR, half adder circuit using full swing GDI have less average power as compared to the CMOS logic.

Adder: The 1 bit full adder is implemented using GDI with only 10 Tr. This adder provides weak logic 0 and logic 1. Using modified full swing GDI gates, 1 bit full adder is designed as shown Fig. 6a. The simulated waveform is as shown in Fig. 6b, the output of the full adder is at full voltage from 0 V to Vdd.

Multiplier and divider: The performance of the arithmetic circuits depends upon the type of adder used in it. Here, 4×4 Vedic multiplier is used which produces faster computation compared to conventional multiplier. The 2×2 Vedic multiplier is implemented using half adder. With the help of 4 bit parallel adder and 2×2 Vedic multiplier it is extended to achieve 4×4 multiplication. The block diagram of 4×4 Vedic multiplier is as shown in Fig 7a (Subudhi *et al*., 2014). The same block is implemented in Cadence Virtuoso 45 nm is shown in Fig. 7b.

The block diagram of 7×4 divider is as shown in Fig 8a. The main block of divider circuit is XOR and full adder. The quotient and remainder are obtained. The Divider circuit is implemented using Cadence Virtuoso as shown in Fig. 8b.

Table 2: Average power of full swing GDI logic

	Average power (nw)	
Logic gates	Proposed full swing GDI	CMOS
AND	27.7	35.3
OR	45.1	44.1
XOR	14.2	218.0
HA	38.9	197.5

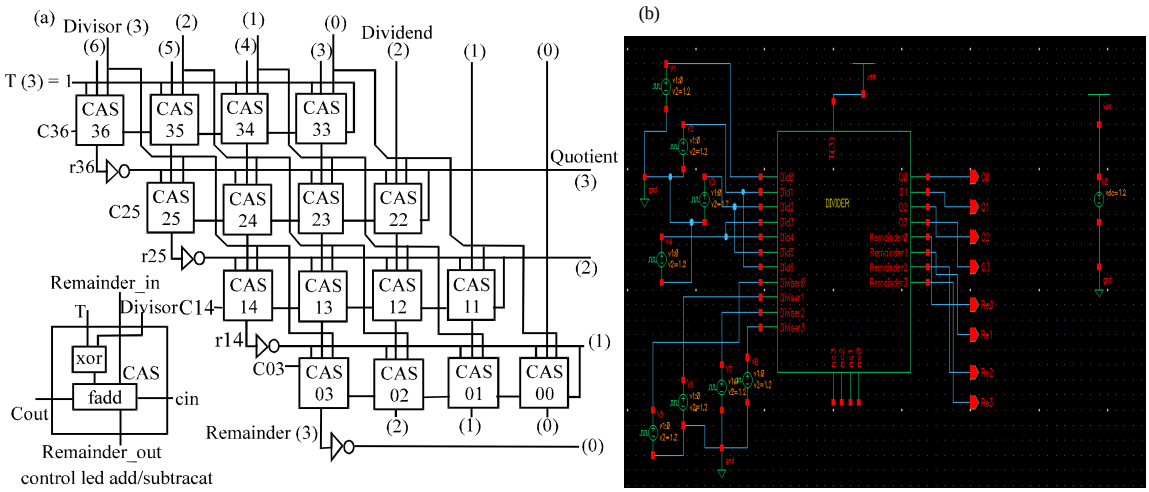

Fig. 8: a) Divider block diagram and b) Divider using Cadence Virtuoso

Table 3: Average power of arithmetic circuits

	Average power	
Variables	GDI FS	CMOS
Full adder (nw)	105.90	166.00
Divider (7×4) (μw)	4.36	7.22
Vedic multiplier (2×2) (nw)	155.80	504.10
4bit RCA (nw)	769.40	767.60
Vedic multiplier (4×4) (μw)	1.55	4.50

RESULTS AND DISCUSSION

The average power of full swing GDI arithmetic circuits are compared with CMOS circuits. Table 3 gives the average power of both CMOS and modified full swing GDI logic. The full swing GDI gives lesser average power than CMOS.

CONCLUSION

The gate diffusion input is an efficient low power design technique. Complex functions can be implemented using less number of transistors. The disadvantage of the GDI technique is reduced output voltage swing. The modified full swing GDI logic are designed using additional transistors to obtain as equivalent to CMOS logic output swing. The arithmetic circuits are designed in Cadence Virtuoso 45 nm technology. The average power of full swing GDI logic are lesser than CMOS logic. The full adder circuit is improved by 37% as compare to CMOS logic. Using this adder circuit multiplier and divider circuit average power is reduced with 66 and 40% and compared to CMOS logic, respectively.

REFERENCES

Koppad, D. and S. Hiremath, 2016. Low power 1-bit full adder circuit using modified Gate Diffusion Input (GDI). Proceedings of the 2016 IEEE 1st International Conference on Micro and Nano Technologies Modelling and Simulation, March 21-24, 2016, IEEE, Leipzig, Germany, pp: 65-68.

Morgenshtein, A., A. Fish and I.A. Wagner, 2002. Gate-Diffusion Input (GDI): A power-efficient method for digital combinatorial circuits. IEEE Trans. Very Large Scale Integr. Syst., 10: 566-581.

Neil, H.E.W. and E. Kamran, 1993. Principles of CMOS VLSI Design. 2nd Edn., Pearson Education Ltd., London, England isBN:978-81-317-19412-8, Pages: 737.

Singh, A.P. and R. Kumar, 1892. Implementation of 1-bit full adder using Gate Diffusion Input (GDI) cell. Intl. J. Electron. Comput. Sci. Eng., 1: 333-342.

Subudhi, A.D., K.C. Gauda, A.K. Pala and J. Das, 2014. Design and implementation of high speed 4x4 vedic multiplier. Intl. J. Adv. Res. Comput. Sci. Software Eng., 4: 362-366.