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A 3.3 V Bi-Directional IO for Multiple Loads in 55 nm CMOS

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Abstract: Interfacing core logic and external world is always been a challenge in VLSI industry. Specially designed IO circuits are used for this purpose. Isolation of crucial core part is achieved by the help of IO circuitry. This study proposes a bi-directional IO for various loads depends on the core circuit which drives the IO. The driving capability of the IO circuit can be varied from 10-40 pF based on the loading in the pad. Control is provided by the help of signals produced by the core circuit. By varying these signals, the loading ability for an IO can be set by the internal logic. In this study, an IO is proposed to connect 1.2 V internal circuitry to 3.3 V pad. Pull-up pull-down networks are included to ensure low short circuit current.

Key words: General Purpose Input Output (GPIO), level shifters, Electrostatic Discharge (ESD), Schmitt trigger, produced, IO, circuits

INTRODUCTION

Interfacing internal core logic circuit to noisy exterior environment is achieved by the help of IO pads. Communication of core circuit in terms of input and output data bit must be flexible according to the surrounding blocks. IO circuits are used to provide this flexibility. Depends on the operating voltage of the peripheral IC which needs to be connected to the core logic IO should convert the internal signal to a higher voltage level. Level shifters are used for this conversions. On the same side the signals needs to be received by the core logic, this voltage levels are generally low values. Direct coupling this signals results in damaging the internal logic. A down shifter is used for this purpose. There are several types of IO circuits (Abraham, 2014). In some application data only needs to be sent out. In some cases communication in both direction is essential. In some cases the signal needs to be extremely noise immune. Based on the application various IO architecture are present. Another aspect it when the core logic is not in use the pads should act as buffers. A high impedance sate to be achieved during this time. Also, when it is neither transmitting nor receiving, the logic state in the pad should be predictable. Internal control signals needs to be provided for this. The methodology for the establishment of these control signals is much important and critical. Shrinkage of technology node is very rapid. Due to this the supply voltage is being scaled down results in faster logic's. IO should match the data processing speed of the core if not it will results in data loss. General purpose IO circuits should be capable of driving huge on-chip capacitance. The internal logic and the surrounding chips could be working in various voltage levels. Up and down level shifters are necessary for voltage conversion to required values. Proper working of this level shifters is essential for the efficient working of the IO circuit. While converting to a higher voltage level the stress introduced in the MOSFETs should be taken with at most care. Stress can cause deterioration in the device over time compromising the device performance and lifetime. While receiving the data from the external world, elimination of noise components is necessary. A Schmitt trigger is used to achieve this. it can provide a hysteresis which leads to lower VIL and higher VIH values. For driving the high capacitance pad several buffers and drivers are necessary (Purushothaman, 2016). Electro static discharge will cause more damage to the chip than earlier days due to the technology shrinkage (Oleg *et al*., 2008). A IO circuits should contain circuits to protect from an ESD event. Generally HBM (Human Body Model) and CDM (Charged Device Model) diodes are incorporated in the IO circuit to bypass the ESD current to the supply nets (Chaine *et al*., 1995).

In this study, a modified level shifter and schmitt trigger design is proposed to overcome the stress issues when connecting to a marginally high voltage. Through this design a better duty cycle and high input noise margin is obtained.

Architecture: Some of the major constraints while designing an IO circuit is:

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- Multiple load carrying ability
- Short circuit current control
- Ability to predict the state of the pad when both receiver and transmitter is ideal
- Low leakage

IO circuits mainly consist of three blocks. Transmitter, receiver and a pull-up pull-down network. The transmitter receives input from the internal logic circuit. An input buffer is necessary in order to strengthen this weak signal. Transmitter level shifter in the IO converts the VDDC level to the VDDIO level (Serneels *et al*., 2008). When the IO pad acts as an input buffer high impedance state should be achieved. This high impedance state is created by a tri-state buffer which is incorporated in the proposed level shifter design. System is designed is to handle upto 40 pf even though it might not always necessary that much current need to flow to the pad. A predriver circuit is used to overcome this issue. Predriver circuit decides how much current should flow to the PAD based on the load. Top level architecture of the IO circuit is shown in Fig. 1.

The receiver block contains a Schmitt trigger (Kumar *et al*., 2012) which is used for hysteresis control. The hysteresis control make sure that the receiver circuit will not transmit any noise to the internal core circuit which it picks up from the noisy outside world. The down level shifter (Kumar *et al*., 2010) change the voltage level from pad value to internal logic value, a core buffer is introduced to strengthen the signal before giving to the internal logic. The ESD protection diodes are connected to the PAD. In this study, a modified level shifter and Schmitt trigger circuit is proposed to overcome the stress issues in the MOSFET while connecting to a high voltage node.

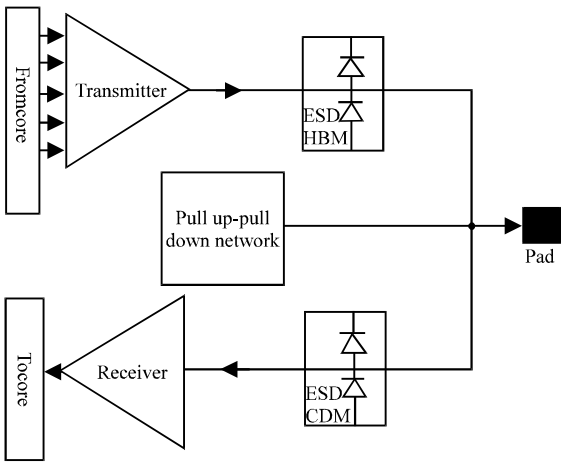

Fig. 1: IO architecture

MATERIALS AND METHODS

Proposed system

Transmitter: The block diagram of transmitter part is shown in Fig. 2. Transmitter mainly consist of four level shifters and a predriver. Pre-driver will decide how many level shifters should be enabled depending on the requirement. Two control signals DRV <0:1> which are generated by the core circuitry will help the predriver to choose suitable number of level shifters. TRIENC, V REFP and V REFN are the other control signals. Here, TRIENC will decide the state of the pad. The pad will be in high impedance then TRIENC = Logic 1. When TRIENC is in logic 0, IO circuit is in transmission mode.

Pre-driver: Pre-driver is a decoding logic which is realised using NAND, NOR and NOT gates (Uyemura, 2002). It also consist of a simple level shifter just to boost up the TRIENC signal to an intermediate level. Pre-driver is designed in such a way that the it operates in core circuits power supply which make the predriver circuit faster than the previous designs. Working of predriver circuit is shown in Table 1.

Level shifter: Level shifter plays a crucial role in converting the core voltage level to IO level. In 55 nm technology, the core voltage is 1.2 V which is to be up shifted to 3.3 V. The output of the level shifter should settle before 10% of time period with a minimum variation in duty cycle, worst case should be <20% (Ravi *et al*., 2015) across process variations and voltage.

Table 1: Predriver decoder output

DRV1	DRV0	Data VDDC<3:0>	VREFTRI<3:0>
0	0	0 0 0 D	0 0 0 1
0	1	0 0 D D	0 0 1 1
1	0	0 D D D	0 1 1 1
1	1	D D D D	1 1 1 1

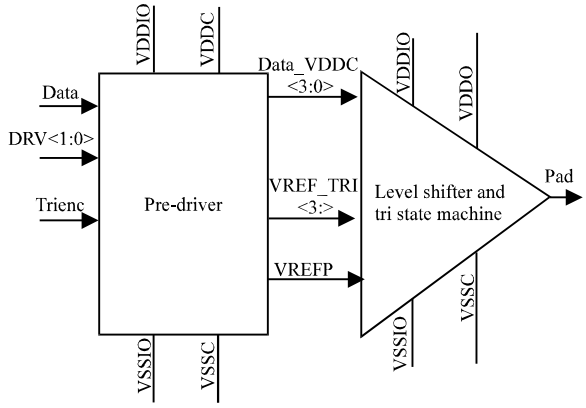

Fig. 2: Transmitter block diagram

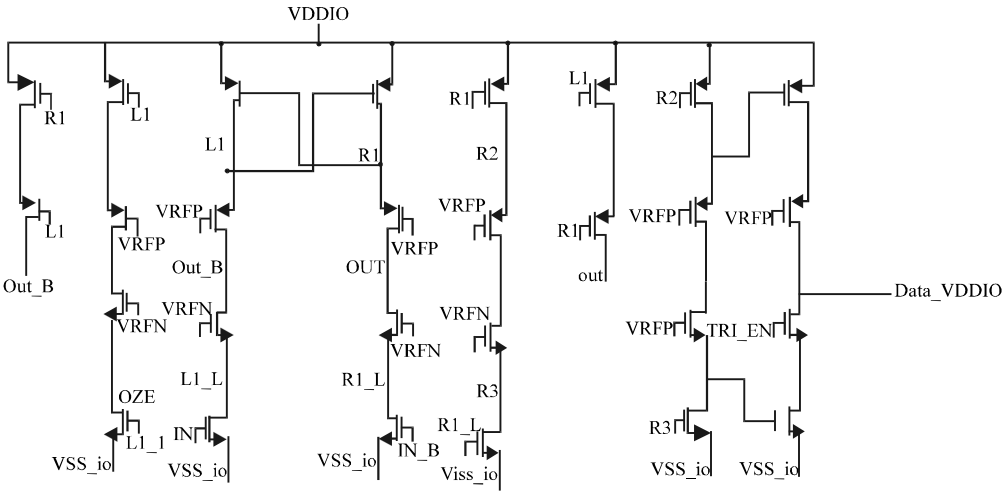

Fig. 3: Proposed level shifter circuit diagram

Another thing should be taken care is the stress introduced in the devices. In this study, a new design for a level shifter is proposed. This circuit will also act as a tri-state machine when the TRI EN signal is high which will keep the pad in high impedance. High impedance state is necessary when the pad is operated as a buffer by using this circuit no additional driver circuit is needed. This circuit itself is capable of driving the load in the pad. Circuit diagram of the proposed level shifter is shown in Fig. 3. Here, input signals IN and IN_B is fed to bottom NMOS's. Top portion consist cross coupled PMOS devices. Design of level shifters is done such that the PMOS and NMOS sizing is done for obtaining optimum rise and fall times. From the level shifter circuit it is clear that when the input falls from 1-0, the deciding node for a transition to occur is the node OUT which has to fall fast, so that, the PMOS switches on and thus, 3.3 V appears at the node LL of the so that OUT node is perfectly pulled down by NMOS transistors. This occurs in the reverse case also. Additional devices are added to reduce the stress (Rahul *et al*., 2015) between the nodes. Not only it reduces the stress it will also helps to minimize the leakage current. Since, the OUT net is experiencing more loading due to additional capacitance introduced by the buffers, there will be a mismatch in current flow between the two legs of level shifter. To avoid this same buffers are added to the OUTB net. This will maintain the symmetry thereby ensures equal current flows through the level shifter legs. For enabling the stacked devices V RFN V RFP bias signals are provided which is set to 1.8 V. The circuit will also act as a tri-state buffer by setting the TRIEN signal to logic 0.

Pull-up pull-down network: It is critical to predict the state of the pad when there is no transmission or reception takes place. Pull-up and pull-down network is used for this. For this two control signals are generated in the core. The circuit consist of a stacked PMOS device and a stacked NMOS device and a current limiting resistor (Purushothaman, 2016) to avoid the unnecessary current flow. It also helps in reducing leakage.

Receiver: The receiver part of an IO circuit contain a circuit for noise eliminating circuit, a down level shifter and buffers. Noise elimination is achieved by hysteresis control. A Schmitt trigger is used for serving this purpose. ESD diodes are also connected to the pad for bypassing ESD currents to the power nets. Schmitt trigger output is connected to the down level shifter for scaling down its value to the core level. The down level shifter for 3.3-1.2 V voltage scaling is a stacked inverter circuit with supply voltage of 1.2 V. The schmitt trigger circuit is designed for producing a better VIL and VIH values. Receiver buffers are used to reshape the level shifter output and for strengthening it, design consideration is based on the level of signal conditioning. Receiver enable signal is used to trigger the receiver circuit.

Schmitt trigger: A modified Schmitt trigger circuit is proposed in this study. A Schmitt trigger is used in the receiver to eliminate the external noises by introducing a hysteresis in the received signal from the pad. Being in contact with the external world the pad is susceptible to noise. Removal of this noise is one of the important function of the IO circuit. Modified Schmitt trigger circuit diagram is shown in Fig. 4.

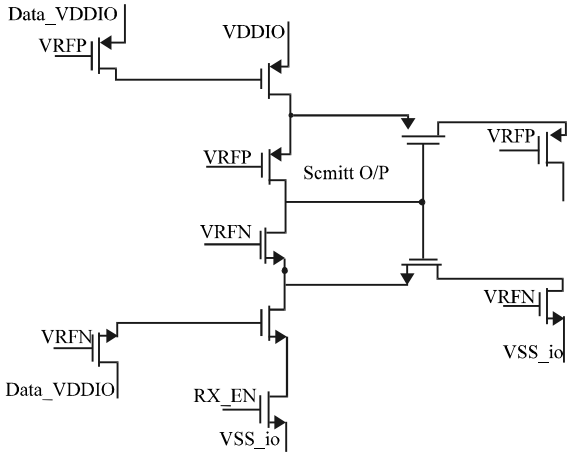

Fig. 4: Modified Schmitt circuit

The cascaded transistors in between will have higher Vth than top and bottom transistors due body effect, Because of this Vth variation these transistors are capable of providing a hysteresis window as they switch from higher to lower logic levels. For the improvement of the hysteresis extra transistors are added to the output net. When logic 0 is applied to the input, the PMOS's are ON and the NMOS's are OFF. As the input-level crosses to threshold voltage of bottom NMOS, it turns ON and tries to pull down the node between itself and the stacked NMOS to 0. At the same time, the extra transistor will turn ON and tries to pull up the node to VDD-Vth. Because of this the output level will stay high for more duration. When the input rise to value such that it can provide a VGS greater than the threshold voltage of bottom NMOS transistor. When the input switches from high to low PMOS's will undergo the same operation. The (W/L) values of the stacked and extra transistors will decide the shape of hysteresis loop. Input is fed through another set of transistors for reducing the stress in the nodes. These transistors are enabled by control signal with bias voltage 1.8 V.

RESULTS AND DISCUSSION

The IO block is designed for a core voltage of 1.2 V and a pad voltage of 3.3 V. The circuit is implemented and simulated in 55 nm CMOS technology model. Simulation are done for various PVT corners. Obtained results shows only minimal variation in the PVT checks. Observed results are shown in Table 2.

Figure 5 shows the output of level shifter. The input core voltage is effectively converted to 3.29734 V. Duty cycle has been observed as 50.55 in typical process. maximum duty cycle observed is 50.68. PVT corner analysis of duty cycle is shown in Fig. 6.

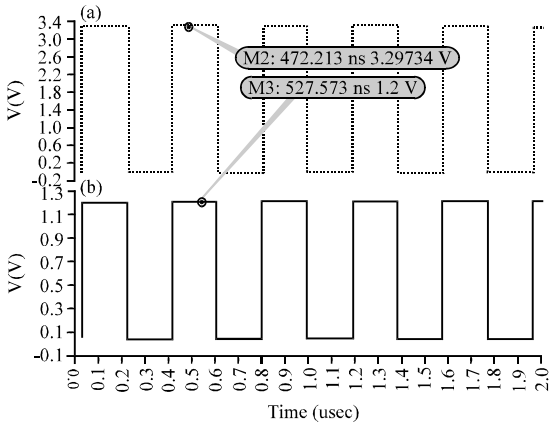

Fig 5: a, b) Level shifter output

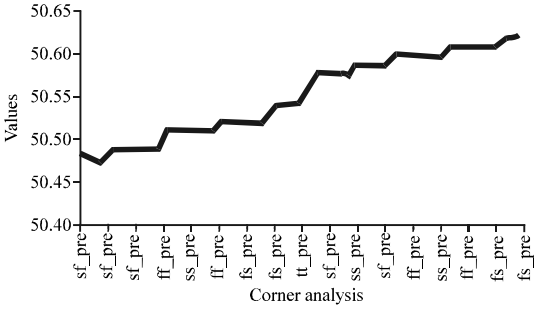

Fig. 6: PVT corner analysis of duty cycle

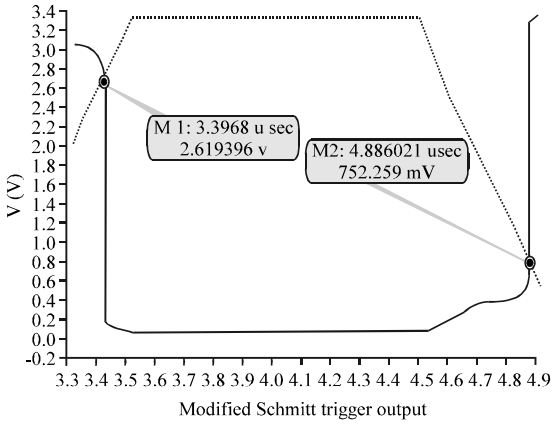

Fig. 7: Modified Schmitt trigger otput

Figure 7 shows the VIL and VIH levels of Schmitt trigger. Obtained results shows that the designed circuit has higher input noise margin. In the receiver part the output from the pad is transmitted to internal core circuitry. The signal level is down shifted to 1.2 V from 3.3 V. Output of the receiver is shown in Fig. 8.

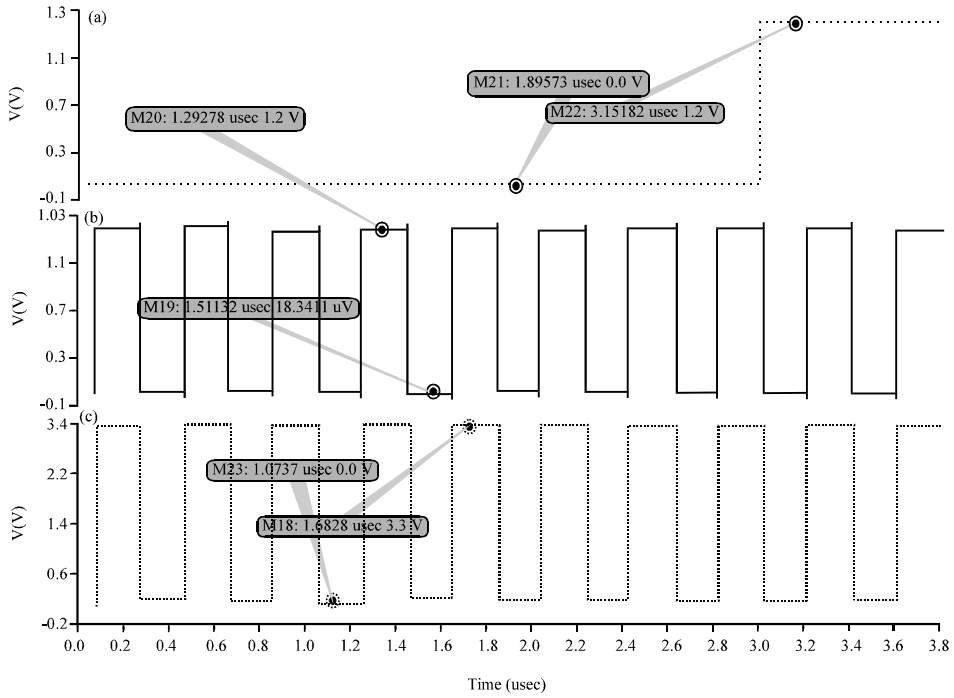

Fig. 8: Receiver output

Table 2: Result observed for IO circuit

Parameters	Minimum	Typical	Maximum
VDDIO	3	3.3	3.6
VDDC	1.08	1.2	1.32
Temperature	-40	27	125
Frequency		50 MHz	
VIL			0.25×VDDIO
VIH	0.78×VDDIO		
Duty cycle	50.46	50.55	50.68
VOL			0.25 V
VOL	3.15 V		

CONCLUSION

This study presents a 3.3 V IO circuit. New design for up level shifter and Schmitt trigger has been successfully implemented in 55 nm technology. Circuit is found to be stable under various PVT corner analysis. By the new design the stress experienced in the devices has been reduced. The IO can drive up to 40 pF at a frequency of 50 MHz with a duty cycle of 50.55.

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