Journal of Engineering and Applied Sciences 13 (Special Issue 14): 11108-11113, 2018
ISSN: 1816-949X

Implementation of QPSK Transceiver Using System Generator Based Communication

[1]Ekhlas K. Hamza, [1]Laheeb S. Mahdy and [2]Fadel Sahib
[1]Department of Control and Systems Engineering, University of Technology, 52 Street, Baghdad, Iraq
[2]Department of Electrical Engineering, College of Engineering, Mustansiriyah University, Baghdad, Iraq

Abstract: QPSK is higher order planner use on digital modulation. QPSK is one type of digital modulation technique use to transfer the base band data wirelessly in efficient way compare from to other modulation. This study present the basic of QPSK modulation technique.The proposed QPSK transceiver can be implement on FPGA (Field Programmable Gate Array) by use the notation of hardware co-simulation on depressed power. QPSK transceiver are simulate using MATLAB (Simulink) environment with system generator and the algorithm for transceiver have been simulate using MATLAB R2011a with Xilinx ISE 14.1 system generator and later on that convert very fast speed integrated circuit hardware description languages to perform it in FPGA on SPARTAN 3A board.

Key words: QPSK, Simulink, Xilinx system generator, FPGA, MATLAB, algorithm

INTRODUCTION

The modulator is the basic demand from communication system there is create to decrease channel castrate and for used in RF communication subsequently much type from transporter modulation technique has been previously proposed depend on to channel properties and data rate from systems (Taggart and Kumar, 2011; Jain *et al*., 2017; Grollier and Houcke, 2018). QPSK (Quadrature Phase Shift Keying) are one from the modulation planner utilized on wireless communication systems because its capability to move two times data rate to specified bandwidth (Panasiewicz *et al*., 2017; Pareek, 2016). The system based on FPGA has feature like re programmability and re configurability and they are also very easy to upgrade, hence, it is possible to have flexibility in the product development cycle (Rieth *et al*., 2015; Khanna *et al*., 2015). In (QPSK) modulation transporter band acquire (4) separated event that are used to symbolize set of (2) input data bit from Table 1 is shown. Every set take one shape from the QPSK event ±135° and ±45° for (1) bit symbolize in phase (I) and (2) bit symbolize Quadrature phase (Q), (QPSK) modulation are couple from (BPSK) Binary Phase Shaft Keying, data transmission on a (QPSK) are two time compare (BPSK) (Yang and Tsai, 2016; Al Safi and Bazuin, 2016).

Table 1: QPSK phase for several event

Input	QPSK(°)
00	225
01	315
10	135
11	45

MATERIALS AND METHODS

QPSK transceiver model: QPSK transceiver is general from block diagram in Fig. 1, contain transmitter and receiver, the transmitter contain for input data for QPSK is random binary sequence (1's and 0's) generated a by Bernoulli Binary Generator. In the QPSK we can send two bit per symbol and so is use for high data rate application. AWGN are a channel on who the single important into communications are a linear supplement for wideband or white noise for a fixed spectral density (W/Hz) for bandwidth and gaussian division for a capacity. The receiver demodulate the input signal using binary phase shift keying. Block of the delay are uses to sample and hold with one sample period delay. Block of the error rate counting compare input of transmitter for the output data of a receiver.

QPSK transmitter: Quadrature Phase Shift Keying (QPSK) are consist of 2 (BPSK) Binary Phase Shift Keying modulator, mapped circuit, whose are S/P (Serial to Parallel) convertor shift register and transporter generator. The binary serial bits series split for 2 bit parallel sequence in phase (I) bit and Quadrature phase (Q) bit are

Corresponding Author: Laheeb S. Mahdy, Department of Control and Systems Engineering, University of Technology, 52 Street, Baghdad, Iraq

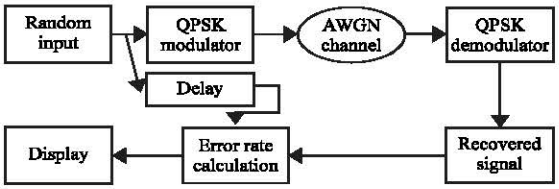

Fig. 1: QPSK transceiver model

applied for Binary Phase Shift Keying (BPSK) modulator whose transporter frequency are orthogonal for each other, there is generate with transporter generator. Output for both BPSK (Binary Phase Shift Keying) modulators are add with summing amplifier which products QPSK modulate signal which can be transmit through antenna (Fig. 2).

QPSK receiver: The QPSK demodulator is shown in Fig. 3. In demodulator of the QPSK signal is applied to 2 balance modulator and there is multiplied for same transporter frequency as on the modulator (Raghavendra *et al*., 2013). The output for each balance modulators hold jointly baseband component and up frequency component. The LPF (Low Pass Filter) remove up frequency components and leave baseband component. The output of 2 LPF's is then specific for the damping circuit who give the authentic signal m(t). The signal of output upper balance modulator is given from Eq. 2 and 3 in phase component.

$$\text{st cos wt} = [(1/\sqrt{2})\text{dI (t) cos wt}+((1/\sqrt{2})\text{dQ(t)sin wt}]\text{ cos wt} \quad (1)$$

$$\text{st cos wt} = [(1/\sqrt{2})\text{ dI (t)}[1+(\cos 2\text{wt}/2)]+\text{dQ(t)sin wt cos wt} \quad (2)$$

The signal of output lower balance modulator is given from Eq. 3.

$$\text{s(t) sin wt} = [(1/\sqrt{2})\text{dI(t) cos wt}+(1/\sqrt{2})\text{dQ(t)sin wt}]\text{ sin wt} \quad (3)$$

$$\text{s(t) sin wt} = [(1/\sqrt{2})\text{dI(t)cos wt.sin wt}+(1/\sqrt{2})\text{dQ(t)sin}^2\text{wt} \quad (4)$$

Equation 4 quadrature phase component. The demapping circuit added the in phase component and quadrature phase component which product into modulating signal m(t).

QPSK transceiver based of system generator: In the QPSK transceiver is follow, transmitter and receiver based simulate using MATLAB (Simulink) environment with system generator.

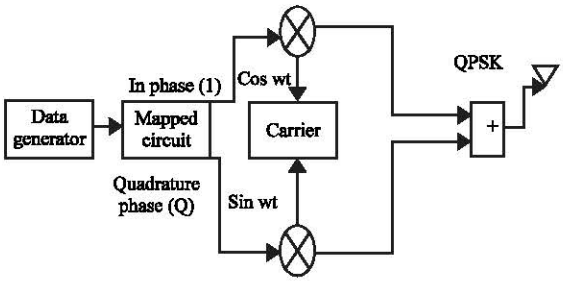

Fig. 2: Transmitter of QPSK

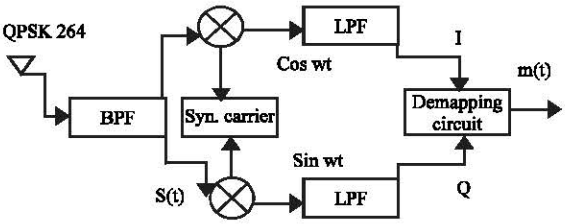

Fig. 3: Receiver of QPSK

QPSK transmitter of system generator: System generator are digital signal layout agent of Xilinx, it is base in MATLAB-Simulink medium use FPGA layout. All implement stages, include synthesis, place and route is mechanically perform for generated on FPGA program file. In Fig. 4 is shown the achievement from QPSK transmitter employ system generator tool on Simulink. The QPSK transmitter in system generator contain input data is random binary sequence generate a by using bernoulli binary generator, serial to parallel and combination of two ROM (Mapper-I, Mapper-Q). The serial to parallel input is ordered with the most significant word first, the serial unsigned data. Xilinx ROM block is a single port read only memory that stores four words corresponding to "00", "01", "10", "11". Two ROM are used for both I and Q channels.

QPSK receiver of system generator: The QPSK receiver design contain from two BPSK detection, the first BPSK (In phase) and the two BPSK (Quadrature phase), concatenated and parallel to serial. Figure 5 shown receiver of QPSK and Fig. 6 shown transceiver of QPSK.

The simulation QPSK Model result is based on the Xilinx system generator. The following waveform appear in Fig. 7. The QPSK transmitter in system generator consists: Bernoulli Binary Generator (BBG), (BBG) which is used to inspire the data random input as shown in the Fig. 7 the row (a), gate in block which is used for giving input to the Xilinx portion of the Simulink design, gate out

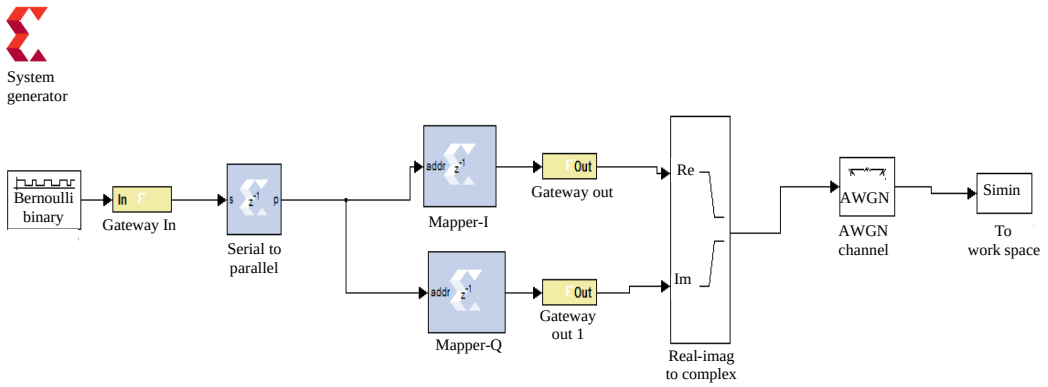

Fig. 4: QPSK transmitter of system generator

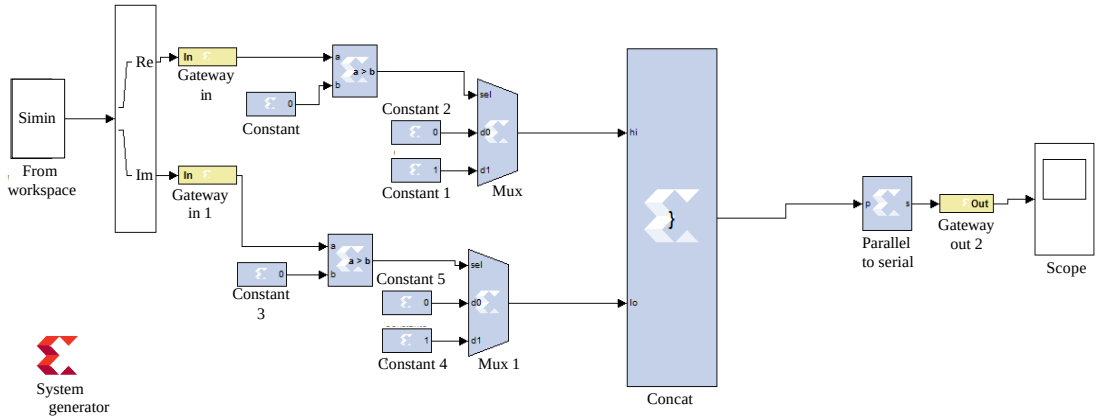

Fig. 5: QPSK receiver of system generator

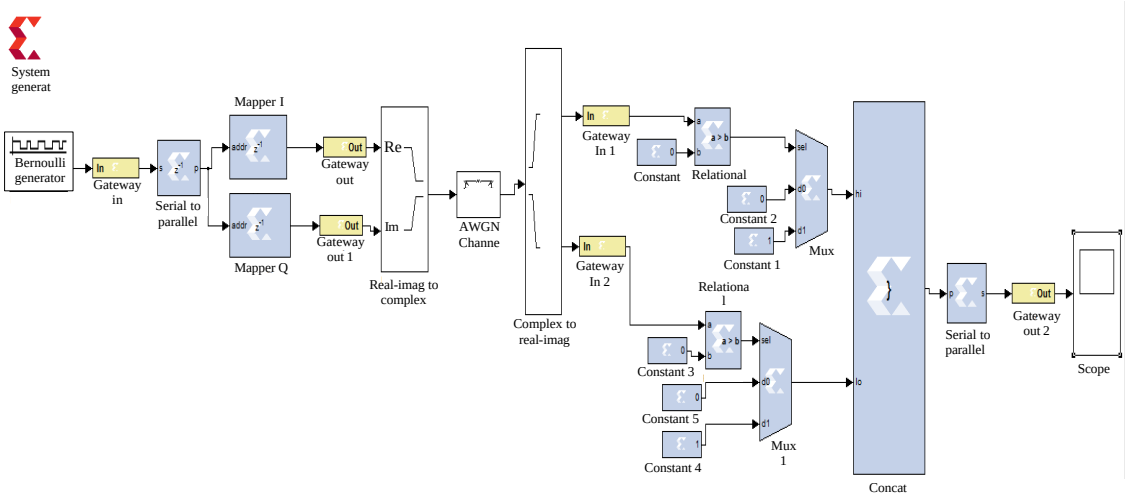

Fig. 6: QPSK transceiver of system generator

block which is used for the xilinx portion of the Simulink design; the Serial to Parallel (S/P) block take the serial unsigned data represented in fixed point of one bit with zero binary point and create a signal output of two bits to be mapped later in the ROM to the corresponding QPSK symbol. QPSK symbol contain for quadrature and in

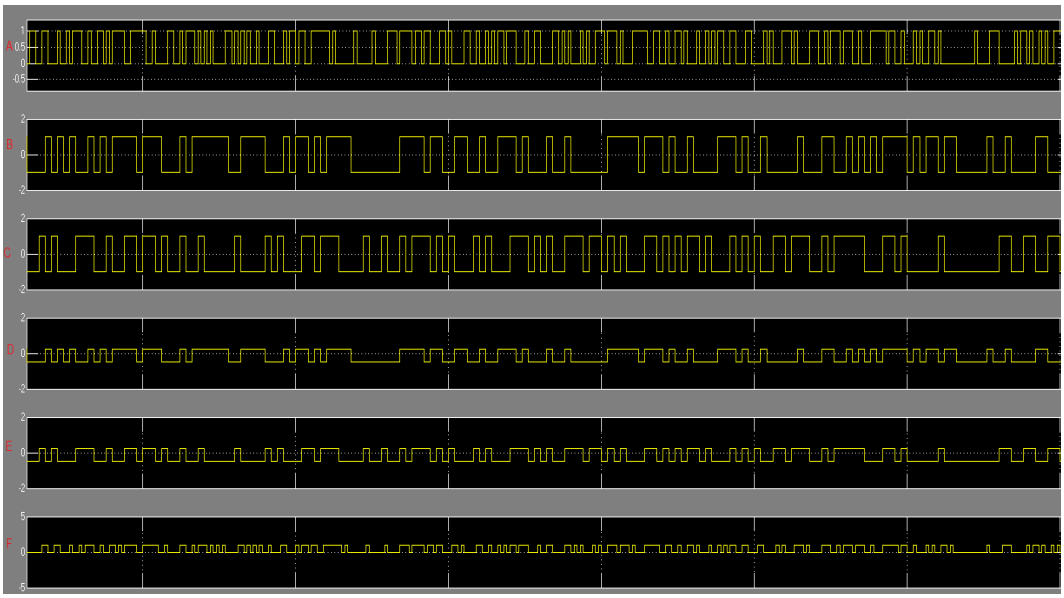

Fig. 7: Simulation waveform for QPSK fig

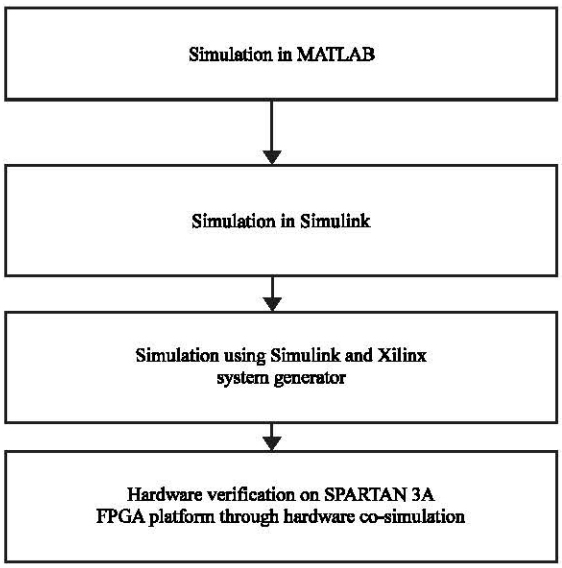

Fig. 8: FPGA based hardware software co-simulation

phase value, the two rom are use of both Q and channels, the output wave of the Mapper-I and the output Mapper-Q as shown in the figure below the row(b), row(c); Additive White Gaussian Noise (AWGN) channel block is added of linear addition for white noise, the QPSK receiver in system generator consists: The two Binary Phase Shift Keying (BPSK) which is used to demodulation of QPSK, the output wave of the BPSK as shown in the figure below the row (d) and row (e), the two bits coming from first BPSK and second BPSK channels are concatenated to compose unsigned value by used Xilinx bus concatenated and Parallel to Serial (P/S) leads to two serial samples, the output wave of the (P/S) as shown in Fig. 8 the row(f).

RESULTS AND DISCUSSION

Hardware-software co-simulation: For System Generator (SG) supplied hardware co-simulation made its likely blend design run on FPGA straight to Simulink simulation. Hardware co-simulation compilation target automatically make bit flow and support it to block as shown in Fig. 8. When of the design systems are simulates on Simulink result to compile fraction is calculate on FPGA hardware always result on significantly high simulate time while verifying the functional correctness for hardware.

QPSK transceiver of system generator by JTAG: The QPSK transceiver is follow, transmitter and receiver in system generator are implement on SPARTAN 3A board with use hardware-software co-simulation via. JTAG cable.

QPSK transmitter of system generator by JTAG: In this Fig. 9 show the QPSK transmitter of system generator is implementation on device SPARTAN 3A by hardware-software co-simulation through JTAG cable.

QPSK resceiver of system generator by JTAG: In this Fig. 10 show the QPSK receiver of system generator is implementation on device SPARTAN 3A by hardware-software co-simulation through JTAG cable as shown in Fig. 11.

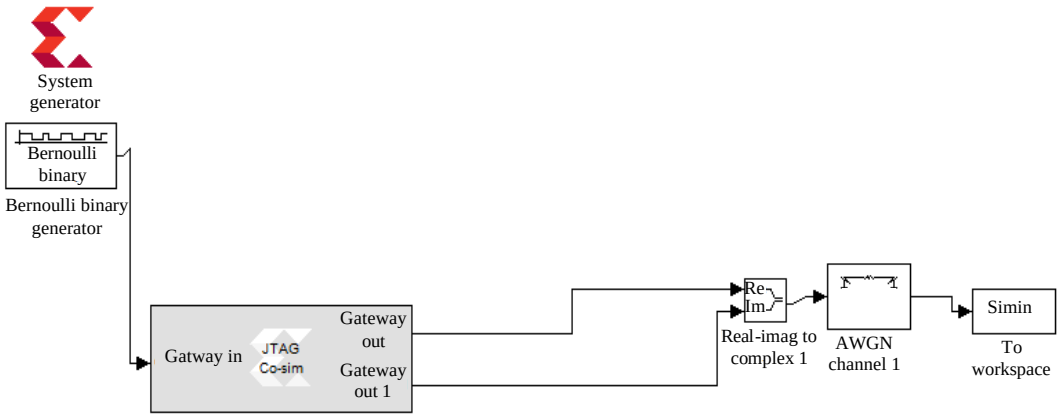

Fig. 9: QPSK transmitter

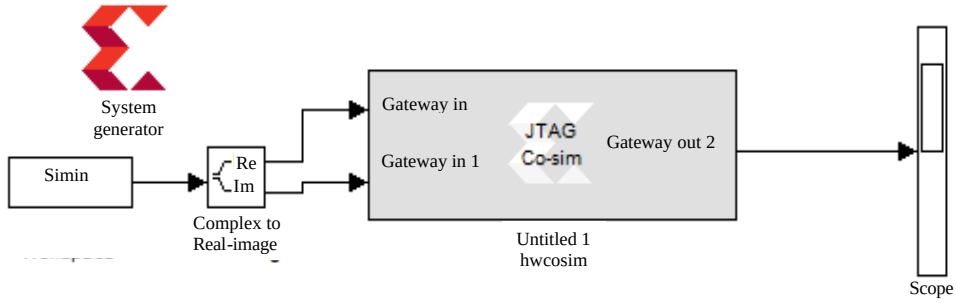

Fig. 10: QPSK receiver

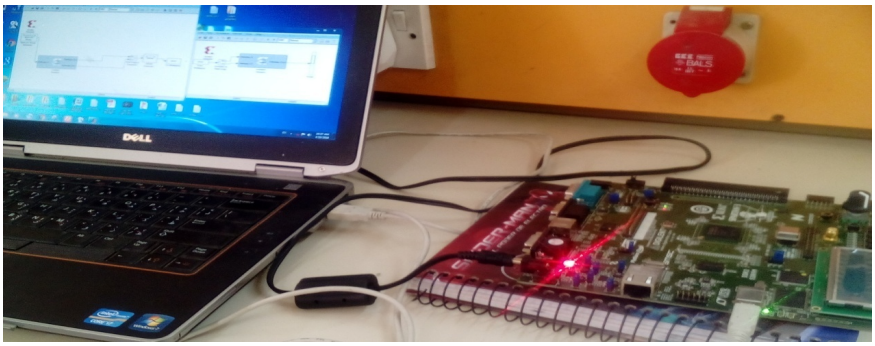

Fig. 11: Implementation QPSK on FPGA

Table 2: Devices utilization of QPSK transmitter

	Device utilization summary			
Logic utilization	Used	Available	Utilization (%)	Notes (sec)
No. of slice flip flops	2	11.776	1	
No. of occupied slices	2	5.888	1	
No. of slices containing only related logic	2	2	100	
No. of slices containing unrelated logic	0	2	0	
No. of bonded IOBs	7	372	1	
No. of BUFGMUXs	1	24	4	
No. of RAMB 16BWEs	2	20	10	
Average fanout of non-clock nets	1.75			

Table 3: Devices utilization summary of QPSK receiver

	Device utilization summary		
Logic utilization	Used	Available	Utilization (%)
No. of slices	10	5888	0
No. of slice flip flops	16	11776	0
No. of input LUTs	3	11776	0
No. of bonded IOBs	6	372	1
No. of GCLKs	1	24	4

Resource utilization: Table 2 and 3 is shown design summary of QPSK transmitter board and receivers. The device utilization summary is generate when the design is synthesized successfully.

CONCLUSION

The proposed of the QPSK in this study from the communication systems were implemented on the Simulink medium using Xilinx system generator. The QPSK Model (transceiver) are successfully simulation and implementation in FPGA. The future goal is to in practice establish the implement and simulate of spectrum sensing in Cognitive Radio (CR).

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