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Design and Implementation of a Low-Voltage Four Selectable Fractional-Order Differentiator in a 0.35 μm CMOS Technology

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Abstract: This study focused on the design and implementation of a four selectable Fractional-Order (0.2, 0.4, 0.6 and 0.8) Differentiator (FOD) in a 0.35 μm CMOS technology operated at 1.5 V supply. In comparison with previous research that use discrete components and generic microcontroller to switch an FOD from one order to the next, this design of a selectable FOD was realized in an analog microelectronics scale. The dimension of the Integrated Circuit (IC) layout was further reduced by employing reusability of capacitors and resistors. The whole chip layout of the design, excluding input/output pads has a dimension of 8.10×6.30 mm or equivalent to a final area of 51.03 mm^2. The four possible orders of an FOD were characterized in terms of its magnitude and phase response in the working bandwidth from 10-1 kHz. Characterization was made using SPICE simulation tool and IC layout editor software.

Key words: Constant phase element, resistor-capacitor ladder, selectable fractional-order differentiator, characterization, implementation, microcontroller

INTRODUCTION

Since, the first research on system modeling a few centuries ago, a lot of dynamical systems are described as Integer Order (IO) systems. However, several researches in many different areas (Khanra *et al*., 2008; Gonzalez *et al*., 2013; Benchellal *et al*., 2006; Dalir and Bashour, 2010) have proven otherwise. The real world is more aptly described as Fractional Order (FO) in nature, thus, it should be characterized by dynamic systems of non-integer order. As for example, description of the voltage-current relation of a semiinfinite lossy transmission line (Wang, 1987) or diffusion of heat through a semi-infinite solid (Podlubny, 1998) are more accurately modeled when represented as a fractional order system.

The field of fractional calculus was first developed by mathematicians in the middle of the ninetieth century. But the idea of fractional calculus has already been established, since, the classical calculus with the first reference being associated with Leibniz and hospital in 1695 where half-order derivative was mentioned (Petras, 2011). Though existed for more than 300 years, the idea of fractional calculus has remained quite a strange topic because of the higher complexity it exhibits and the absence of solution methods for fractional differential equation. Not until major advancements have been made in this area in the last three decades where mathematicians like Euler, Lagrange, Laplace.

Constant Phase Element (CPE): According to Valsa *et al*. (2011), an ideal CPE has impedance defined as:

$$Z(s) = Ds^{\alpha} \quad (1)$$

And for $s = j\omega$:

$$Z(j\omega) = D\omega^{\alpha}(\cos\varphi + j\sin\varphi) \quad (2)$$

where $\varphi = (90^*\alpha)$ in degrees. The characteristics of the impedance is primarily dependent on the value of α. There are three classical groups that the impedance may be categorized. If $\alpha = +1$, it is an inductive reactance, if $\alpha = -1$, it represents a capacitive reactance and it is a real resistance or conductance if $\alpha = 0$. However, these categories were further extended as researchers found it necessary to have an order other than 0 and ±1 for a more accurate modeling of a dynamical system. Since then, fractors are introduced. Fractors can either be a fractional capacitor or a fractional inductor still depending on the value of α (Gonzales, 2013; Gonzalez *et al*., 2014). If $0<\alpha<1$, it corresponds to a fractal inductor and if $-1<\alpha<0$, a fractal capacitor.

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The modulus of the impedance depends on frequency according to the magnitude of " (Gonzales, 2013). Its value in decibels varies Lacroix and Fourier dabbled with it following hospital's and Leibniz's first inquisition (Loverro, 2004). Since then, it has gained attentions in many engineering applications such as electrical network as FO impedance (Haba *et al*., 2008), automatic control theory as FO controller (Podlubny *et al*., 2002) and signal processing as FO filter (Ferdi, 2011).

MATERIALS AND METHODS

Fractional-order differentiator:A Fractional-Order Differentiator (FOD) is basically a modification of a basic differentiator. The FOD can be built and designed on the principle clearly visible as shown in Fig. 1. Apparently, it is almost the same with a basic differentiator except for an input element being replaced by a Constant Phase Element (CPE). Along with the resistance RF, CPE defines the order of the FOD (Dorcak *et al*., 2012) with the expression 20*" dB/decade and in correspondence with the sign of ", the modulus increases or decreases. Furthermore, argument of the impedance is constant at the expression (90*")° and frequency independent.

RC ladder network for CPE realization: Constant phase element can be electronically realized by having an infinite parallel combination of series RC network (Podlubny *et al*., 2002). This realization is practically impossible to achieve due to the infinite number of components needed. An improved version of CPE was introduced by Gonzales (2013). The optimization reduced the complexity of the model and at the same time preserves the required good qualities of a CPE. The problem was resolved by truncating the network to form finite number of ladder branches and substituting two single components (C_p and R_p) at both ends of the truncated network as shown in Fig. 2.

The succeeding discussions of the RC ladder computation in this study are based by Gonzalez *et al*. (2014). However for this study, the cited procedure was further simplified and reduced to come up with a more general and flexible way in designing and realizing constant phase element.

Generally, the conceptual design starts with the identification of 4 initial values namely the ripple factor Î n order of the differentiation ", number of RC ladder branches m and initial value of R_1. Given that the ladder is only an approximation of an ideal CPE network, it is therefore, inevitable at a certain range of frequency for ripple to exist. The allowable phase ripple and variable ab is related as:

$$\Delta\varphi = \frac{0.24}{ab} - 1 \quad (3)$$

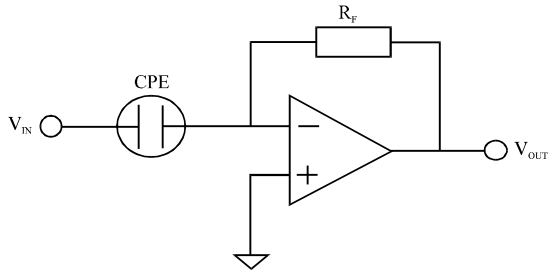

Fig. 1: Fractional-order differentiator circuit

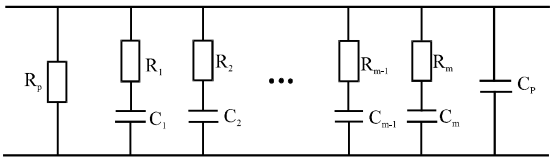

Fig. 2: Improved RC ladder with R_p and C_p

Also, the order of differentiation " can be linked with variable ab in Eq. 4:

$$\alpha = \frac{\log \alpha}{\log(ab)} \quad (4)$$

The computed variables a and b will be used to determine the values of the RC ladder branches (m parallel sections) by using Eq. 5 and 6:

$$R_K = R_1 a^{k-1} \quad (5)$$

And:

$$C_k = \frac{b^{k-1}}{100\ R_1} \quad (6)$$

The resistive side of the ladder can be represented by a single resistor:

$$R_p = R_1 \frac{1-a}{a} \quad (7)$$

while the capacitive side can be represented by a single capacitor:

$$C_p = \frac{b^m}{100\ R_1 (1-b)} \quad (8)$$

Table 1 presents the summarized comparison of the original computation based by Gonzalez *et al*. (2014) and optimized RC ladder branch values computation developed and presented by Abulencia and Abad (2015) was adopted in this study. The major difference in the optimized method relative to the steps in the original (Gonzalez *et al*., 2014) is that there is no recalibration necessary at the end of the computation. This idea makes the designing of constant phase element more general

Table 1: Comparison of the original and optimized RC ladder branch values computation

Steps	Original computation (Gonzalez *et al*., 2013)	Optimized computation
Initial values needed	Phase Ripple ($\Delta\phi$) Desired gain (Dr) order (α) No. of branch (m) Initial R_1 and C_1	Phase Ripple ($\Delta\phi$) Order (α) No. of branch (m) Initial R_1
Determination of parameters 'a' and 'b'	$ab \approx 0.24/1+\Delta\varphi$ $\log a = \alpha \log (ab)$	$ab \approx 0.24/1+\Delta\varphi$ $\log a = \alpha \log (ab)$
Determination of RC ladder branch values	$R_k = R_1 a^{k-1}$ $C_k = C_1 b^{k-1}$	$R_k = R_1 a^{k-1}$ $C_k = b^{k-1}/100R_1$
Determination of 'R_p' and 'C_p'	$R_p = R_1 1\text{-}a/a$ $C_p = C_1 b^m/1\text{-}b$	$R_p = R_1 1\text{-}a/a$ $C_p = C_1 b^m/100\ R_1\ (1\text{-}b)$
Approx. min. and max. frequencies of operation	$\omega_{max} \approx \omega_{min}/(ab)^m$ $\omega_{av} = \sqrt{\omega_{max}\omega_{min}}$	$\omega_{max} \approx \omega_{min}/(ab)^m$ $\omega_{av} = \sqrt{\omega_{max}\omega_{min}}$
Recalibration of the resistor and capacitor values	$Y(j\omega) = 1/R_p + j\omega C_p + \ldots + \sum_{k=1}^{m} \frac{j\omega C_k}{1+j\omega R_k C_k}$ $D = \frac{1}{\lvert Y(j\omega_{av})\rvert\, \omega_{av}^{z}\rvert}$	No recalibration needed

Table 2: List of all resistor and capacitor values for the four fractional order differentiation

Order	0.20	0.40	0.60	0.80
R_1 (Ω)	200000.00	200000.00	200000.00	200000.00
R_2 (Ω)	144955.93	105061.11	76146.16	55189.19
R_3 (Ω)	105061.11	55189.19	28991.19	15229.23
R_4 (Ω)	76146.16	28991.19	11037.84	4202.44
R_5 (Ω)	55189.19	15229.23	4202.44	1159.65
R_p (Ω)	75945.93	180730.79	325305.56	524779.66
C_1 (F)	5.0000E-08	5.0000E-08	5.0000E-08	5.0000
C_2 (F)	1.3797E-08	1.9037E-08	2.6265E-08	3.6239
C_3 (F)	3.8073E-09	7.2478E-09	1.3797E-08	2.6265
C_4 (F)	1.0506E-09	2.7595E-09	7.2478E-09	1.9037
C_5 (F)	2.8991E-10	1.0506E-09	3.8073E-09	1.3797
C_p (F)	1.1049E-10	6.4592E-10	4.2132E-09	3.6335

and flexible as this allows having common values of R_1 and C_1 for different fractional orders as shown in Table 2.

It can also be observed from Table 2 that as the order of an FOD increases, the resistor values needed in the RC ladder branches decreases contrary though to R_p which behaves otherwise and to R_1 which is common to all orders. On the other side as the order of an FOD increases, capacitor values also increases for all RC ladder branches excluding to the Common C_1. Such RC ladder characteristics make employing reusability of resistors and capacitors much simpler in switching from one order to the next.

Conceptual design: A variable Fractional-Order Differentiator (FOD) as the name implies can be tuned to a certain differentiator depending on the acquired order α from the user. According to 15, a certain differentiator is composed of different set of Constant Phase Element

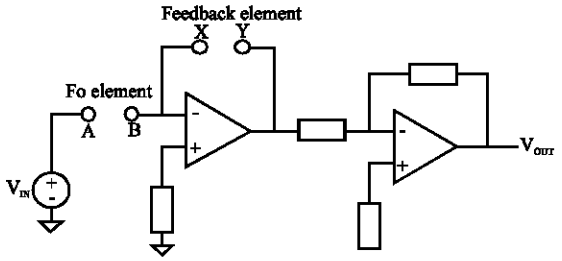

Fig. 3: Schematic overview of a selectable FOD for CPE and R_F paths

(CPE) and Feedback Resistor (RF) circuit corresponding to the selected order. For instance, the fractional order $\alpha = 0.20$ requires a CPE (0.20) and RF (0.20) and likewise an order $\alpha = 0.80$ needs a CPE (0.80) and RF (0.80) to perform their corresponding differentiation.

The selector module is basically a circuit switch that connects or breaks the flow of current to sub-circuit/s in the system. Due to the fact that the selected order necessitates the change of RC ladder network and feedback resistor, there will be two sets of selector module circuits for both the arm (pins A and B) and feedback (pins X and Y) paths of the operational amplifier shown in Fig. 3.

Optimization of CPE by employing reusability of resistor and capacitor: In this study, aside from having the value of C_1 and R_1 common to all four orders considered, reusing of capacitors and resistors has also been a major factor to attain a comparably smaller physical layout. In essence, reusing of capacitors and resistors simply means the utilization of some values of capacitors/resistors to two or more FOD in switching from one order to the next.

It is very known that resistors connected in series will add up like wise while capacitors connected in parallel. Those are the basic theorems that were used to employ resistor and capacitor reusability.

Considering for instance two orders 0.20 and 0.40, the value of R_p-D_0 which is 75945.93 Ω (Table 3) used in FOD (0.20) could be totally used again for FOD (0.40). By connecting R_p-D_1 which 104,784.86 Ω in series to the reused R_p-D_0, the necessary R_p = 180.730.79 Ω (Table 2) could be generated. The switching for the remaining branches (R_2-R_5) is somewhat similar. The only difference is that it is in a reverse manner due to the inverse relationship of the resistor values to the order of differentiation. For the capacitor values, the value of C_2-D_0 equivalent to 13.797 nF (Table 3) used in FOD (0.20) could be reused for FOD (0.40). Thus, instead of using a total of C_2 = 19.037 nF for FOD (0.40), a parallel capacitor C_2-D_1

Table 3: Resistance and capacitance difference for actual CPE array

Variables	D_0	D_1	D_2	D_3
R_1	$R_1(0.80)$ 200000.00 Ω	$R_1(0.60)$-$R_1(0.80)$ 0.00 Ω	$R_1(0.40)$-$R_1(0.60)$ 0.00 Ω	$R_1(0.20)$-$R_1(0.40)$ 0.00 Ω
R_2	$R_2(0.80)$ 55189.19 Ω	$R_2(0.60)$-$R_2(0.80)$ 20956.97 Ω	$R_2(0.40)$-$R_2(0.40)$ 28914.95 Ω	$R_2(0.20)$-$R_2(0.40)$ 39894.82 Ω
R_3	$R_3(0.80)$ 55229.23 Ω	$R_3(0.60)$-$R_3(0.80)$ 13761.96 Ω	$R_3(0.40)$-$R_3(0.60)$ 26198.00 Ω	$R_2(0.20)$-$R_2(0.40)$ 49871.93 Ω
R_4	$R_4(0.80)$ 4202.44 Ω	$R_4(0.60)$-$R_4(0.80)$ 6835.39 Ω	$R_4(0.40)$-$R_4(0.60)$ 17953.35 Ω	$R_4(0.20)$-$R_4(0.40)$ 47154.97 Ω
R_5	$R_5(0.80)$ 1159.65 Ω	$R_5(0.60)$-$R_5(0.80)$ 3042.80 Ω	$R_5(0.40)$-$R_5(0.60)$ 11026.79 Ω	$R_3(0.20)$-$R_5(0.40)$ 39959.95 Ω
R_p	$R_p(0.20)$ 75945.93 Ω	$R_p(0.40)$-$R_p(0.20)$ 104784.86 Ω	$R_p(0.60)$-$R_p(0.40)$ 144574.77 Ω	$R_p(0.80)$-$R_p(0.60)$ 199474.10 Ω
C_1	$C_1(0.20)$ 50.00 nF	$C_1(0.40)$-$C_1(0.20)$ 0.00 nF	$C_1(0.60)$-$C_1(0.40)$ 0.00 nF	$C_1(0.80)$-$C_1(0.60)$ 0.00 nF
C_2	$C_2(0.20)$ 13.797 nF	$C_2(0.40)$-$C_2(0.20)$ 5.2392 nF	$C_2(0.60)$-$C_2(0.40)$ 7.2287 nF	$C_2(0.80)$-$C_2(0.60)$ 9.9737 nF
C_3	$C_3(0.20)$ 3.8073 nF	$C_3(0.40)$-$C_3(0.20)$ 3.4405 nF	$C_3(0.60)$-$C_3(0.40)$ 6.5495 nF	$C_3(0.60)$-$C_3(0.60)$ 12.468 nF
C_4	$C_4(0.20)$ 1.0506 nF	$C_4(0.40)$-$C_4(0.20)$ 1.7088 nF	$C_4(0.60)$-$C_4(0.40)$ 4.4883 nF	$C_4(0.60)$-$C_4(0.60)$ 11.789 nF
C_5	$C_5(0.20)$ 289.91 pF	$C_5(0.40)$-$C_5(0.20)$ 760.70 pF	$C_5(0.60)$-$C_5(0.40)$ 2.7567 pF	$C_5(0.60)$-$C_5(0.60)$ 9.9900 pF
C_p	$C_p(0.20)$	$C_p(0.40)$-$C_p(0.20)$	$C_p(0.60)$-$C_p(0.40)$	$C_p(0.60)$-$C_p(0.60)$

Table 4: Summation of resistance and capacitance differences

Orders	0.20	0.40	0.60	0.80
R_1	R_1 (D_0)	R_1 (D_0)	R_1 (D_0)	R_1 (D_0)
R_2	$\sum$ (R_2 (D_0):R_2 (D_3))	$\sum$ (R_2 (D_0):R_2 (D_2))	$\sum$ (R_2 (D_0):R_2 (D_1))	R_2 (D_0)
R_3	$\sum$ (R_3 (D_0):R_3 (D_3))	$\sum$ (R_3 (D_0):R_3 (D_2))	$\sum$ (R_3 (D_0):R_3 (D_1))	R_3 (D_0)
R_4	$\sum$ (R_4 (D_0):R_4 (D_3))	$\sum$ (R_4 (D_0):R_4 (D_2))	$\sum$ (R_4 (D_0):R_4 (D_1))	R_4 (D_0)
R_5	$\sum$ (R_5 (D_0):R_5 (D_3))	$\sum$ (R_5 (D_0):R_5 (D_2))	$\sum$ (R_5 (D_0):R_5 (D_1))	R_5 (D_0)
R_p	R_p (D_0)	$\sum$ (R_p (D_0):R_p (D_1))	$\sum$ (R_p (D_0):R_p (D_2))	$\sum$ (R_p (D_0):R_p (D_3))
C_1	C_1 (D_0)	C_1 (D_0)	C_1 (D_0)	C_1 (D_0)
C_2	C_2 (D_0)	$\sum$ (C_2 (D_0):C_2 (D_1))	$\sum$ (C_2 (D_0):C_2 (D_2))	$\sum$ (C_2 (D_0):C_2 (D_3))
C_3	C_3 (D_0)	$\sum$ (C_3 (D_0):C_3 (D_1))	$\sum$ (C_3 (D_0):C_3 (D_2))	$\sum$ (C_3 (D_0):C_3 (D_3))
C_4	C_4 (D_0)	$\sum$ (C_4 (D_0):C_4 (D_1))	$\sum$ (C_4 (D_0):C_4 (D_2))	$\sum$ (C_4 (D_0):C_4 (D_3))
C_5	C_5 (D_0)	$\sum$ (C_5 (D_0):C_5 (D_1))	$\sum$ (C_5 (D_0):C_5 (D_2))	$\sum$ (C_5 (D_0):C_5 (D_3))
C_p	C_p (D_0)	$\sum$ (C_p (D_0):C_p (D_1))	$\sum$ (C_p (D_0):C_p (D_2))	$\sum$ (C_p (D_0):C_p (D_3))

equivalent to 5.2392 nF is switched to add up with the reused C_2-D_0. The capacitor switching is quite more complex though compared to the resistors as it requires sets of OR gates for it to be realized. Same applies with the remaining branches (C_3-C_5 and C_p).

In general, this scheme could be extended for a higher number of differentiation orders taken into consideration. Table 3 summarizes all the values of resistors and capacitors required after employing reusability for a selectable four fractional orders. Table 4 summarizes the summation of resistance and capacitance differences needed for every order.

Figure 4 shows the top level schematic of a selectable fractional order differentiator. Apparently, reusability requires quite a lot of transmission gate in its realization. This is on the other hand not a problem considering that the layout implementation of a transmission gate is extensively much smaller compared to capacitor.

In this study, aside from having the value of C_1 and R_1 common to all four orders considered, reusing of capacitors and resistors has also been a major factor to attain a comparably smaller physical layout. In essence, reusing of capacitors and resistors simply means the utilization of some values of capacitors/resistors to two or more FOD in switching from one order to the next.

Feedback resistor consideration: The ideal magnitude of an FOD is 0 dB at ω = 1 rad/sec. However, since, the ladder may not perform well at ω = 1 rad/sec, it is more practical to calibrate the FOD circuit at the average frequency (Gonzalez *et al*., 2014). The average frequency ω_{av} can be computed using the equation shown in Table 2. For instance, if the order of choice is 0.20, the average frequency is around 5590.2 rad sec or equivalent to 890 Hz. Since, the nearest decade point is at 1 kHz, the magnitude of the gain should be at $|G(j\omega)|\ \omega = 2\pi\ (1000) = \omega^{0.2}|\ \omega = 2\ \pi\ (1000) = 5.7496$ which is around 15.19 dB. Table 5 summarizes the corresponding magnitude gain for four orders in the frequency band of interest (10, 100 Hz and 1 kHz).

Table 5: Corresponding magnitude gain for four fractional orders in the frequencies (dB): 10, 100 Hz and 1 kHz

Orders	10 Hz	100 Hz	1 kHz
0.20	7.190	11.19	15.19
0.40	14.39	22.39	30.39
0.60	21.58	33.58	45.58
0.80	28.77	44.77	60.77

The value of the feedback resistor R_F must be chosen to meet the required magnitude gain. Considering the FOD with an order 0.40 as an example, the feedback resistor is identified to research at approximately 600 kΩ. In the IC layout point of view, this occupies large area. Thus for this study, R_F value was reduced to one-third of the original value but the post-cascaded inverting amplifier should have a gain three times larger relative to its original value in order to cancel the reduction in the R_F value.

The final value of the feedback resistors is as follows, order 0.2, R_F = 51 kΩ, order 0.4, R_F = 206 kΩ, order 0.6, R_F = 531 kΩ and order 0.8, R_F = 804 kΩ.

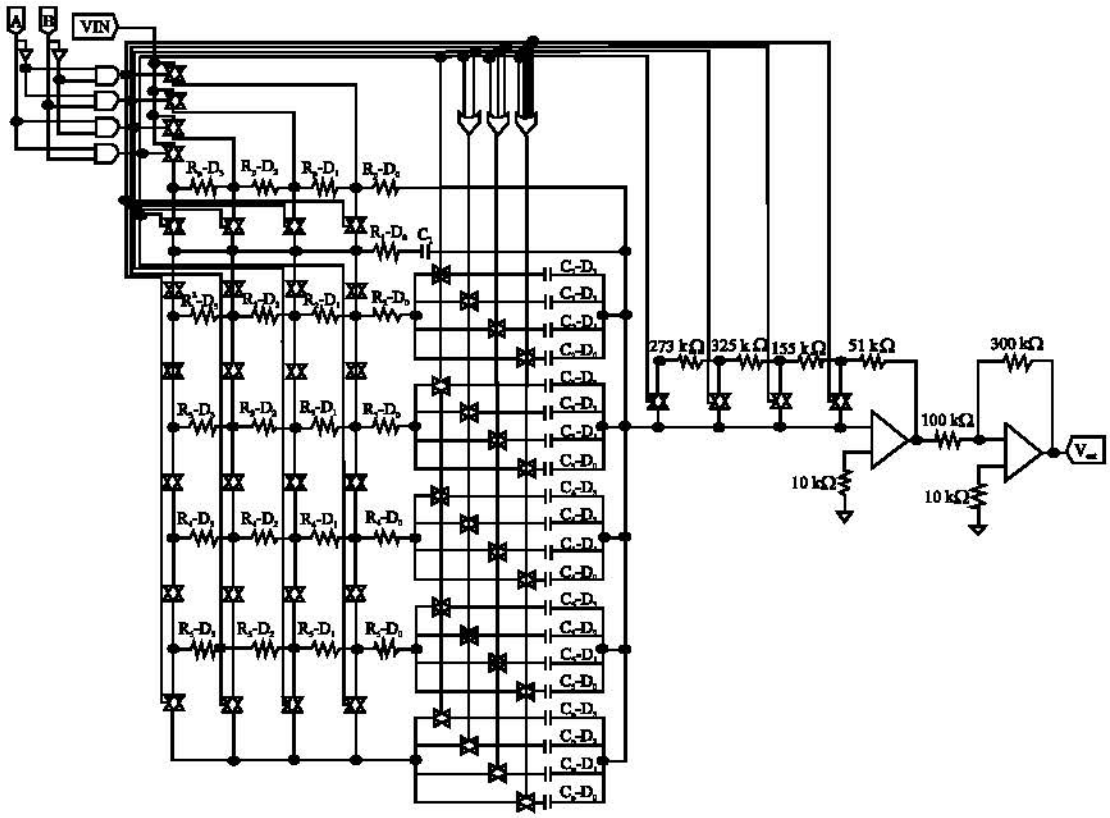

Fig. 4: Top level schematic of a selectable FOD

RESULTS AND DISCUSSION

Complementary Metal Oxide Semiconductor (CMOS) analog realization of a selectable FOD: This study focused on the realization of a selectable (FOD) implemented on a single Integrated Circuit (IC) design layout similar to the one presented by Abad *et al*. Discrete components used in Fig. 4 have been designed and implemented on a microelectronics scale. Tanner Software was used to produce a single chip layout. Layout Versus Schematic (LVS) and Design Rule Check (DRC) were used as layout verification tools.

Operational Amplifier (OpAmp) CMOS module: The low voltage op-amp topology (Yap, 2009) shown in Fig. 5 was adopted for this study. The op-amp can research at a voltage supply of 1.5 V which is low compared to the typical 3.3 V for the 0.35 μm technology library. The adopted Op-Amp can be operated either by using unipolar (1.5 V-gnd) or bipolar supply (+/-0.75 V). Computations of transistor sizes were based on (Yap, 2009; Allen and Holberg, 2002).

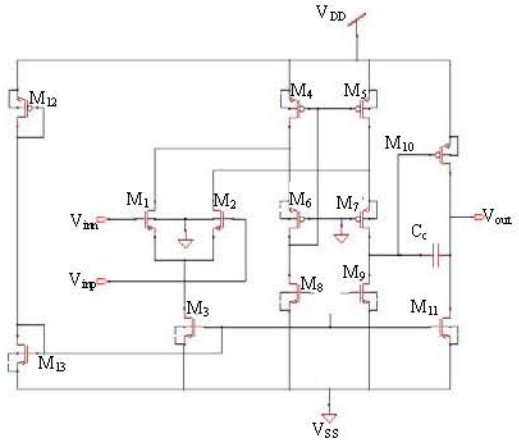

Fig. 5: Op-amp low voltage design

Figure 6 presents the layout of the inverting amplifier with its Compensation Capacitor (CC). The op-amp in this design was laid out with a guard ring wrapped around. It prevents noise from entering digital circuits whereas it prevents noise from getting out of it for analog (Atendido *et al*., 2014).

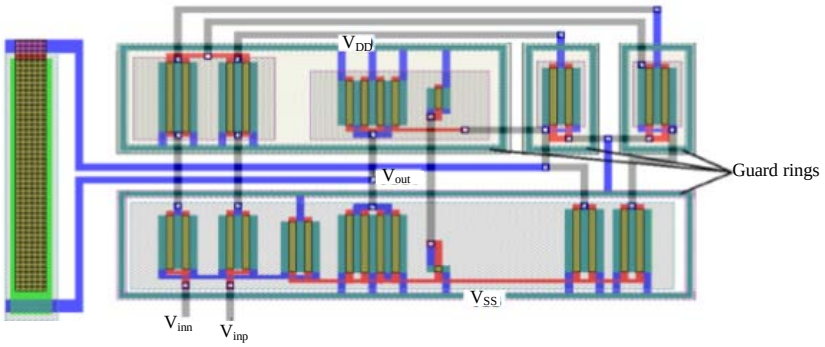

Fig. 6: Layout of a low-voltage op-amp with guard rings

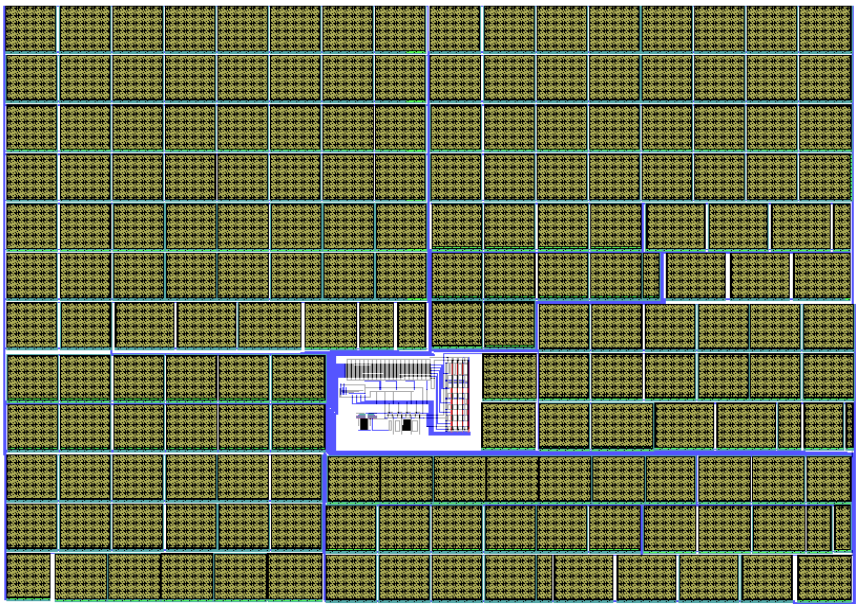

Fig. 7: Top-level layout of a selectable FOD

CMOS layout view of a selectable FOD: Figure 7 shows the whole chip layout of the design of a selectable FOD with 4 possible orders. It has a dimension of 8.10×6.30 mm or equivalent to a final area of 51.03 mm^2. NMOS capacitor of the constant phase element occupies almost 95% of the overall design area. Only 5% of the area is occupied by the inverting OP AMP, set of resistors and digital logic gates including AND and OR gates, inverter and transmission gates. Although, the design utilizes 52 switches in expense of employing reusability, this has negligible effect as far as overall layout area is concerned.

Figure 8 presents the phase and magnitude response for the differentiation orders 0.20, 0.40, 0.60 and 0.80. The range of operation in which the FOD is applicable is between 10 Hz to around 1 kHz. Yet not all FODs are working for this whole frequency band of interest. Theoretically, the RC ladder can perform the desired constant phase element. However when incorporated in an Op-Amp circuit, the range of frequencies diminishes due to the characteristics and Gain-Bandwidth-Product (GBP) limitation of the op-amp. For higher bandwidth applications, a design of op-amp with higher GBP is necessary.

Transient response of the design was also analyzed using a sinusoidal input signal. Figure 9 shows the output signal for an input signal $V_{in} = 5 \sin (120\ \pi t)$ mV where the frequency was set to 60 Hz.+

Table 6 summarized the transient response in terms of output peak voltage and its corresponding phase shift relative to the input signal.

Table 6: Summary of transient response analysis

Order	FOD gain at 60 Hz	Ideal transient response	Simulation transient response
FOD (0.20)	3.28	V_{pk} = 16.40 mV, φ = 18.0°	V_{pk} = 16.45 mV, φ = 17.50°
FOD (0.40)	10.73	V_{pk} = 53.65 mV, φ = 36.0°	V_{pk} = 53.27 mV, φ = 35.30°
FOD (0.60)	35.14	V_{pk} = 175.7 mV, φ = 54.0°	V_{pk} = 178.33 mV, φ = 52.90°
FOD (0.80)	115.10	V_{pk} = 575.5 mV, φ = 72.0°	V_{pk} = 521.06 mV, φ = 70.20°

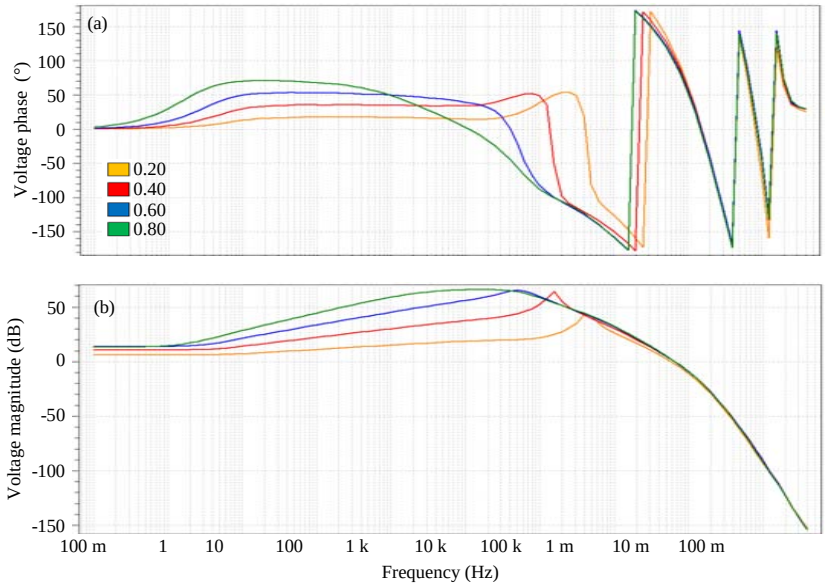

Fig. 8: a) Phase response for 4 FOD and b) Magnitude response for 4 FOD

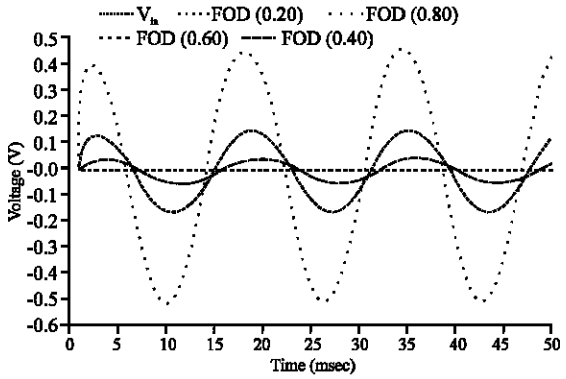

Fig. 9: Transient response for selectable 4 FODs

CONCLUSION

In this study, a design of a low-voltage selectable Fractional-Order Differentiator (FOD) has been conceptualized and implemented in a 0.35 μm CMOS technology. The design was successfully realized in an analog microelectronic scale, thus, relatively smaller. The dimension was further reduced by employing reusability of capacitors and resistors when switching from one order to the next. The final physical layout of the design using L-Edit has a dimension of 8.10×6.30 mm or equivalent to only 51.03 mm^2. This is just almost 50% of the foreseen final area of 108.60 mm^2, i.e. without employing reusability and far much smaller than a selectable FOD using microcontroller. Some of the orders only operate from 10-100 Hz while others are from 100-1 kHz. This is due to the gain-bandwidth limitation of the op-amp.

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