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Performance Analysis of Single Phase Closed Loop System for Cascaded H-Bridge Multilevel Inverter Using Renewable Source

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Abstract: This study presents a closed loop "Synchronous Reference Frame" (SRF) control method using seven level cascaded H-bridge multilevel inverter for a single phase grid connected photovoltaic system. The proposed control scheme is obtained in order to inject quality current to the grid connected system. This method can generate the sinusoidal current which reduces the total harmonic distortion. The control strategy allows independent control of each DC-link voltage. In addition, it tracks the maximum power point of PV strings. The simulation results for seven level CHB-MLI for 555 W/230 V/50 Hz is presented to validate the proposed control scheme. Simulation is done using MATLAB Simulink platform.

Key words: Photo Voltaic (PV), Maximum Power Point Tracking (MPPT), DC link capacitor, boost converter, cascaded H-bridge multilevel inverter, PI controller, "Synchronous Reference Frame" (SRF)

INTRODUCTION

Renewable energy, particularly solar energy is becoming popular and attractive due to the energy crisis and environmental issues caused by conventional energy sources. Solar energy in the form of light can be converted to DC electricity using Solar Photo-Voltaic (SPV) cells. The voltage generate by a single solar cell is around 0.5 V. Multiple solar cells are interconnected to obtain desired level of PV output. The prominent feature of a multilevel inverter is its ability to generate sinusoidal like AC voltage from multiple DC voltage levels. Therefore, multilevel inverters are considered most suitable for grid connected photovoltaic system employing distributed MPPT (Xiao *et al*., 2012) algorithm.

Throughout the day the intensity and angle of sunlight falling on the PV module is varying leading to a varying output voltage. This voltage has to be converted to a fixed level through a boost converter (Erickson and Dragan, 2012; Devi and Srivani, 2016) using MPPT algorithm. Among various MPPT methods Perturb and observe method and incremental and conductance algorithm are mostly used due to their simplicity and accuracy (Hohm and Ropp, 2003; Kirthika and SrivaniIyengar, 2015; Pachpande and Zope, 2012; Cherif and Hamrouni, 2007). The fixed DC voltage from the chopper circuit (Mohan *et al*., 2012) is converted to an AC voltage by means of multilevel inverter which is suitable for medium and high power application (Rodriguez *et al*., 2002; Tolbert and Peng, 2000; Calais *et al*., 2002; Choi *et al*., 1991; Kjaer, 2005). An ideal inverter design is void of transformers to improve the efficiency and reduce the size and cost (Alajmi *et al*., 2013). Out of many available Pulse Width Modulation (PWM) methods for the inverter switches, carrier based sinusoidal PWM is found most suitable (Lawan and Abbas, 2015; Bin, 2006). For the closed loop scheme the reactive current reference of d-q based controller is set to zero and active current reference is based on the active power to be supplied to the grid (Prabhu *et al*., 2016).

This study proposes to analyse performance of a single phase seven level CHB multilevel inverter using solar energy source. Three control schemes are envisaged to improve the overall efficiency and reduce Total Harmonic Distortion (THD) of the system. The incremental conductance method is used to extract the maximum power from PV, "Synchronous Reference Frame" (SRF) control is incorporated to feed only active power in to the grid and Level Shifted PWM (LSPWM) multicarrier topology is used for the generation of PWM pulses for the inverter switches.

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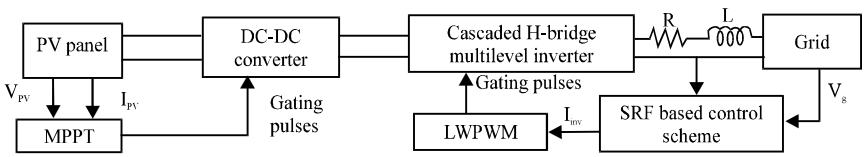

Fig. 1: Block diagram of single phase grid connected PV system

System description: The main aim of this study is to improve the overall efficiency of the system and to reduce the total harmonic distortion without any usage of the transformer. Hence, the system is designed in three modules along with three control schemes. The block diagram of the system is shown in Fig.1.

PV module at the beginning provides the required input DC power to the system. This study considers CHSM5612M PV module with a maximum output power of 185 W at MPP of 36.38 V. A DC-DC converter module at the second stage amplifies the DC voltage to 110 V. The PWM pulses for the converter is generated by the MPPT control module. The third module is the CHB inverter. A cascaded multilevel inverter with 'n' levels should have '(n-1)/2' input sources to generate the required AC output waveform (Rodriguez *et al*., 2002; Tolbert and Peng, 2000). Increasing the value of 'n' would reduce the harmonics in the system. In order to improve the stability of the grid only active power from the inverter is passed on to the grid by maintaining Voltage of the grid (V_g) and current of Inverter (I_{inv}) in-phase with each other. "Synchronous Reference Frame (SRF)" control scheme is envisaged to achieve this. The SRF based algorithm provides reference sine wave for the Level Shifted PWM (LSPWM) module which in turn generates the gating pulses for the inverter switches. There are many methods to generate LSPWM pulses (Bin, 2006; Lawan and Abbas, 2015), Phase Disposition PWM (PDPWM) technique is considered in this study. The output of inverter is connected to the grid.

MATERIALS AND METHODS

Design and analysis of the system: The design of grid connected single phase cascaded multilevel inverter includes PV module, boost converter, cascaded H-bridge multilevel inverter, DC link capacitor and the closed loop control using SRF method.

PV module: A PV module is normally a series of connected solar cells designed to provide required output voltage and power. PV module with different power rating (3-300 W) is available commercially. This study considers CHSM5612M PV Module with a maximum power output of 185W at V_{MPP} of 36.38 V The main factors

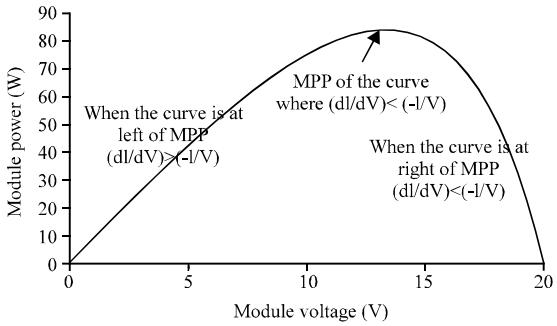

Fig. 2: PV curve for MPPT

considered for PV panel design are sun irradiance and cell temperature which are taken as inputs to PV array. A required feature of a PV system is the ability to track the Maximum Power Point (MPP) of the PV array. MPP tracking is desirable in both standalone and grid connected PV systems because the solar irradiance and temperature changes throughout the day.

Distributed MPPT control: The "Maximum Power Point" (MPP) is the point on the P-V curve of a PV Module at which it operates with maximum output power (Hohm and Ropp, 2003). MPP varies with change in solar irradiance levels and temperature of the PV module. In order to operate PV Module effectively MPP should be maintained always. Main function for the MPPT is to control the PV system to run it near its MPP. Many algorithms are available to track MPPs and Incremental Conductance (INC) method is applied in this study. In INC method, the PV module voltage is tuned to maintain operation at MPP voltage. Set of rules are determined from the PV curve shown in Fig. 2.

$$\frac{dP}{dV} = \frac{d(IV)}{dV} = I + V\left(\frac{dI}{dV}\right) \quad (1)$$

The MPP can be tracked by comparing the instantaneous conductance (I/V) to the incremental conductance (dI/dV) because at MPP dP/dV = 0.

The flowchart at Fig. 3, depicts the algorithm of INC method for MPP tracking. The dV and dI values are derived by comparing V(k) and I(k) of present and previous cycle. Following conditions are verified and the voltage is adjusted accordingly to maintain MPP.

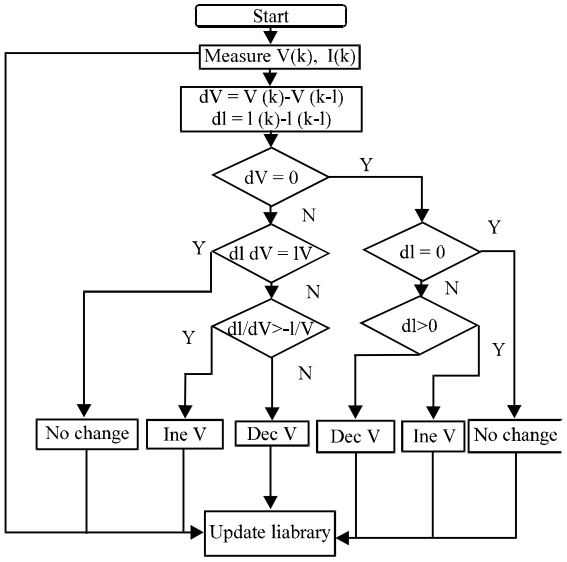

Fig. 3: Incremental conductance method flow chart

If dV≠ 0 and dI = 0, then that point is the MPP. If dv = 0 and dI>0, then the point of operation is left of MPP, If dV ≠ 0 and dI<0, then the point of operation is right of MPP.

If dV = 0 and dI/dV = -I/V, then that point is the MPP. If dv ≠ 0 and dI/dV> -I/V, then the operating point is left of MPP. If dv ≠ 0 and dI/dV< -I/V, then the operating point is right of MPP.

In order to maintain the MPP, the operating point has to move in same direction when the operating point is left of MPP and to the opposite direction when it is right of MPP.

Boost converter: The circuit of boost converter is shown in Fig. 4 where V_s is the source Voltage, L is the inductor, S is the Switch, D is the Diode, C is the Capacitor, R is the load Resistor and V_o is the output Voltage. The switching on period is T and the switch is closed for time 'dT' and open for '(1-d) T' (Hohm and Ropp, 2003).The input and output voltages are expressed using Eq. 2 where 'd' is the duty ratio (Mohan *et al*., 2012).

$$V_0 = \frac{V_s}{1\text{-}d} \quad (2)$$

From Eq. 2, d = 0 if the switch is always open. Hence, the output and input voltage is equal. As the duty ratio increases, value of 1-d reduces thereby increasing the output voltage. Average current in the inductor is determined by the fact that the average power supplied by the source must be equal to the average power consumed by the load (R). Design parameters for the boost converter is shown in Table 1.

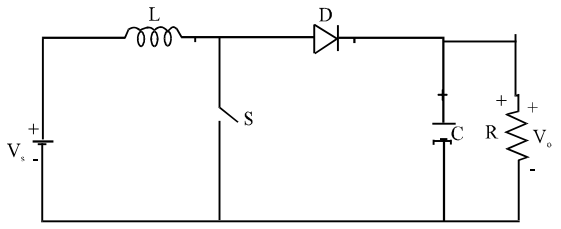

Fig. 4: Circuit diagram of boost converter

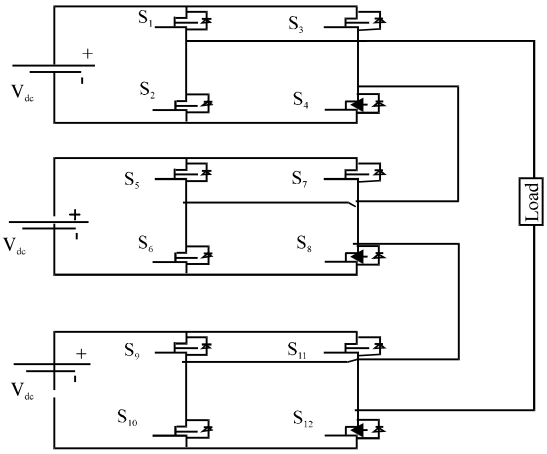

Fig. 5: Single phase seven level CHB MLI

Table 1: Boost converter parameters

Parameters	Values
Source voltage	36.38 V
Output voltage (V_0)	110 V
Switching frequency	20 kHz
Change in Inductor current (ΔI_L)	40% of I_L
Output voltage ripple	1% of V_0
Inductor current (I_L)	5.39 A
Duty ratio (d)	67 (%)
Inductor (L)	500 µH
Capacitor (C)	52 µF

Cascaded H-bridge multilevel inverter: For the single-phase inverters each inverter level with 'V_{dc}' as the DC voltage of each H-bridge can provide three different voltage outputs; $+V_{dc}$, 0 and $-V_{dc}$ (Rodriguez *et al*., 2002; Choi *et al*., 1991). With different combinations of the four switches in each H-bridge module, the output voltage ranges from $-3V_{dc}$ to $+3V_{dc}$. Figure 5 shows switch connections where S_1-S_{12} are the switches for the H-bridge circuit. The switching pattern for the same is shown in Table 2.

Design of DC-link capacitor: The design of DC-link capacitor is the main limiting factor of the inverter lifetime. It provides the connection between the input and inverter, prevents the transients from the load going back to input

Table 2: Switching pattern of seven level inverter

Volt level	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	S_{10}	S_{11}	S_{12}
3 V_{dc}	ON	OFF	OFF	ON	ON	OFF	OFF	ON	ON	OFF	OFF	ON
2 V_{dc}	ON	OFF	OFF	ON	ON	OFF	OFF	ON	ON	OFF	ON	OFF
V_{dc}	ON	OFF	OFF	ON	ON	OFF	ON	OFF	ON	OFF	ON	OFF
0	ON	OFF	ON	OFF	ON	OFF	ON	OFF	ON	OFF	ON	OFF
-V_{dc}	OFF	ON	ON	OFF	OFF	ON	OFF	ON	OFF	ON	OFF	ON
-2 V_{dc}	OFF	ON	ON	OFF	OFF	ON	ON	OFF	OFF	ON	OFF	ON
-3 V_{dc}	OFF	ON	ON	OFF	OFF	ON	ON	OFF	OFF	ON	ON	OFF

side and smoothens the DC pulses (Xiao *et al*., 2012). For calculating the DC-link capacitor value after PV module the formula used is:

$$C = \frac{P_{total}}{2 * n * \omega_{grid} * V_{dc} * v_{ripple}} \quad (3)$$

Where:

P_{total} = The total maximum Power of all PV panels
V_{dc} = The MPP Voltage of the PV panels connected to one inverter
v_{ripple} = The amplitude of the Voltage ripple

The DC-link capacitor after boost converter is calculated as:

$$C = \frac{2 * P_{max}}{f_s * V_{dc}^{\ 2} * (1 - k^2)} \quad (4)$$

Where:

P_{max} = The max output Power of boost converter
f_s = The switching frequency
V_{dc} = The output Voltage of boost con6erter
k = Calculated as

$$k = \frac{V_{dc\,min}}{V_{dc}} \quad (5)$$

Design of closed loop system using SRF control: The overall control scheme consists of SRF controller and PI controller.

Synchronous reference frame control: In grid tie inverter, in order to improve the stability of the grid only active power from the inverter is to be passed on to the grid. To achieve this Voltage of the grid (V_g) and current of Inverter (I_{inv}) should be in-phase with each other. "Synchronous Reference Frame (SRF)" control scheme is envisaged for this. Figure 6 depicts the flow of control in SRF scheme. Real-time tracking of phase angle of the Vg is employed using "Phase Locked Loop (PLL)" technique. Consider the following, "I_α" the inverter current and "I_β" 90° out of phase with "I_α". "$V_{g\alpha}$" the grid voltage and "$V_{g\beta}$" 90° out of phase with "$V_{g\alpha}$". Synchronous rotating reference frame (d-q reference frame) is developed from the stationary reference frame (α-β reference frame). $V_{g\beta}$ and I_β is required to be derived to process this transformation:

$$V_{g\alpha}(t) = V\cos(\omega t) \quad (6)$$

$$V_{g\beta}(t) = V\sin(\omega t) \quad (7)$$

Where:

V = The maximum grid voltage
ωt = The real-time phase angle derived by PLL. Derive the value of $I_\alpha(t)$ and $I_\alpha(t)$

$$I_\alpha(t) = I\cos(\omega t + \varphi) \quad (8)$$

$$I_\beta(t) = I\sin(\omega t + \varphi) \quad (9)$$

Where:

I = The maximum Inverter current
Φ = The inverter current phase angle in comparison to the reference

The '**Φ**' value must be brought to zero to synchronise V_g and I_{inv} and transfer only active power to the connected grid. Phase synchronisation is achieved by using α-β to d-q transfer control (Park's transformation theory). Derive the direct current I_d and reactive current I_q as:

$$\begin{bmatrix} I_d \\ I_q \end{bmatrix} = \begin{bmatrix} \cos\theta & \sin\theta \\ -\sin\theta & \cos\theta \end{bmatrix} \begin{bmatrix} I_\alpha \\ I_\beta \end{bmatrix} \quad (10)$$

Therefore, I_d and I_q would be a constant value in proportion with I_α and I_β. When **Φ** = 0, I_d = I and I_q = 0. If maximumum inverter current is I then consider I_d^* as current reference to maintain "**Φ**" at zero. MPPT technique is used to derive I_d^* in solar based power stations. This would enforce balancing of power being drawn from PV modules. As the system is designed to recieve only active power from the inverter, the reactive current to the grid (I_q^*) must be maintained at zero. At a given instance (t) the error signals "$e_d(t)$" and "$e_q(t)$" is derived by comparing reference current and actual current (Prabhu *et al*., 2016).

$$e_d(t) = I_d^* - I_d(t) \quad (11)$$

$$e_q(t) = I_q^* - I_q(t) \quad (12)$$

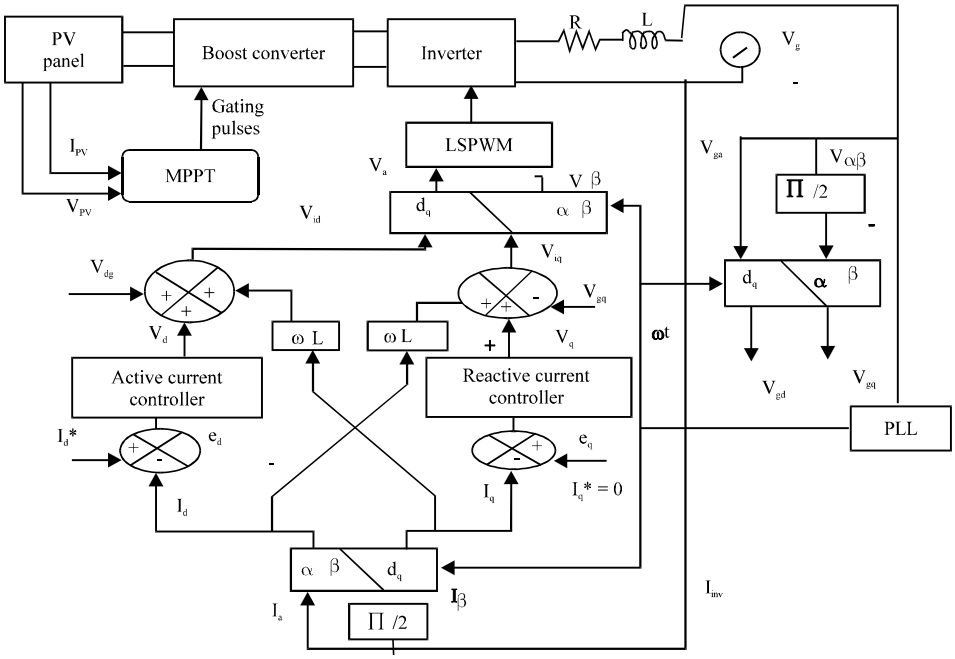

Fig. 6: SRF control scheme

The PI controller receives these error signal to generate voltages V_d and V_q. By applying the voltage balance equation (Lawan and Abbas, 2015).

$$V_{id}(t) = V_{gd} + V_d + \omega L I_q \quad (13)$$

$$V_{iq}(t) = V_{gq} + V_q - \omega L I_d \quad (14)$$

Where V_{id} and V_{iq} are the DC components of the inverter voltage obtained by voltage decoupling. Which are transformed back to stationary reference frame using inverse Park's transformation (V_α and V_β) V_α is the reference signal to the LSPWM generator which intern generates the switching sequences for the grid tie inverter.

PI controller: PI controller is a feedback control loop that calculates an error signal by comparingthe output of a system with a set point. The set point is the level at which the system is running. Block diagram of PI controller is shown at Fig. 7. The controller output is given by:

$$K_p \Delta = K_I \int \Delta dt \quad (15)$$

Δ is the error in instantaneous value (PV) with respect to the set point (sp):

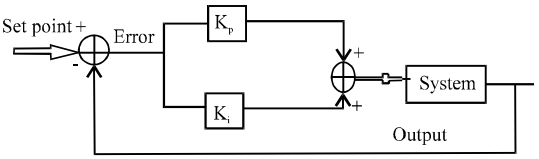

Fig. 7: PI controller block diagram

$$\Delta = sp - PV \quad (16)$$

Laplace transformation can be used to design a PI controller:

$$C = \frac{G(1+TS)}{TS} \quad (17)$$

Where:
G = Kp = Proportional gain
G/T = K_I = Integral gain

In manual tuning first set K_I value to be zero and increase K_p value slightly until the output of the loop oscillates. Then set K_p as half the value and increase K_I. Increasing too much K_I will cause instability. Thus, by proper manual tuning the K_p and K_i values can be set for proper control of system.

RESULTS AND DISCUSSION

Open loop simulation: The main simulation diagram is depicted in Fig. 8. The diagram contains four subsystems.

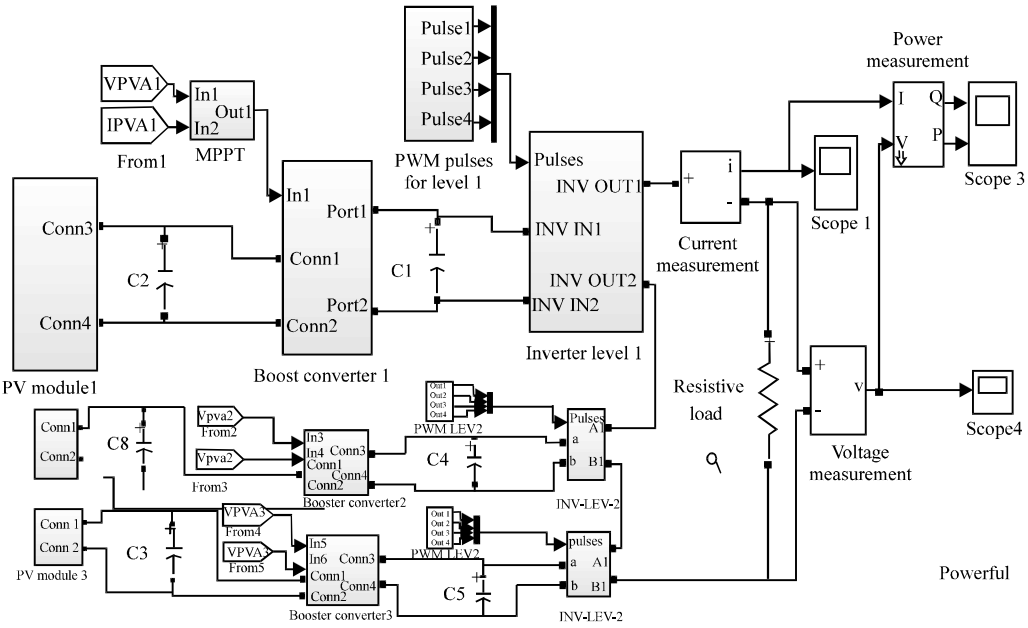

Fig. 8: Open loop simulation diagram

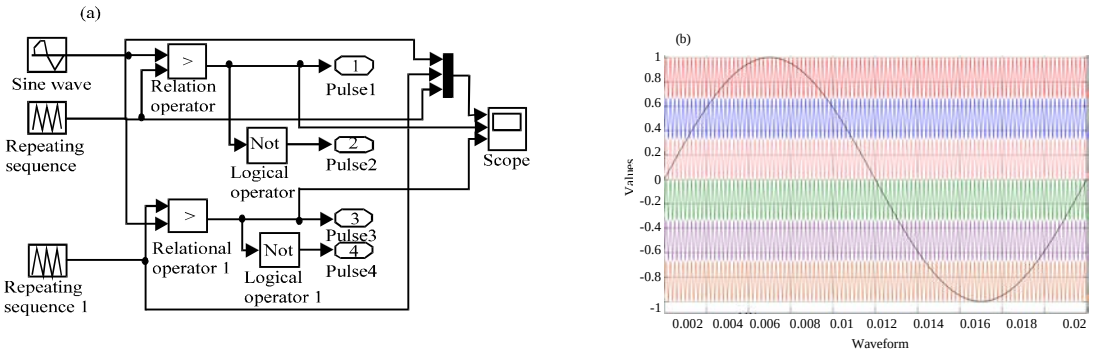

Fig. 9 a, b): Phase disposition simulation and PWM waveform

The subsystem 1 is the modelling of PV module consisting of three PV modules, subsystem 2 the boost converter, subsystem 3 the H-bridge inverter and subsystem 4 the PWM pulse generator for the MOSFET switches of inverter.

Output of boost converterd is connected to an H-bridge inverter. The pulses for inverter switches are generated using level shifted PWM method as shown in Fig. 9. The pulses are generated by comparing a sinusoidal reference signal with the triangular carrier signal. Whenever the reference signal intersects the carrier signal the PWM pulse raises and in the next intersection the pulse falls. This process is reapeated for every intersections.

In seven level inverter the amplitude of output voltage is ranging from -3 V_{dc} to +3 V_{dc}. So, in LSPWM method the amplitude of output voltage is divided in to three parts that is 1/3, 2/3 and 1. Out of many LSPWM methods PD-PWM method shown at Fig. 9 is considered. The gating pulses waveform for the switches are shown in Fig.10.

Closed loop simulation: The output of MPPT control is duty ratio for gating pulse of DC-DC converter. The duty ratio is multiplied by V_{MPP} to obtain reference voltage which is given to a PI controller. The PI controller gives a reference current is used as a reference parameter for SRF control scheme. The simulation diagram is shown in Fig.11.

Simulation results: The simulation results include both open loop and closed loop simulation. The inverter

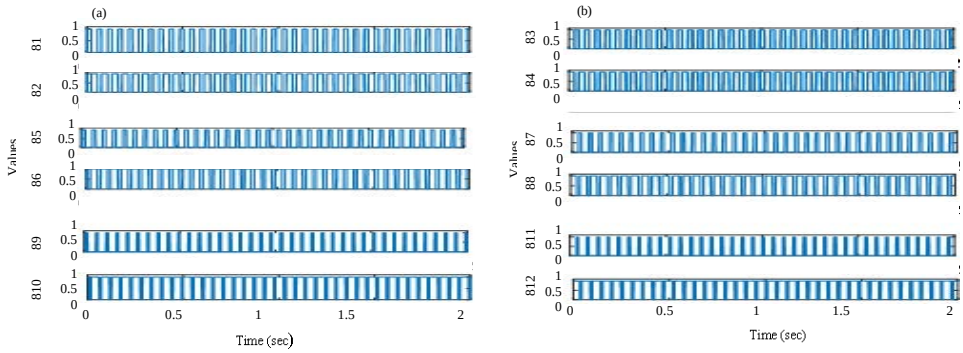

Fig. 10: Gate pulses for each switches of the multilevel inverter

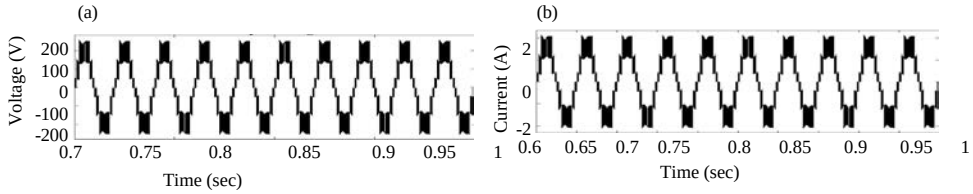

Fig. 11: Open loop inverter output voltage and current Vs time

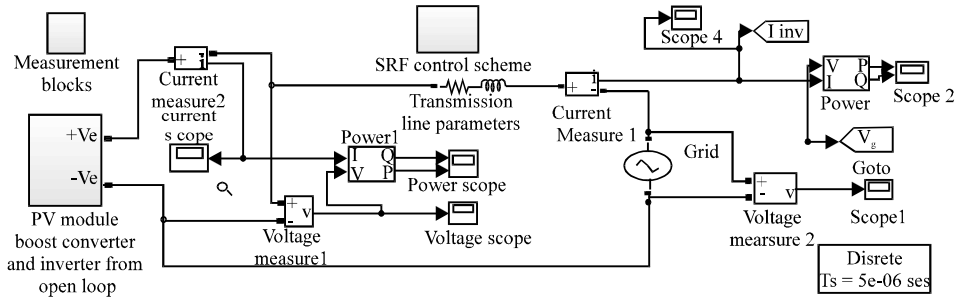

Fig. 12: Closed loop simulation diagram

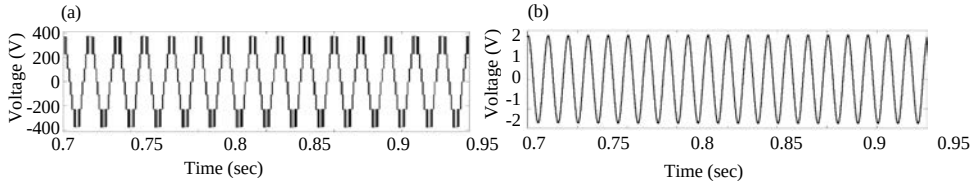

Fig. 13: Closed loop inverter out put voltage and current vs. time

voltage and current wave forms for open loop simulation is shown in Fig. 12. The inverter output voltage is around 280 V and inverter current is 2 A. The closed loop simulation result for inverter output voltage and current is shown in Fig. 13. The inverter voltage appeared to be 380 V and inverter current appeared to be 3 A.

The active and reactive power at the inverter side is shown in Fig. 14. The active power obtained to be 550 W and reactive power considered to be zero because we

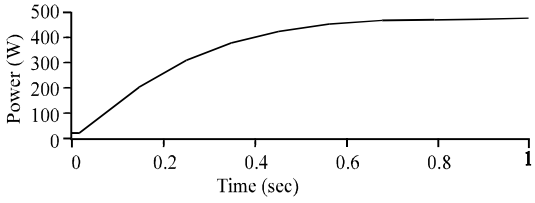

Fig. 14: Active power vs. time

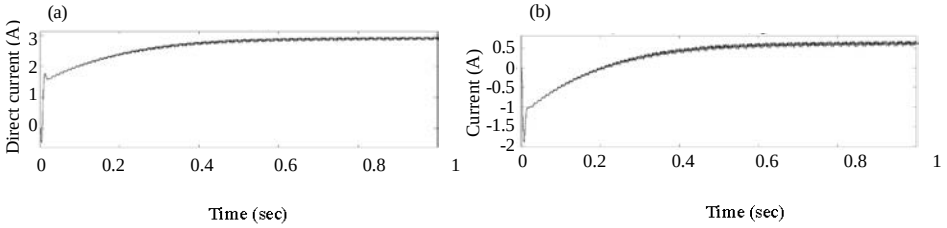

Fig. 15: Direct current vs. time and quadrature axis current vs. time

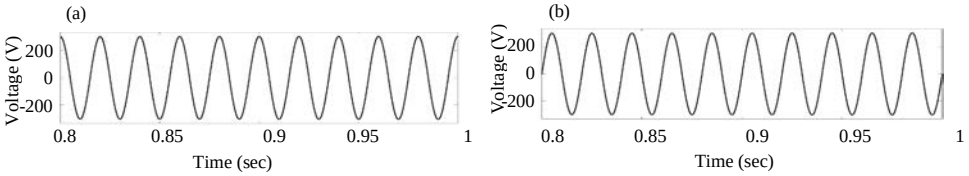

Fig. 16: Alpha and beta components of voltage

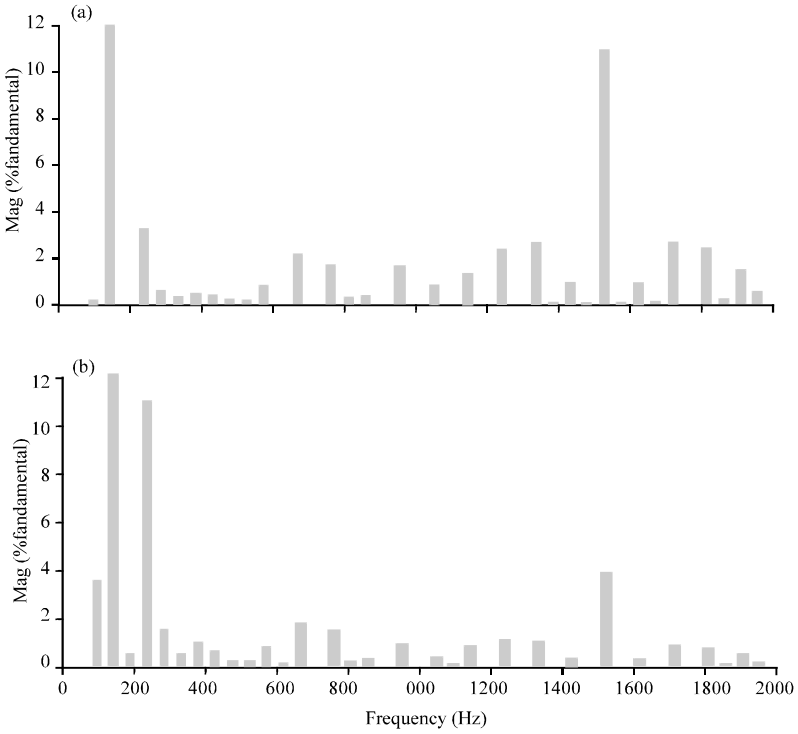

Fig. 17: THD analysis of open loop inverter output voltage and current vs. time. Fundamental (50 Hz) = 223.4, THD = 25.35% FFT analysis

need only active power to be delivered to the grid. The DC components I_d and I_q, the output of Parks transformation in synchronous reference frame are shown in Fig. 15. Here, I_d magnitude is same as inverter output current and I_q is less than I_d. V_α and V_β using inverse parks transformations are used as the reference signal for generating gating pulses for inverter circuit. Here, V_α is same as grid voltage and V_β is in quadrature with V_α. The corresponding waveform is shown in Fig. 16. The harmonics analysis using THD analysis window for the open loop inverter voltage is shown in Fig. 17 with fundamental voltage and current values are 223.4 V and

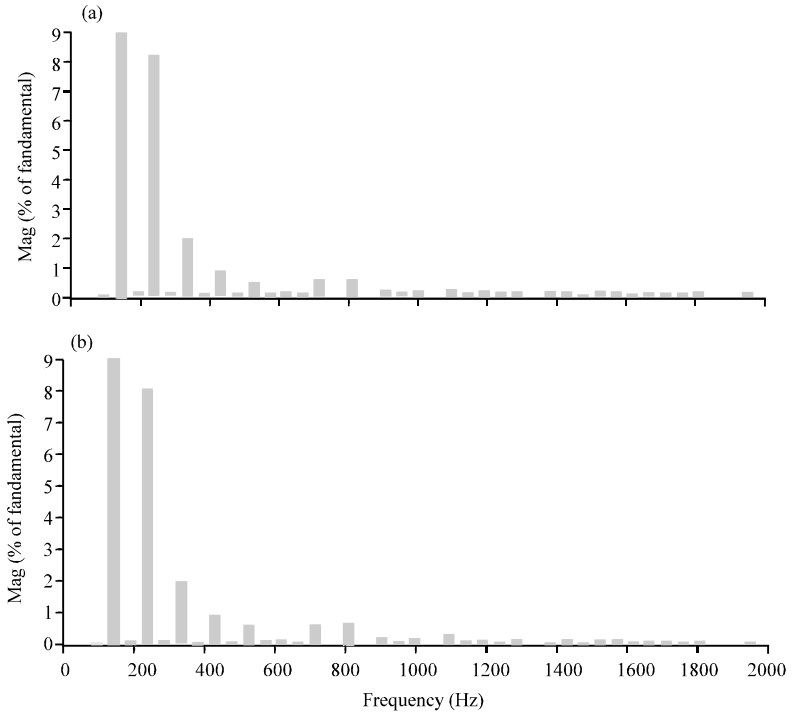

Fig. 18: THD analysis of closed loop inverter voltage and current vs. time. Fundamental (50 Hz) = 367.4, THD 19.37% FFT analysis

1.862 A, respectively. The closed loop analysis for the voltage and current is shown in Fig .18 with fundamental voltage and current values of 367.4 V and 2.923 A, respectively.

CONCLUSION

In this study, a performance analysis of single phase closed loop system for cascaded H-bridge multilevel inverter using renewable source has been presented. Individual MPPT control is enforced for each PV module towards increasing the efficiency of the PV systems. "Synchronous Reference Frame (SRF)" control is enforced to transmit only active power from inverter. Level Shifted PWM (LSPWM) multicarrier topology is used for generation of PWM pulses for the inverter switches.

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