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Analysis of DCVS and MODL Logic in CLA

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Abstract: This study deals about 4 bit carry look ahead adder implementation in differential cascade voltage switch and multi output domino logic styles. The main idea of Manchester carry chain is splitting the carry into odd and even parts for reducing the delay time for carry bit to increase the speed of the circuit. The DCVS and MODL logic styles are analyzed in terms of power, delay and power delay product with supply voltages 0.8-1.8 V and temperature 27°C at 180 nm technology.

Key words: DCVS, MODL, MCC, CLA, CMOS logic, low power VLSI

INTRODUCTION

The flexibility and high logic density is the two main reasons for choosing differential cascade switch logic. Differential cascade switch logic is mainly preferred for digital implementation. The drawback of DCVS logic is poor driving capability. The effect of process corners and temperature variations are investigated in ternary logic (Mirzaee *et al*., 2013). The full adder was designed by using 14T adder based on XOR/XNOR modules by hybrid combination of pass transistor logic and DCVS logic. The level restoration was achieved at the driving stage (Bazzazi and Eskafi, 2010). The high speed 2×2 multiplier was designed by using DCVS logic styles. The simulation was carried out BSIM3v3 Model in Tanner Software (Gupta *et al*., 2012).

The energy consumption of modern digital CMOS circuits has been traditionally dominated by switching energy having quadratic dependence on supply voltage, voltage scaling is an effective way to minimize the overall energy consumption of system-on-a chip. The BCDL provides better switching transition than the conventional logic style at threshold voltage regions and it reduces foot print of the silicon chip (Mani *et al*., 2013).

The functional power of the differential logic trees reduces the device redundancy. The different types of DCVS logic families are static and dynamic differential voltage switch logic are analyzed and results are verified by using layout techniques (Roy, 2015). The ULPD and complementary pass transistor logic based DCVSL introduced for low power designs. The simulation was carried out by using 180 nm technologies. The ULPD was designed using depletion type MOSFETs. This technique is used to reduce leakage current when compared to standard diode connected MOSFETs (Srinivasulu and Rajesh, 2013; Chanda *et al*., 2011).

The combination of adiabatic logic and DCVS logic are applied to multipliers for better energy consumption (Efstathiou *et al*., 2013). For wide adder speed is important concern. In order to increase the speed of the adder, the concept of multi output domino logic was incorporated (Ajane *et al*., 2011). Based on the input signal it decides the carry is propagated to next stage or it is kill the carry bit. The approach is named as Manchester carry chain and it is applied to pseudo random noise sequence generator (Nehru and Shanmugam, 2014). The simulations have taken as reference from proposed ALU structure.

MATERIALS AND METHODS

Four bit MCC: The 4 bit MCC is mainly used to reduce to computation time. The 4 bit MCC can perform the operation of 16 bit CLA. The MCC is mainly used to reduce the number of transistor count by using shared logic.

Domino implementation for the generate: Figure 1 shows the implementation of generation signal using domino logic. In the output stage INVX 1 cell is connected to the output for cascading purpose. The PM3 pull up transistor and inverter cell are used for full swing restoration at output node. The main advantage of domino logic is to start evaluating the output, only the clock signal is enter into evaluation mode.

Domino implementation for XOR propagate: The propagate signal implemented in domino logic is shown in Fig. 2. In the XOR gate implementation, the pull down

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module is consisting of only NMOS transistors. The NMOS is used for discharging the output load capacitance at evaluation mode.

Conventional Manchester carry chain adder: The conventional 4 bit Manchester carry chain adder is consist of propagate and generated signals and it is shown in Fig. 3. The computation time is mainly depends on the group propagate and group generate computation time. In general complexity of adder is increased based on the number of bits.

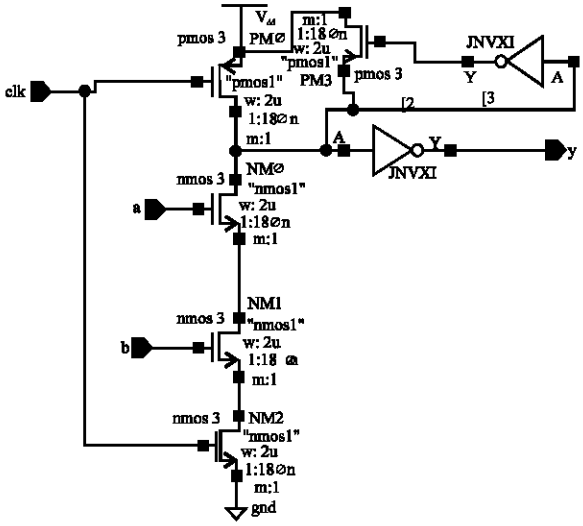

Fig. 1: Domino implementation for the generate signal

Bit CLA CMOS adder in multi output DCVS logic: Differential Cascade Voltage Switch (DCVS) logic is a CMOS circuit technique that has potential advantages over conventional NAND/NOR logic in terms of circuit delay, layout density, power and logic flexibility. A detailed comparison of DCVS logic and conventional logic is carried out by simulation using SPICE of the performance of full adders designed using the different circuit techniques. The parameters compared are: input gate capacitance, number of transistors required, propagation delay time and average power dissipation. In the static case, DCVS appears to be superior to full CMOS in regards to input capacitance and device count but inferior in regards to power dissipation. The speeds of the two technologies are similar. In the dynamic case, DCVS can be faster than more conventional CMOS dynamic logic but only at the expense of increased device count and power dissipation.

Generation of propagate and generate signals: This gate generates the generate and propagate signals and it is shown in Fig. 4. This implementation uses the recurrence of the logic to reduce the device count.

CLA gate in multi output DCVS logic: A four stage Carry Look-Ahead (CLA) CMOS adder based on transistor sharing in a Multi-Output Differential Cascode Voltage Switch (MODCVS) logic is designed using cadence software with 180 mm technology as shown in Fig. 5. This proposed figure utilizes less power when compared to Manchester carry chain adders. The AND gate which

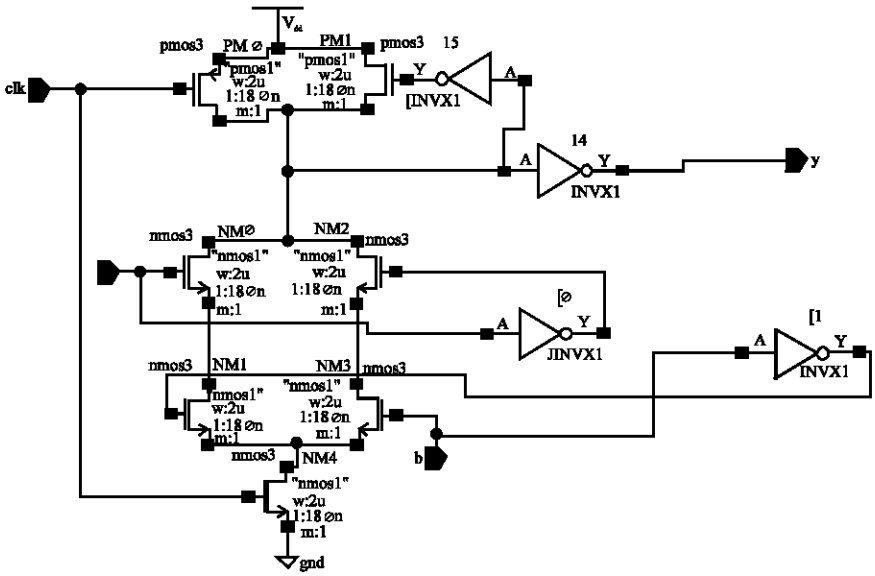

Fig. 2: Domino implementation for XOR propagate

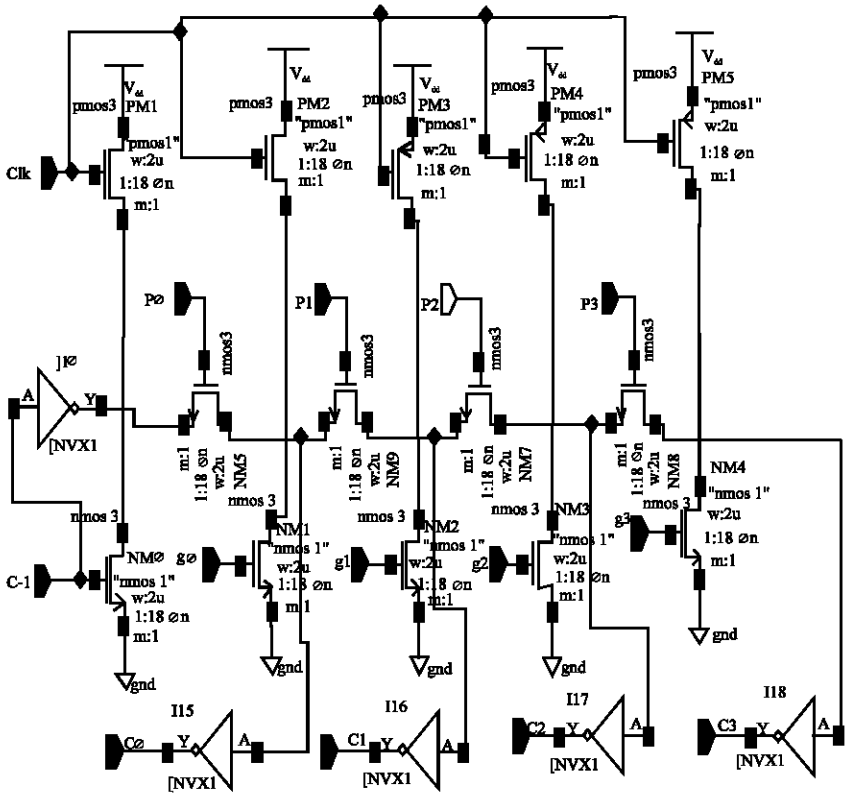

Fig. 3: Four bit MCC

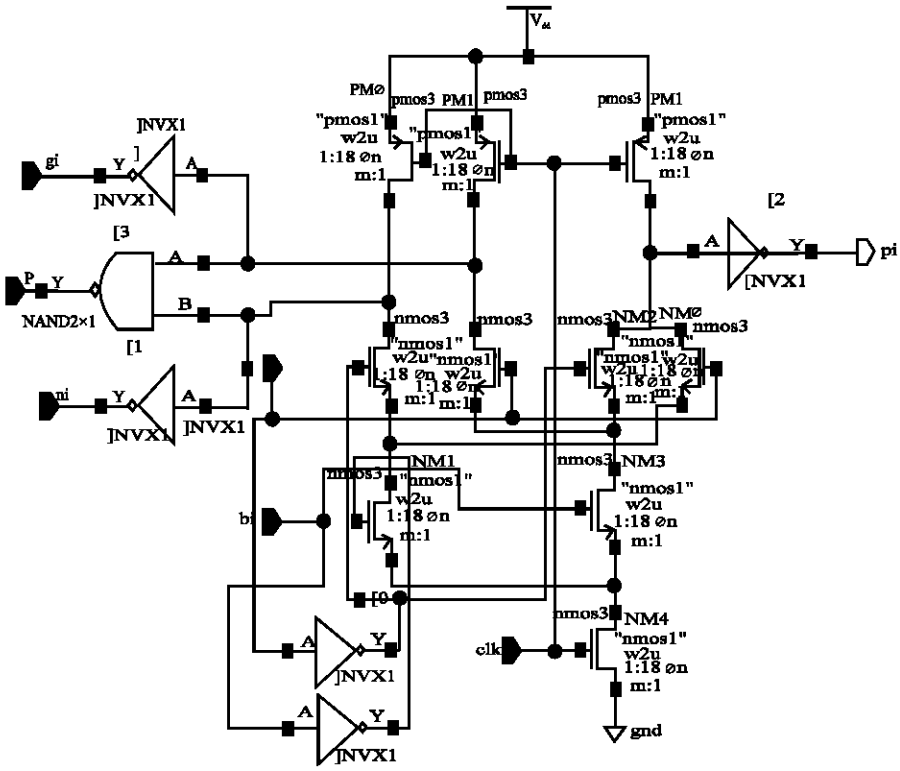

Fig. 4: Generation of generate and propagate signals

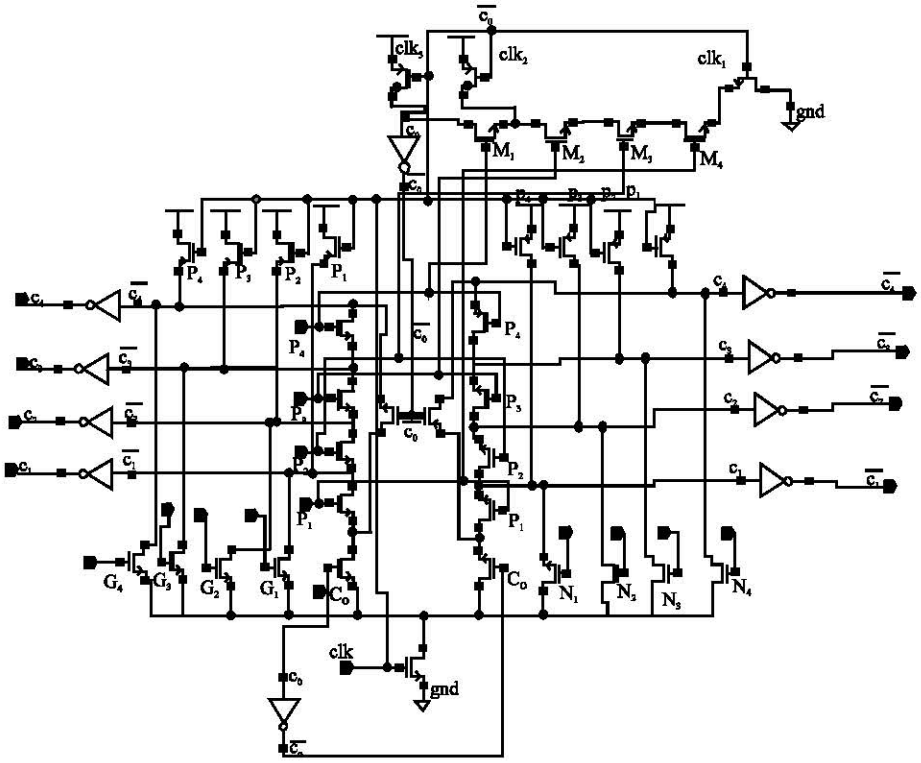

Fig. 5: CLA gate in multi output DCVS logic

used in pull up network reduces the propagative time in the entire circuit. The true and complementary carry signals are generated by using group propagate and generate signals.

A 4 bit Carry Look-Ahead (CLA) CMOS adde based on transistor sharing in a Multi-OutputDdifferential Cascode Voltage Switch (MODCVS) logic is presented. This adder uses a new enhanced CLA unit which enables the generation of all output carries in one single compact gate structure. Simulation results show that the proposed 4 bit adder has 14.7% less transistors and a 29.6% reduction in average power consumption compared to a standard DCVS implementation. The 4 bit adder has been designed to demonstrate the functionality and the features of such new logic structure. Multiple output logic gates have been proposed for recurrent logic such as circuits based on the Carry Look-Ahead (CLA) adder principle. In this logic style, single logic gates produce multiple functions and the device count reduction of a factor of 2 or more can be achieved depending on the degree of recurrence in the circuit.

RESULTS AND DISCUSSION

Bit Manchester carry chain circuit: Figure 6 shows the conventional circuit consists of 4 bit two inputs namely P(0, 1, 2, 3) and G(0, 1, 2, 3). The operation of the circuit is controlled by clock signal. The input values are from P_i

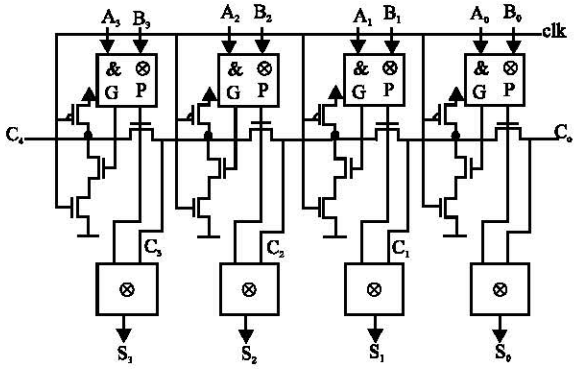

Fig. 6: Simulated circuit diagram of conventional 4 bit MCC

and G_i values of the domino propagate and generate output values. If clock equals to 0, the circuit will enter into pre-charge state and no output will be obtained. If clock value is 1, then the output will depend on the input values. The inputs of propagate and generate signals from P_i and G_i will possesses and the corresponding output carry signals namely C(0, 1, 2, 3).

Figure 7 shows the implementation of 4 bit conventional Manchester Carry Chain (MCC) using transistor level logic. It is a chain of pass transistors that are used to implement the carry chain. It was designed

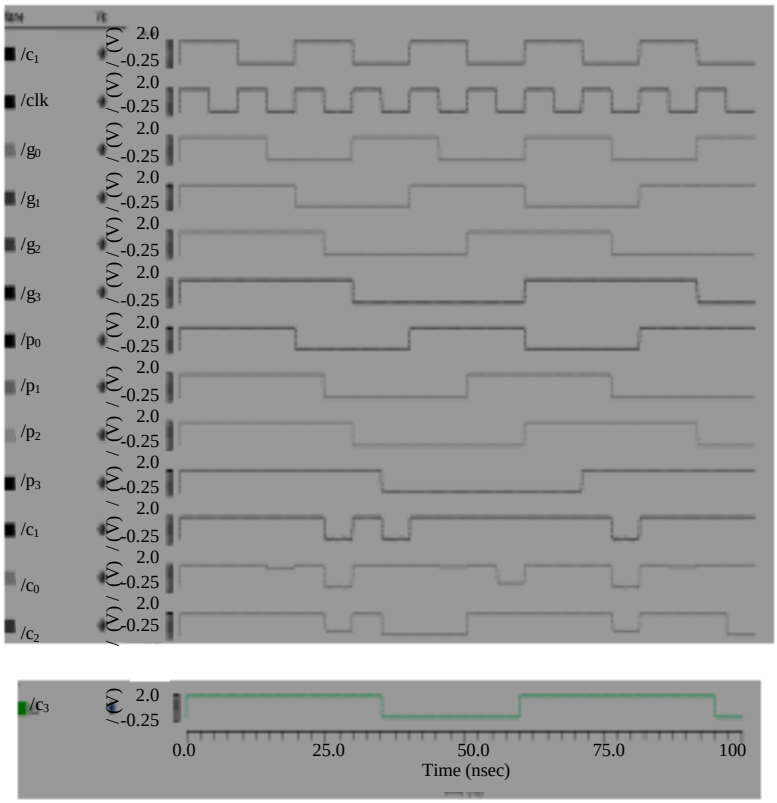

Fig. 7: Waveforms of conventional 4 bit MCC

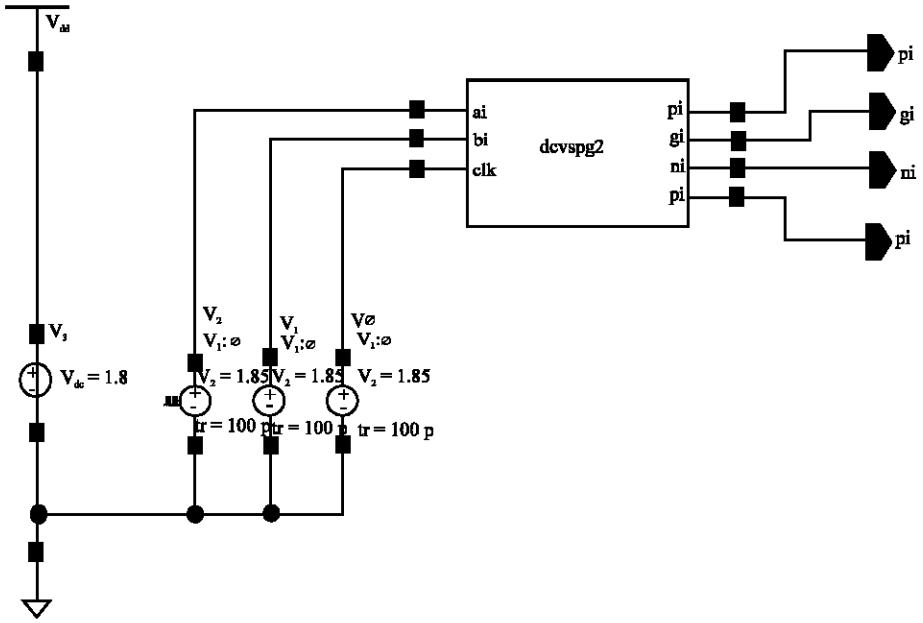

Fig. 8: Schematic of 4 bit DCVS generate and propagate signals

using dynamic logic. The Manchester carry chain is working based on carry kill signal, carry generate and carry propagate signals.

Bit DCVS propagate and genarate signals: Figure 8 shows the schematic of DCVS which propagate and generate signals of 4 bits. The differential cascade voltage

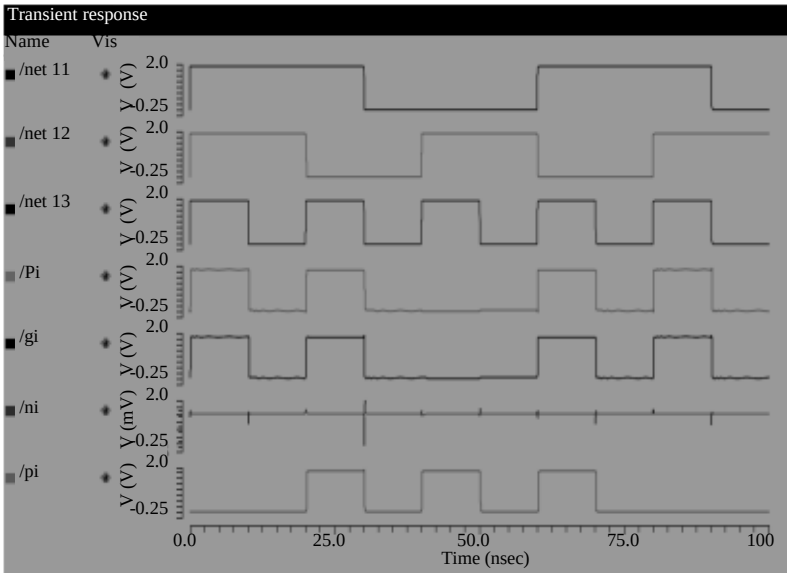

Fig. 9: Waveforms of 4 bit DCVS generate and propagate signals

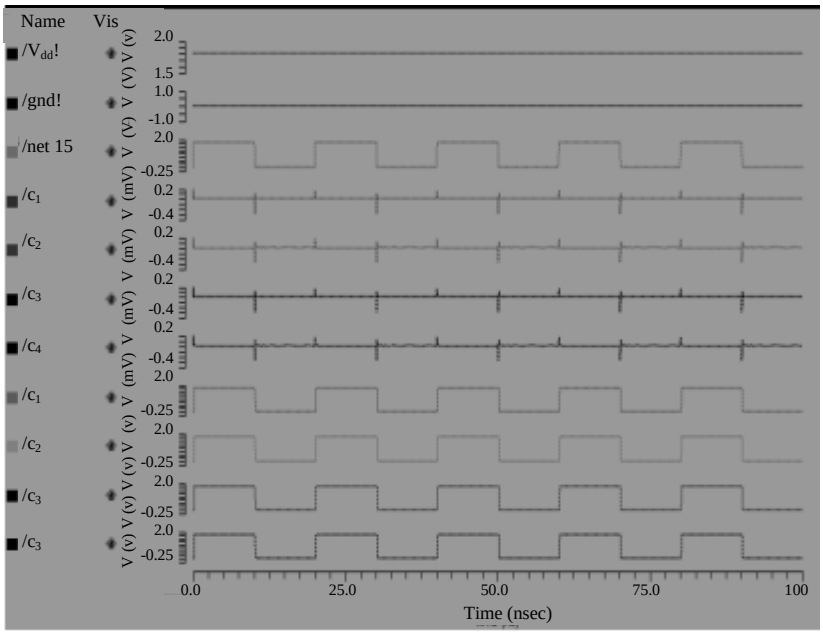

Fig. 10: Waveforms of 4 bit CLA gate in multi output DCVS logic

switch logic consists of true and complementary outputs. In self-timed circuits, the completion signals involved in the asynchronous local communication can be generated in a general way with dynamic Differential Cascode Voltage Switch (DCVS) logic.

Waveforms: Figure 9 shows the waveforms obtained for 4 bit DCVS propagate and generate using transistor level logic. The both input are high then generate output is high otherwise it is zero.

Bit CLA gate in multi output DCVS logic: Figure 10 shows the waveforms obtained 4 bit high speed adder using transistor level logic. The basic idea of multi output domino logic is sharing n FET logic in evaluate phase.

Power and delay comparision tables: The simulation results were carried out by using cadence virtuoso software. The proposed logic styles are analyzed in terms of power, delay and power delay product. The circuits are tested with different supply voltages, process corners

Table 1: Average delay, power and PD poduct of 4 bit Mnchester carry chain in CLA

Voltage (V)	Average delay (sec)	Average power (W)	Average PD product (J)
0.8	192.525-12	57.0E-6	10.97*E-15
1.2	81.85E-12	360.4E-6	29.498*E-15
1.4	66.05E-12	628.6E-6	41.519*E-15
1.6	55.607E-12	982.0E-6	54.60*E-15
1.8	48.11E-12	1417E-6	68.17*E-15

Table 2: Average delay, power and PD product of 4 bit DCVS logic in CLA

Voltage (V)	Average delay (sec)	Average power (W)	Average PD Product (J)
0.8	109E-12	2.772E-6	3.038*E-15
1.2	371.755E-12	6.494E-6	2.414*E-15
1.4	292.7E-12	9.00E-6	2.634*E-15
1.6	251.975E-12	12.11E-6	3.0514*E-15
1.8	49.59E-12	1089E-6	54.00*E-15

and room temperature. The performance of DCVS and multi output domino logic were reported in Table 1 and 2.

CONCLUSION

The main focus is to investigate the tradeoff between DCVS and multi output domino logic in CLA. The DCVS logic is 49.89% improvement in power consumption than multi output domino logic. The multi output domino logic is gives 56% high speed than the DCVS logic. The proposed adder results less delay and more power compared to the DCVS logic. The simulation was carried out using standard Cadence Virtuoso tool with 180 nm technology. The simulation result of this adder improves the speed compared to standard adder module.

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