

Design and Implementation of Area Efficient Reversible Full Adder-Subtractor in QCA

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Abstract: In the near future, the part of energy dissipation due to information loss in irreversible computation will become a serious issue in VLSI chips. A Quantum-dot Cellular Automata (QCA) is an emerging nanotechnology which facilitates reversible computing. It's a new computing paradigm with applications in extremely low energy dissipation. In this study reversible full adder-subtractor is proposed. For evaluating the functionality and energy dissipation QCA Designer and QCAPro tools are used. Proposed design is implemented in multi-layer in QCA designertool. It improves 78% of cell count compared to the existing QCA-based reversible full adder-subtractor. QCAPro tool demonstrates the efficiency of leakage and switching energy improvements.

Key words: Quantum-dot cellular automata, reversible computing, full adder-subtractor, single layer circuit, multi-layer circuit, reversible

INTRODUCTION

Nanotechnology provides new possibilities for computing due to the unique properties that arise at such reduced feature sizes. Among these new devices, Quantum-dot Cellular Automata (QCA) (Lent *et al.*, 1994; Smith, 1999) operates new physical phenomena and innovative techniques that depart from a CMOS-based model. QCA gives a solution at nano-scale and it also offers a new method of computation and information (Amlani *et al.*, 1998; Orlov *et al.*, 1997).

In modern VLSI system, the power consumption is the main concern. The disproportionate scaling of the size of transistors and power supply voltage has led to high leakage currents and high power density creating hot spots in CMOS chips. For this reason, different computational paradigms by using nanotechnologies, addressing small size and low power dissipation should be considered. Reversible computing is a computational paradigms which is a one-to-one mapping between the input and output states of the circuit (Ma *et al.*, 2008; Sen *et al.*, 2014).

The first 1 bit full adder in QCA was proposed by Tougaw and Lent (1994). This design is constructed using five-three input majority gates and three inverters. However, a simpler QCA full adder was presented (Wei *et al.*, 2003). This full adder is composed of three-three input majority gates and two inverters. Different layouts for a QCA full adder have been

presented using this design (Zhang *et al.*, 2004). Then, anovel QCA full adder design was introduced (Azghadi *et al.*, 2007). This design is composed of one three input majority gates, one inverter and a new kind of majority gate, a five input voter are used only for its advantages in wire crossing (Hashemi *et al.*, 2012; Cho and Swartzlander, 2007; Pudi and Sridharan, 2012). A new five-input majority gate (5 MV) is proposed and a new full adder based on that 5 MV is synthesized (Hashemi *et al.*, 2012). After that adder, subtractor is designed (Sangsefidi *et al.*, 2015) which is 8 bit. A multilayer 1-bit Full-Adder (FA) is designed (Bahar *et al.*, 2014). This design presents a single layer five-input Majority Voter gate (MV5) and power dissipation are estimated.

For the design of many computation systems and functional circuits adder and subtractor are used. Different kinds of half/full adder designs with different number of majority gates are presented (Kim *et al.*, 2007; Ahmad *et al.*, 2014a-c; Safavi and Mosleh, 2013; Santra and Roy, 2014) and the full adder design proposed has better performance.

A small number of QCA based binary subtractors have been proposed. Full adder and full subtractor designed (Ahmad *et al.*, 2014a-c) present less area, circuit complexity and clock delays. Fredkin (Bahar *et al.*, 2015) and Feynman (Bahar *et al.*, 2014) gates based different binary subtractors have been proposed (Thapliyal *et al.*, 2005). For employing half subtractor, the design proposed

(Lakshmi *et al.*, 2010; Srivastava *et al.*, 2011) has required 77 and 55 cells. Reshi has proposed a half and full subtractors that require 45 and 104 cells, respectively for implementation (Srivastava *et al.*, 2011). Most recently, 2-input XOR gate based half and full subtractors (Bahar *et al.*, 2017) have been proposed which required 19 and 32 cells, respectively.

Reversible Quantum Gate (RQG) is proposed (Moaiyeri *et al.*, 2016). This design is proposed reversible full adder subtractor using RQG gate in single layer. This design improves the cell count and area.

In this study, reversible full adder-subtractor is proposed which is implemented in multi-layer using RQG gate. It has significantly lower number of cells and smaller area even in comparison with its single layer and multilayer counterparts.

Overview of QCA: One of the most attractive and promising nanotechnologies is Quantum-dot Cellular Automata (QCA). It operates based on Coulombic interactions (Ma *et al.*, 2008; Roohi *et al.*, 2015). In QCA, two electrons inside the cell determine the '0' and '1' logics as shown in Fig. 1a. The electrons moves quantum-mechanically tunnel between the dots through tunneling junctions and fix either with cell polarization in $P = 1$ (logic 1) or $P = -1$ (logic 0) as illustrated in Fig. 1a.

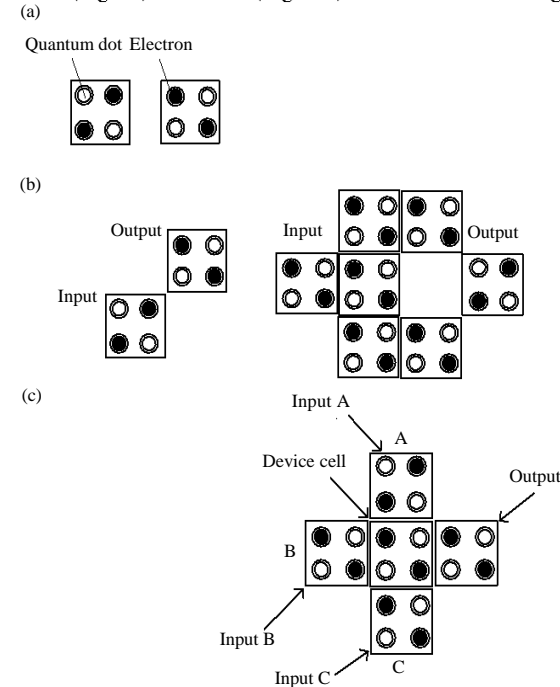


Fig. 1: QCA logic; a) QCA cells; b) QCA inverter and c) QCA three-input majority gate

During the state transition and propagation, there is no energy dissipation in QCA. So, QCA dissipates extremely lower power compared to the CMOS technology. The energy dissipated per switching event in a reversible QCA circuit can be significantly less than $kBT \ln 2$ due to clocked information-preserving system. Implementing efficient reversible logic gates become possible using QCA (Timler and Lent, 2002).

Figure 1b and c show the fundamental QCA gates, the inverter and the Majority (MAJ) gates. The QCA inverter is usually realized in two different configurations reverses the cell polarization and the output of the majority gate will be the majority of the inputs.

MATERIALS AND METHODS

Proposed designs: Reversible Quantum Gate (RQG) is proposed in this study. RQG gate a 3×3 reversible logic gate. According to Eq. 1-3, this gate has three inputs A, B and C and generates three outputs P, Q and R. In Table 1, truth table shows that the RQG gate is fully reversible with a completely one-to-one mapping between the inputs and outputs. Figure 2 is shown the proposed reversible gate:

$$P = \text{MAJ}(A, B, C) = A \cdot B + B \cdot C + A \cdot C \quad (1)$$

$$Q = \text{MAJ}(A', B, C) = A \cdot B + B \cdot C + A' \cdot C \quad (2)$$

$$R = A \oplus C = A \cdot C' + A' \cdot C \quad (3)$$

To implement and verify all of the designs in this study, the QCA designer tool has been used. In Fig. 3, RQG is shown the QCA layout of the proposed reversible gate. The RQG gate is composed of two three-input majority gates and one 2-input exclusive OR (XOR) gate. Figure 4 shows the simulation result of RQG. It shows the correctness of truth table.

Proposed reversible full adder-subtractor: The RQG gate can be used to implement important logic circuits such as

Table 1: Truth table of proposed gate

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	1	1
0	1	0	0	1	0
0	1	1	1	1	1
1	0	0	0	0	1
1	0	1	1	0	0
1	1	0	1	0	1
1	1	1	1	1	0

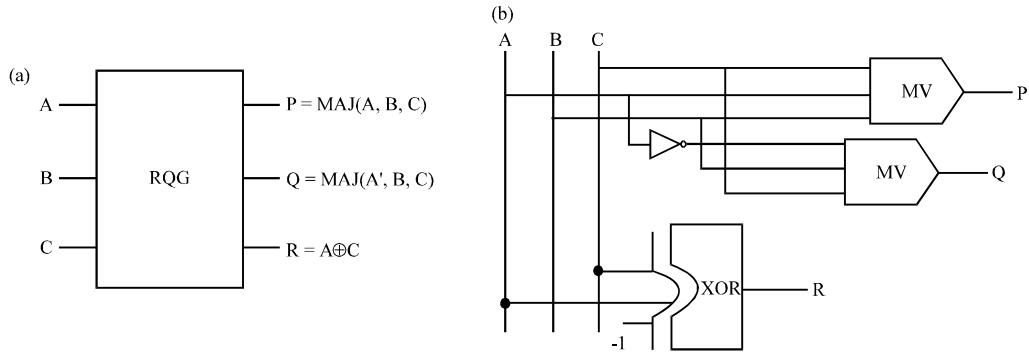


Fig. 2: The proposed reversible gate; a) Block diagram and b) Schematic diagram

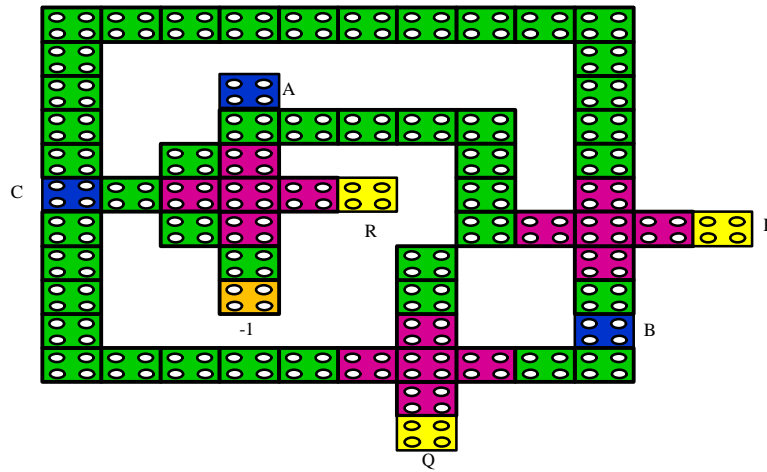


Fig. 3: Layout of the proposed Reversible Quantum Gate (RQG)

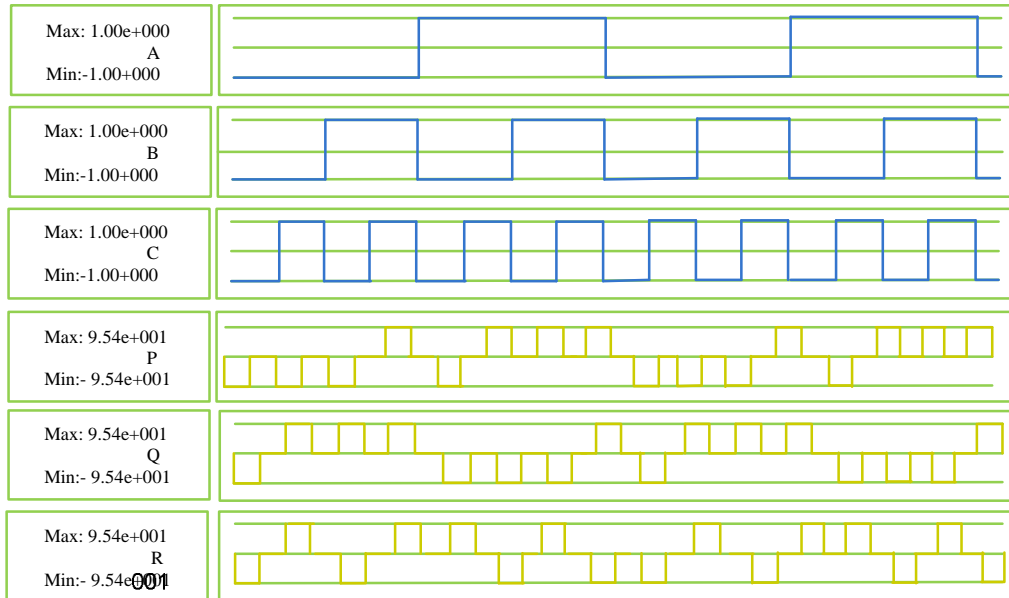


Fig. 4: Simulation result of RQG

full adder and full subtractor. By using an RQG and two Feynman (FG) reversible gates, an efficient reversible full adder-subtractor circuit with four inputs and four outputs is proposed which is shown in Fig. 5. A Feynman gate with x and y inputs, provides x and \oplus outputs (Ma *et al.*, 2008). In the proposed design, the first FG replicates the B input and the second one is used to create a three input XOR ($A \oplus B \oplus C$). The three main outputs of the circuit provides the full adder-subtractor as given in Eq. 4-6 where Sum and Diff are the sum and difference of the three inputs and Cout and Bout are the output carry and borrow, respectively. Furthermore, the fourth output ($A \oplus C$) is a garbage output.

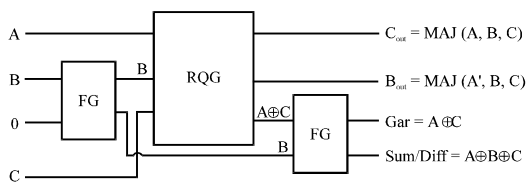


Fig. 5: Proposed reversible full adder-subtractor

The layout of the proposed full adder-subtractor is designed using three layers of QCA cells. Figure 6 shows the QCA implementation of full adder-subtractor. It shows three different layers that indicate the main layer, layer-1 and layer-2. The layout of proposed multi-layer full adder-subtractor shows in Fig. 6d in Top view. This design enhances the robustness and manufacturability of the proposed design. Table 2 presents truth table of the proposed design.

Simulation results and comparisons: A popular simulation tool named QCADesigner is used for simulation and verification of the designs. The simulation

Table 2: Truth table of the proposed reversible full adder-subtractor

A	B	0	C	Cout	Bout	Sum/Diff	Gar
0	0	0	0	0	0	0	0
0	0	0	1	0	1	1	1
0	1	0	0	0	1	1	0
0	1	0	1	1	1	0	1
1	0	0	0	0	0	1	1
1	0	0	1	1	0	0	0
1	1	0	0	1	0	0	1
1	1	0	1	1	1	1	0

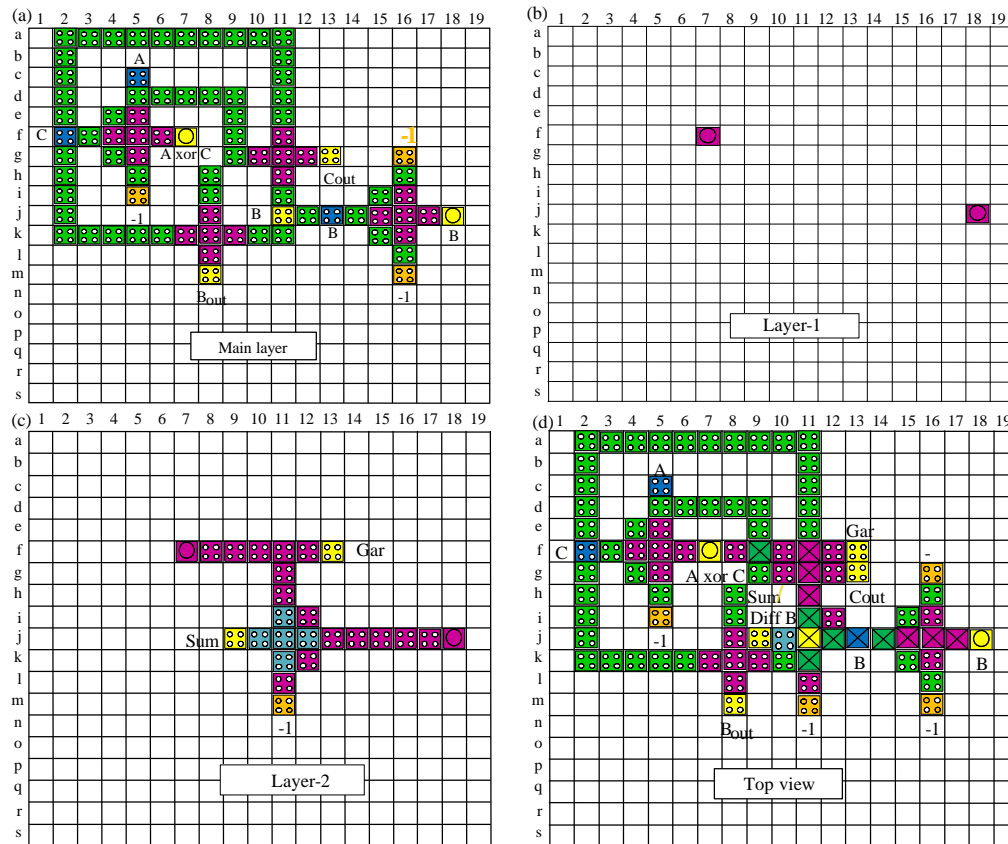


Fig. 6: QCA implementation of the proposed full adder-subtractor; a) Main layer; b) Layer-1; c) Layer-2 and d) Top view

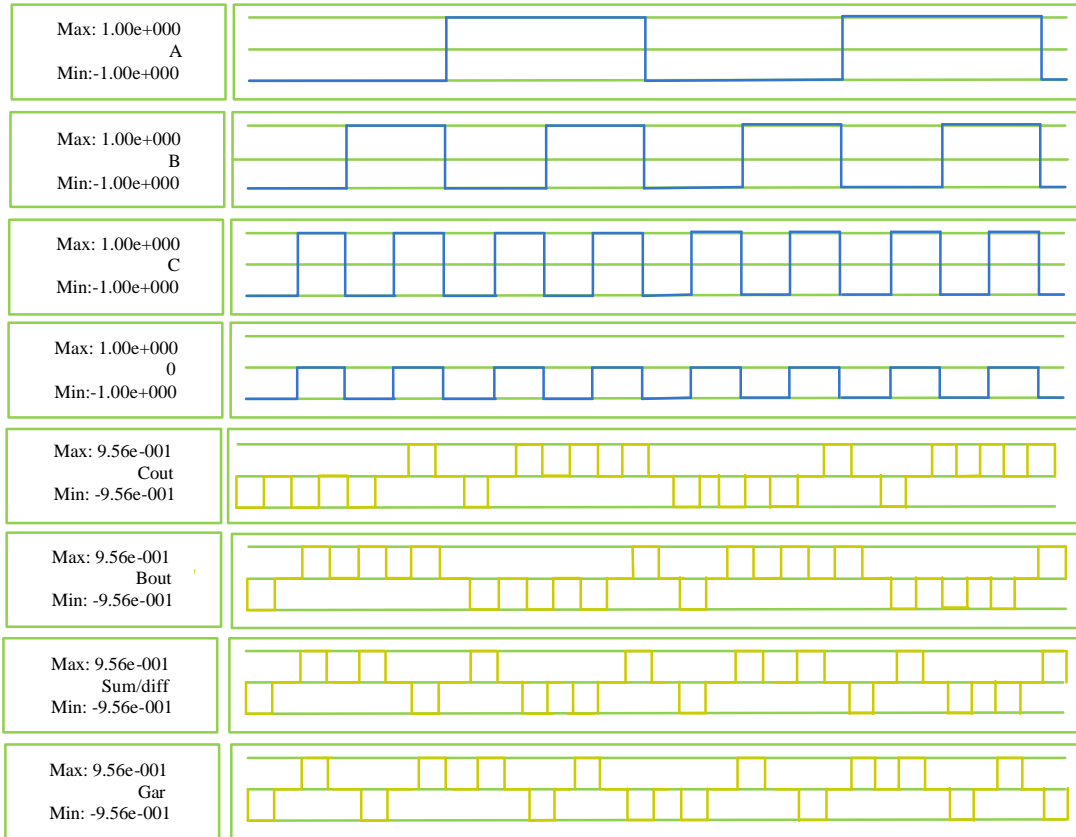


Fig. 7: Simulation results of the proposed full adder-subtractor

Table 3: Comparison of reversible QCA full adders

Categories	Cells	Layers	Area (μm^2)	Latency (clock cycles)	Garbage outputs
QCA (Lent <i>et al.</i> , 1994)	343	1	0.46	1.50	3
QCA2 (Lent <i>et al.</i> , 1994)	356	1	0.47	1.50	3
FG+RQCA (Smith, 1999)	517	1	0.78	3.25	2
Proposed	113	3	0.10	1.25	1

results shown in Fig. 7 claim the functionality of the proposed multi-layer reversible full adder-subtractor which utilizes the RQG gate as its main block.

Table 3 shows a comparison between our proposed full adder-subtractor design and existing reversible designs. The proposed reversible full adder-subtractor produces only one garbage output which is fewer than the other designs. Using different clock zones for wire crossing makes the latency (number of clock cycles) of the proposed design slightly shorter than others. Our proposed design is multi-layer without any rotated cells which significantly enhance its robustness and manufacturability and it performs both addition and subtraction operations. It has considerably lower number of cells and much smaller area in comparison with both single-layer and multilayer designs.

Energy analysis: To evaluate consumed power of the proposed design, we use QCAPro (Saket *et al.*, 2011) tool. QCAPro is an acceptable power valuator tool that estimate energy dissipation of proposed circuits. In three different tunneling energy levels $0.5 E_k$, $1 E_k$, $1.5 E_k$ at 2 K temperature, the energy dissipation is analyzed. Energy dissipation analysis of proposed multi-layer reversible full adder-subtractor at three different tunneling energy levels is shown in Table 4. This table shows leakage energy dissipation, switching energy dissipation and total energy dissipation. The graphical presentation of energy dissipation of proposed full adder-subtractor is shown in Fig. 8.

The power dissipation maps of presented reversible full adder-subtractor are shown in Fig. 9. In this figure, it is clear that high power dissipating cells are indicated with darker colors.

Reliability analysis: Reliability analysis is the temperature effect on Average Output Polarization (AOP) of proposed gates has been analyzed by QCA designer and the maximum and the minimum polarizations for each output cell are observed. The output polarization of cell is taken

Table 4: Energy dissipation analysis of proposed full adder-subtractor

Circuit	Leakage energy dissipation (meV)			Switching energy dissipation (meV)			Total energy dissipation (meV)		
	0.5 Ek	1 Ek	1.5 Ek	0.5 Ek	1 Ek	1.5 Ek	0.5 Ek	1 Ek	1.5 Ek
Multilayer full adder-subtractor	55.67	137.9	239.18	94.75	83.16	72.86	150.42	221.06	312.04

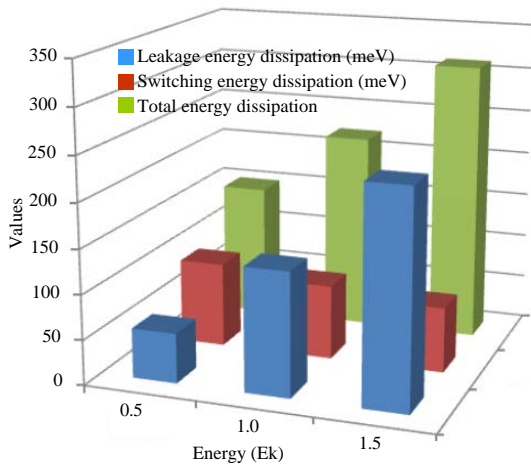


Fig. 8: Energy dissipation of proposed full adder-subtractor

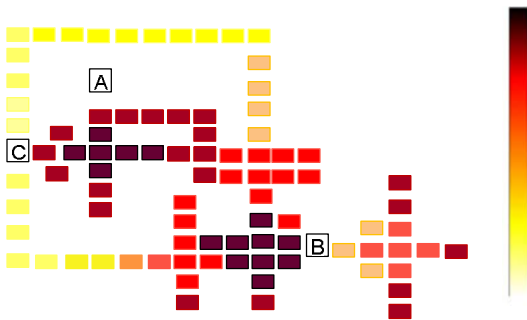


Fig. 9: Power map of proposed reversible full adder-subtractor

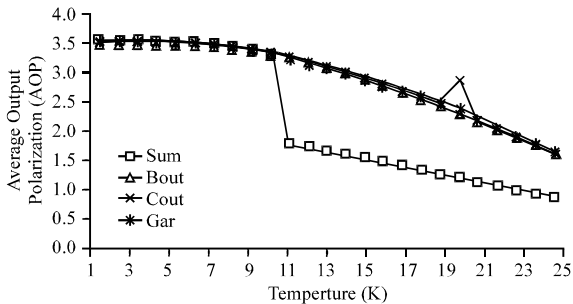


Fig. 10: Effect of temperature on average output polarization of proposed QCA circuit

at different temperature. The AOPs for different output cells of proposed layout at different temperatures are calculated and plotted in Fig. 10. The AOP of the

output cells Sum/Diff and Gar of the reversible full adder-subtractor is gradually decreased, up to a temperature of $T = 7$ K as shown in Fig. 10. Thus, in between temperatures 1 and 7 K, sum/diff and gar works efficiently. Above the temperature $T = 7$ K, the AOP falls down radically and produces inconsistent outputs. The output Bout and Cout remain constant. When the temperature is above 32 K, the AOP is dropped drastically which results incorrect outputs.

CONCLUSION

This study presents an efficient QCA-based multi-layer reversible full adder-subtractor for reversible nanocomputing which provides with both addition and subtraction operations. It has multi-layer structure in terms of cell count area, it outperforms the previous reversible full adder. It improves 78% cell count and 87% area compared to others. The leakage and switching energydissipations in these designs are calculated by using QCAPro tool. In addition, it does not require rotated cells and has a lower number of garbage outputs requiring less power dissipation.

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