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A Study on the Distinction Circuit of Logic Input-Level for Digital Logic Lab-Unit

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Abstract: Digital logic lab-unit plays an important role in electrical engineering education. However, conventional logic level circuit in logic lab is too easy to break down such as surge voltage, wire disconnection and ESD (Electro Static Discharge). In this study, disadvantages of conventional logic level display circuit in logic lab-unit were investigated and an improved logic level display circuit is proposed by both simple hardware circuit and software components with microprocessor. Hardware is constructed with a voltage pre-scaler and a limiter, its output supplied to analog-digital Converter of the microprocessor. In order to verify the performance of the proposed method, experimental circuits were set and the operating conditions were tested. It operates normally from minus input voltage to over voltage. In addition, the logic state is displayed in four stages of open load, logical-low, logical-high and over voltage. The hysteresis characteristics are realized to overcome instability of transition and verified it through experiments. The proposed method can protect against the voltage exceeding the allowable input voltage and it can also detect the input state. Especially, disconnection of wire can be detected by proposed logic level display circuit, so that, trials and errors are reduced.

Key words: Lab-unit, digital, logic, level, logic-lab, A/DC

INTRODUCTION

The digital logic lab-unit is one of the fundamental equipment of the electronics experiments like Oscilloscope, function generator and DC power-supply. The digital logic lab-unit (short for logic lab-unit) consists of circuits that apply an input signal to an experimental target, circuits that distinguish the output state, a simple power supply and a bread-board (De Micheli, 1994; Hoffman, 2004; Morris and Michael, 2006; Nelson, 1995). Although, the logic lab-unit is a convenient device for digital experiments, it can cause unexpected situations during the experiment. For this reason, experimental device should be designed to protect equipment against unexpected situations. The conventional logic level display circuit used in the logic lab-unit is shown in Fig. 1. The input signal passes through the pull-down resistor R_1 and selects positive logic and negative logic by U_2. Then, it is connected to the LED via. U_1 buffer. The output of U_2 is decoded in U_3 along with the output of the other channels and displayed in hexadecimal by the 7-segment LED. A conventional logic level display circuit consists of a +5 V circuit. Therefore, if +12 V or (-) voltage is input, U_1 of the circuit will be damaged instantly and U_2 and U_3 will be damaged as well. Also, not only the +5 V logic is used in the experiment but also the

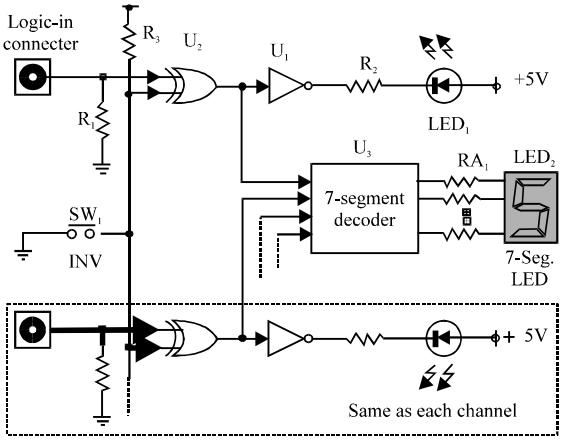

Fig. 1: Conventional schematic circuit design of the logic level display

voltage of +15 V (CMOS logic) can be used, so that, the conventional display circuit cannot be used (Ono *et al*., 2008; Miyata and Kashiwagi, 1993).

Most of the equipment in the training field is simply and often broken down especially by trainees because they do not know if this device is only available for +5 V logic. Another problem of this circuit is that open load and logical-low cannot be distinguished. Even though,

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the wires are connected with the naked eye, it is difficult to find the disconnected point because inside of the wire is invisible (Brandt, 1974; McCluskey and Clegg, 1971; Zhao *et al*., 2008). Moreover, all components consist of discrete devices such as hexa-decimal type 7-segment decoder and mechanical toggle switch; cost is increased by them. In this study, a proposed method improves the problem of the conventional logic level display circuit in logic lab-unit.

MATERIALS AND METHODS

Proposed logic level display circuit

Circuit design of logic level display: In Fig. 2, the proposed output port is that indicate open load (NC: No Connection), logical-low, logical-high and above +5 V (HV: High Voltage). Notice that the following state of display circuit from Fig. 2:

- When open load is detected, the blue LED (B) is on
- When logical-low is detected, the green LED (G) is on
- When logical-high is detected, the red LED (R) is on
- When high voltage is detected, the yellow LED (Y) is on

The pre-scaling circuit is performed using the circuit of Fig. 3a, so that, there is no limitation on the voltage range of the logic signal process. Then, it is connected to the analog-to-digital converter of microprocessor and processed by software. The open load can be detected by voltage divider R1 and R_2, called pre-scaling circuit as shown in Fig. 3a. When the input is logical-low or logical-high, the corresponding voltage is output as shown in Fig. 3b and c, respectively. If the input is above + 5 V, V_o is unconditionally limited to maximum +5 V by Zener diode DZ_1. Figure 3b shows the equivalent circuit that logical-low is input and output voltage can be expressed by:

$$V_{o,\,LO} = \frac{R_2 \,||\, R_3}{R_2 \,||\, R_3 + R_1}.5 \tag{1}$$

Similarly, Fig. 3c shows the equivalent circuit that logical-high is input and output voltage can be obtained by:

$$V_{o,5V} = \frac{R_2 \,||\, R_3}{R_2 \,||\, R_3 + R_1}.5 \tag{2}$$

The output voltage of open load can be expressed as:

$$V_{o,\,NC} = \frac{R_2 \,||\, R_3}{R_2 \,||\, R_3 + R_1}.5 \tag{3}$$

The desired output voltage is that the intervals of the voltages are distributed widely and uniformly in order to

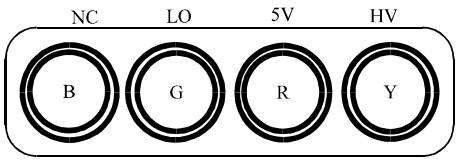

Fig. 2: Output port of proposed logic level display

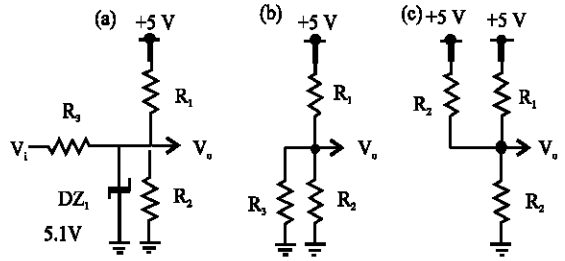

Fig. 3: Pre-scaling circuit of the logic level display: a) Circuit; b) 0 V input and c) +5 V input

Table 1: Desired voltage distribution according to the output state

Input-V_i	Fixed V_o (V)	Aimed V_o (V)
H V	5	5.00
+5 V	-	3.75
NC	2.5	2.50
0 V	-	1.25

distinguish these voltage from the microprocessor as shown in Table 1. Substituting the condition of open load into Eq. 3 yields:

$$2.5 = \frac{R_2}{R_1 + R_2}.5 \tag{4}$$
$$\therefore R_1 = R_2$$

Substituting the condition of logical-high into Eq. 2 yields:

$$3.75 = \frac{R_2}{R_2 + R_2 \,||\, R_3}.5 \tag{5}$$

Substituting the condition of logical-low into Eq. 5 yields:

$$V_{o,LO} = \frac{2.R_2 \,||\, R_3}{2.R_2 \,||\, R_3 + 2.R_3}.5 = \frac{\frac{2}{3}R_3}{\frac{2}{3}R_3 + 2.R_3} \tag{6}$$

As a result, when R_1 and R_2 are the same and R_3 is two times of R_1, they are the most even distribution. In Table 2, the measurement of the voltage is converted by 8 bit A/D converter which is ranged from 0- 255. In Fig. 4, detected voltage is distributed uniformly. Figure 5 shows a schematic circuit design of 8-channel for realizing the proposed logic level display circuit in logic lab-unit.

Software design of logic level display: The threshold to determine each state is the midpoint of each state

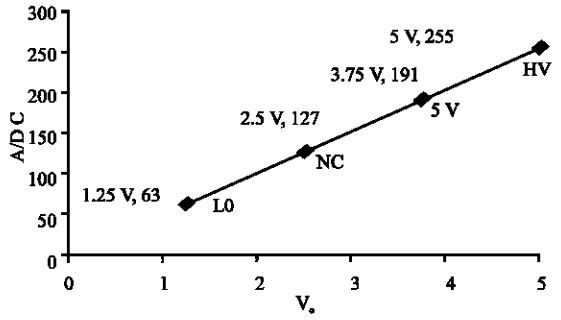

Fig. 4: Detected voltage distribution according to the output state

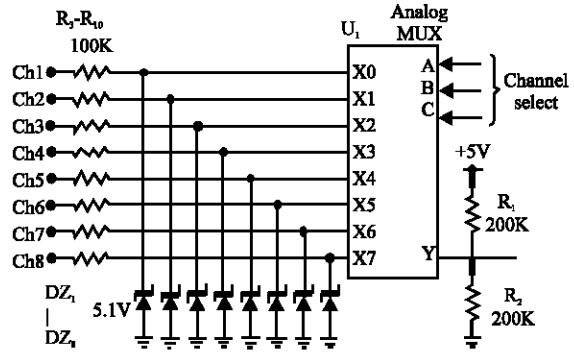

Fig. 5: Schematic circuit design of 8-channel for realizing the proposed logic level

Table 2: To be converted value according to each input

Input-V_i	V_o (V)	8-bit A/D C
HV	5.00	255 (0xFF)
+5V	3.75	191 (0xBF)
NC	2.50	127 (0x7F)
0V	1.25	63 (0x3F)

value as shown in Fig. 6. For example to distinguish between LO and NC-states, a midpoint between the LO-state 63 and the NC-state 127 is thresholds which are 95 as shown in Fig. 6.

However, when the conversion value is slightly oscillated around threshold, the fixed threshold is ambiguous to determine the state. Therefore, the hysteresis characteristics are needed to solve the instability. The state flow of the hysteresis characteristics is shown in Fig. 7.

If the state changes from LO-state to NC-state, the conversion value should exceed V1H. On the other hand in order to change from NC-state to LO-state, the conversion value should be lower than V1L. Namely, the value changing from the LO-state to the NC-state (V1H) and the value changing from the NC-state to the LO-state (V1L) are set differently, so that, the instability of threshold can be solved.

Figure 8 is a flowchart for controlling a proposed circuit of several channels. Figure 8a shows flow chart

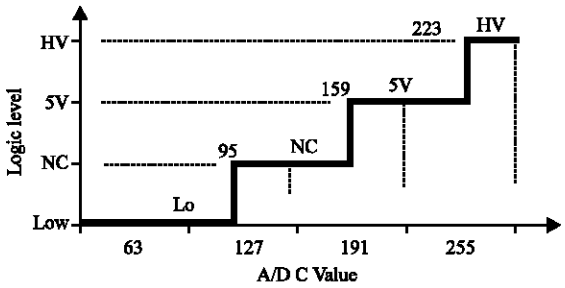

Fig. 6: Threshold of input state in the logic level display

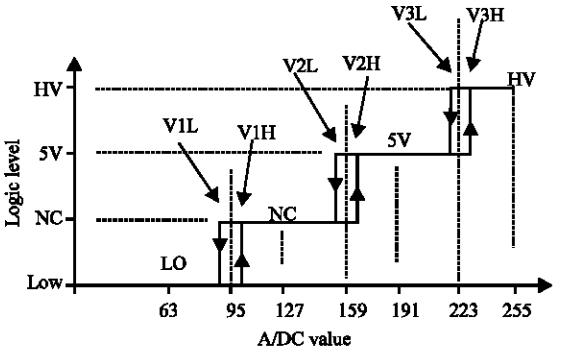

Fig. 7: Hysteresis characteristics of the logic level display

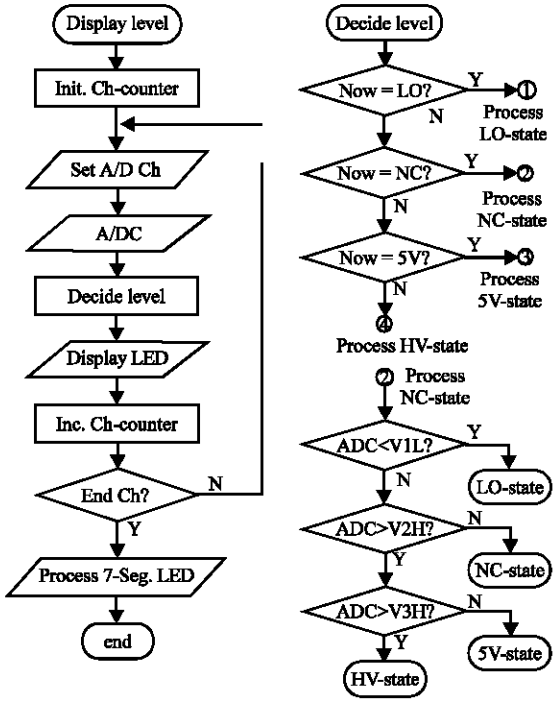

Fig. 8: Flowcharts for the logic level display: a) Main control; b) Branch to each state and c) Process NC-state

of main control, Fig. 8b shows flow chart of state determination and Fig. 8c is flow chart of NC-state processing.

RESULTS AND DISCUSSION

Experiments and considerations

Pre-scaling circuit experiments: The proposed pre-scaling circuit for logic level display was verified by experimental results with the logic lab-unit. The proposed circuit was installed to the logic lab-unit as shown in Fig. 9. Output voltage V_1 was measured according to the input voltage V_i as shown in Table 3 and Fig. 10.

The ideal performance of the proposed pre-scaling circuit is not realized due to the inherent characteristics of the Zener diode. In order to verify the dynamic characteristic of pre-scaling circuit, the output signal for triangular input signal was measured as shown in Fig. 11.

When the input voltage is -2 V and +3.74 V, the output is +0.25 V (Fig. 11 a) and +5 V (Fig. 11b), respectively. Also, from the above input voltage, the output waveform gradually decreases. Therefore, even if, the input voltage is below 0 V or above + 5 V, the output is limited to 0 V to +5 V, this circuit can prevent the device from being damaged by accident.

Software experiments: In order to verify the software that detects the state, the LED indicators for state detection are connected and output of the pre-scaling circuit is connected to the input of the microprocessor (Microchip, 2016). In Fig. 12, the microprocessor detects open load and the blue LED indicator is on.

Table 4 shows the results of LED indicators with various input voltages V_i. Also, the variation of each state is shown in Fig. 13 where LO = 0, NC = 1, 5 V = 2 and HV = 3. In this experiment, the hysteresis threshold was set to ±4.

The state of open load with triangular input waveform is measured that falling point and rising point are different as shown in Fig. 14.

In order to measure each state of the threshold, a circuit for output transition measurement was designed as shown in Fig. 15. When the triangular waveform is input to this circuit, the output is measured in the X-Y mode of the oscilloscope and the hysteresis can be observed as shown in Fig. 16. The output state has following results: 0 V as logical-low, $1/3 \cdot V_{CC}$ as open load, $2/3 \cdot V_{CC}$ as logical-high and V_{CC} as over voltage.

Table 3: Simulation and experimental results of the pre-scaling circuit

Input - V_i (V)	Simulated V_o (V)	Measured V_o (V)
-2	0.25	0.25
-1	0.75	0.75
0	1.25	1.25
+1	1.75	1.75
:	:	:
+4	3.25	3.25
+5	3.75	3.74
+6	4.25	4.12
+7	4.75	4.54
+8	5	4.68
+9	5	4.76
:	:	:
+15	5	4.94
NC	2.5	2.50

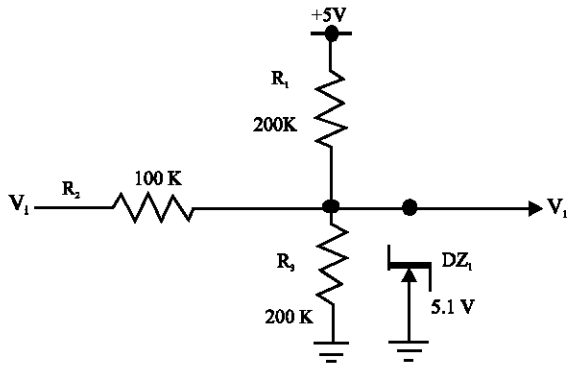

Fig. 9: Pre-scaling circuit for experiment

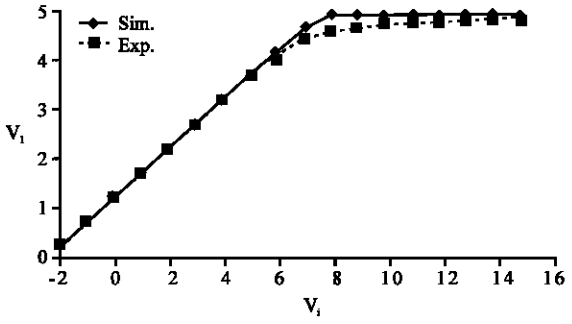

Fig. 10: Result graph of the pre-scaling circuit

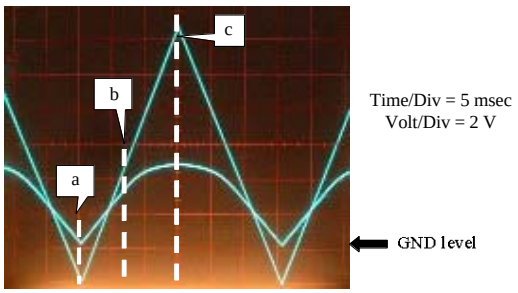

Fig. 11: Result of output signal with a triangular input signal

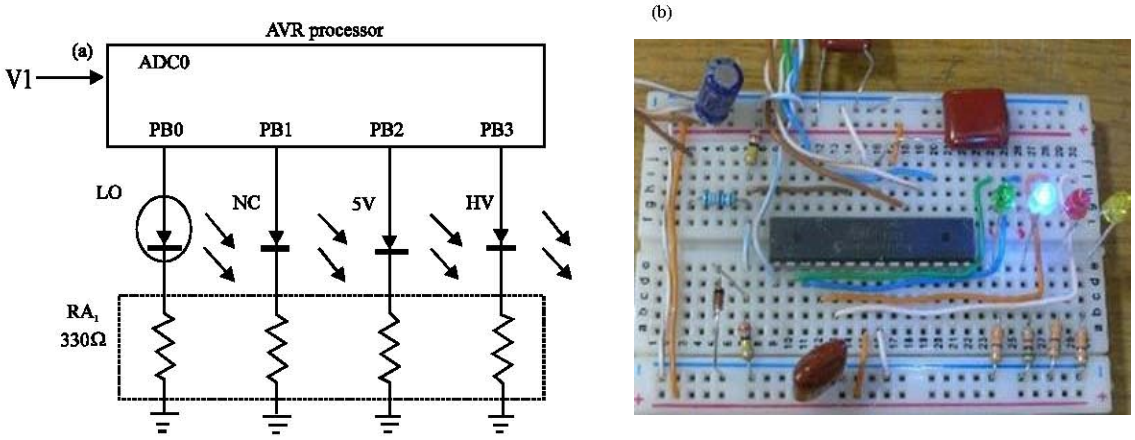

Fig. 12: Output circuit for experiment: a) Output circuit and b) Running at NC-state

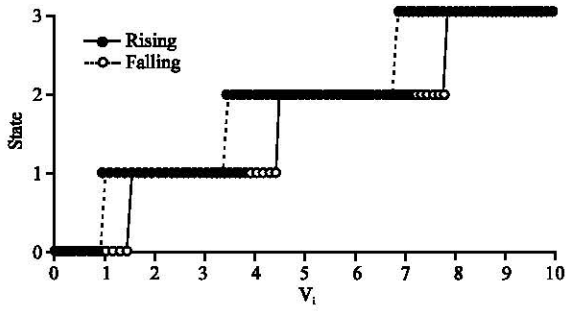

Fig. 13: Transition voltage in the input state

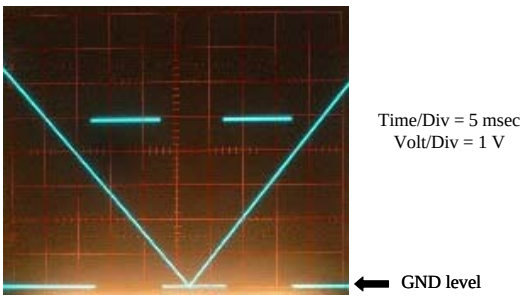

Fig. 14: Open load state of a LED indicator with a triangular input waveform

Table 4: Transition voltage in the input state

State/Direction	Min (V)	Max (V)
LO		
Rising	-	1.4
Falling	-	1.0
NC		
Rising	1.4	4.0
Falling	1.0	3.5
5V		
Rising	4.0	7.6
Falling	3.5	6.8
HV		
Rising	7.6	-
Falling	6.8	-

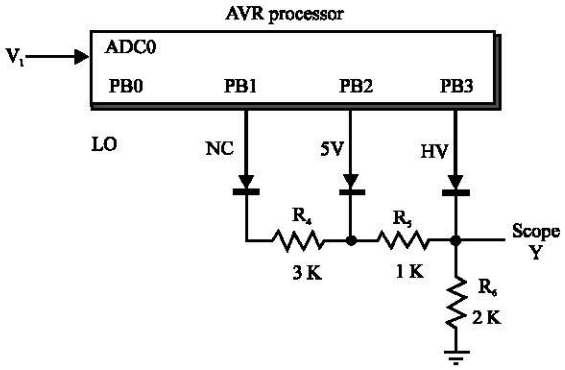

Fig. 15: Schematic circuit for measuring output transition

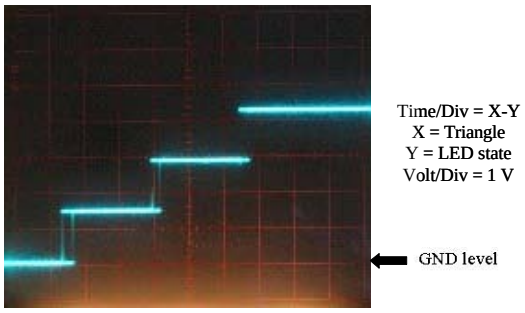

Fig. 16: Output transition of the proposed logic level display circuit

CONCLUSION

In this study, disadvantages of conventional logic level display circuit in logic lab-unit were investigated and an improved logic level display circuit is proposed by both hardware and software components. The proposed method can protect against the voltage exceeding the allowable input voltage and it can also detect the input state. Especially, disconnection of wire can be detected

by proposed logic level display circuit so that trials and errors are reduced. In order to verify the performance of the proposed method, experimental circuits were set and the operating conditions were tested. It operates normally from minus input voltage to over voltage. In addition, the logic state is displayed in four stages of open load, logical-low, logical-high and over voltage. The hysteresis characteristics are realized to overcome instability of transition and verified it through experiments.

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