Journal of Engineering and Applied Sciences 13 (Special Issue 3): 3232-3237, 2018
ISSN: 1816-949X
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Design of RF to DC Rectifier using Steep Slope Tunnel FET Device for RF Powered Systems

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Abstract: Radio Frequency (RF) harvesting is a process of converting the available ambient RF sources in to Dc electricity which can able to power up the ultra low power wireless sensor networks, charging systems, RFID applications and bio-implantable devices.There is a significant challenge in the design of rectifier part in the RF harvesting system, to improve the output dc power with Power Conversion Efficiency (PCE). The main objective of this study is to choose a suitable device and structure of the RF-DC rectifier circuit in the harvesting system which operates in high frequencies. The rectifying device such as schottky diode and diode connected MOSFET, used in the RF rectifiers are suffered with bad threshold voltage levels which makes a large increase in the channel resistance R_{on}, reduces the on-drive current and increase in the voltage drop which leads to high resistive power loss, low power conversion efficiency and acquire very low dc output voltage. To overcome the above issues, a GaN/InN steep slope tunnel FET device is proposed for an efficient structure design . The designed tunnel fet rectifier is thoroughly investigated with different design parameters such as number of stages input dbm, width of TFET, capacitor values and DC current of known load values. The simulation of the circuit shows that it can able to generate a power conversion efficiency of 26.8% for a minimum RF input of -15 dBm at 900 MHz operating frequencies, providing the output dc voltage of 2 V, 4 μA with a load resistive of 500 KΩ.

Key words: RF CMOS rectifier, energy harvesting, sub threshold slope, tunnel FET device, structure, load

INTRODUCTION

Radio-frequency energy harvesting has gain a lot of attention in the recent years and it also offers in various perspective applications for powering such as passive RFID system, wireless sensors networks, wearable bio monitoring system and future implantable medical devices, etc (Jayakumar *et al*., 2014; Khang *et al*., 2015; Tentzeris *et al*., 2014). The RF power level directly available from a normal cellular base station (Singh *et al*., 2013) with 20 W rating and 17 dbi directional gain is around 320 $\mu W/m^2$ from a distance of 500 m. The average available RF power ambient density from the cell phone towers in Malaysia is very small value of around 200-350 $\mu W/m^2$. The designing of RF to DC power converters with the available power density is very challengeable one. The micro power converters output can vary with amount of RF power transmitted its wavelength and the travelling distance between the signal source and the harvesting node. The average dc power P_{av} harvested (Kim *et al*., 2014) from the ambient RF signal can be represented in Eq. 1:

$$P_{av} = P_{Tx} - L + G_{Rx} + G_{Tx} + \eta_{RF\text{-}dc} \quad (1)$$

Where:
P_{tx} = The Power transmitted
L = The propagation Loss factor
G_{rx} = The antenna Gain of the receiver
G_{tx} = The antenna Gain of the transmitter
$\eta_{RF\text{-}dc}$ = The efficiency of rectifier circuit

The propagation Loss (L) of the radiated wave (Kim *et al*., 2014) without wave diffraction from the base station measured in decibels can be represented in Eq. 2 and 3:

$$L = F + 18\log\left(\frac{17h + R^Z}{17h}\right) \quad (2)$$

$$F = \left(\frac{4\pi R}{\lambda_0}\right)^2 \quad (3)$$

Where:
F = The Free space path loss
h = The height of the source
R = The distance from the RF source and
λ_0 = The wavelength
λ_0 = The wavelength of the signal emitted

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Therefore, a high-gain antenna and an active efficient RF-DC conversion circuit are needed to attain an optimum performance of the harvesting system. Rectifier is the most important components in the RF energy harvesting because the whole power conversion efficiency of the system will fluctuate due to the ambient RF environment. Under low RF input power or sub-milli watt level input, normal MOSFET technology suffered from the weak power conversion efficiency and the operating range is also limited. Moreover, the MOSFET technology is also limited to a sub threshold slope of 60 mV/decade (Li *et al.*, 2014; Yeo *et al.*, 2015). So, it can not able to provide the required value of current at low output dc voltages.

To overcome these drawbacks, Tunnel FET (TFET) device which is having the property of carrier injection mechanism as well as having the superior electrical characteristics at low voltages (sub 0.25 V) make it performs the method of RF to dc conversion at sub milliwatt power, hence, the sensitivity range of RF energy harvesting circuits can be improved. In this study, it is proved by means of simulations a high efficient GaN/InN tunnel FET based RF-DC rectifier was designed and it was thoroughly investigated.

MATERIALS AND METHODS

RF CMOS rectifier and its challenges: Owing to low on state resistance and small forward voltage drop (200-300 mv), Schottky diodes are commonly used in low power rectifier for a minimum level of RF input signal. At the circumstance of very high power range of 10 mW, the schottky high barrier diodes are achieving an efficiency of more than 80% because the matching is quite easy and it can deliver the dc power efficiently to the load due to very low ON resistance (Hemour *et al.*, 2014). However, the device requires to be biased or self-biased which requires energy and it fails to operate under very low power rectification. Moreover, Schottky diodes are incompatible in all CMOS technologies since high integration levels are required (Yuan and Bi, 2013; Hameed and Moez, 2015). This made a limit in its use in low cost applications. Later, MOSFET connected diode was used and it substitutes the Schottky diode. However, MOS devices are having higher value of threshold voltage which badly causes the reduction in the efficiency (Li *et al.*, 2014; Shokrani *et al.*, 2014). Following with that, to reduce the high threshold voltage in the MOS devices, the researchers (Dai *et al.*, 2015; Chouhan *et al.*, 2016) proposed a numerous threshold voltage cancellation techniques such as External-V_{TH}-Cancellation (EVC) Internal-V_{TH}-Cancellation

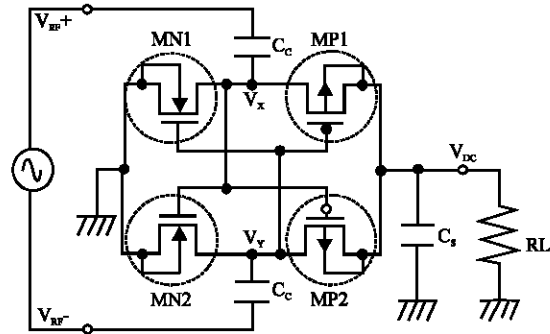

Fig. 1: Cross connected differential rectifier (Kotani *et al.*, 2009)

(IVC) and Self-V_{TH} Cancellation (SVC) techniques for increasing the efficiency of the rectifier. All the threshold cancellation technique requires an aditional circuitry of transistor, resistor and capacitor or external different bias voltage at different stage which makes the rectifier circuit become more complex (Dai *et al.*, 2015). Number of researchers (Shebanee *et al.*, 2015; Yeo *et al.*, 2010) uses a cross connected differential topology design which is shown in Fig. 1. A self V_{th} cancellation technique with less circuit complex and it has higher input reactance because the two differential inputs with less parasitic capacitance and the transistor sizes to be optimized as a tradeoff between being large for low Ron and small for high input reactance.

Sub-threshold swing is expressed as the inverse of the sub-threshold slope voltage which can generate a one decade increase in the drain current. The sub-threshold swing of the mosfets is given by the Eq. 4:

$$S_{s\text{-}th} = \ln(10)\frac{kT}{q}\left(1+\frac{C_d}{C_{ox}}\right) \quad (4)$$

At a maximum of C_{ox} value of 8, this yields 60 mV per decade at room temperature. So, under sub-mW level conditions, the current MOSFET technologies are limited to Subthreshold (SS) swing of 60 mV/dec which limits the required value of current at low output DC voltages Li *et al.*, 2014; Cavalheiro *et al.*, 2015). Hence, while designing the RF rectifier, it is very significant to consider the device structure and its operating characteristics. In other words, the threshold voltage, its bias characteristics and leakage currents are the parameters which plays a critical role in the rectifier's performance. From the literature survey, still there is a challenge remain in the rectifier to improve the sensitivity and PCE for the RF powered systems.

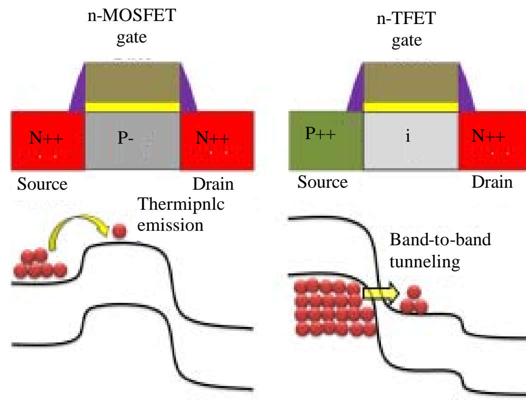

Fig. 2: Comparison of structure and energy band diagram of N-MOSFETS and N-TFET

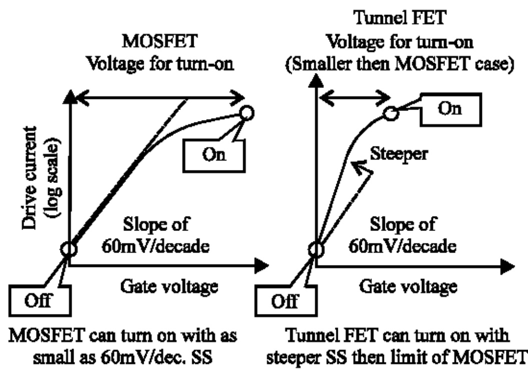

Fig. 3: Transfer characteristics of MOSFET and Tunnel FET

Steep slope tunnel fet device: In N channel-Mosfets, N+, P-, N+ doped region are acted as source, channel and drain terminal. TET is also similar in structure to the Mosfet butN-TFET is P+, I, N+ doped region are acted as source, channel and drain terminal. Compare to mosfets which is thermionic emission as a carrier injection mechanism, the TFET is Band-To-Band Tunneling (BTBT) based novel device concepts can able to reduce the operating voltage have attracted lots of attention. Figure 2 shows the comparison of basic structure and energy band diagram of N-Mosfet and N-TFET. Small sub-threshold swing means better channel control, e.g., improved on/off current which means less leakage and less energy.

The semiconductor band gap between source and channel in TFET acts as a natural filtering in carrier injection thus in principle enables TFET to turn on abruptly which indicates that the sub thre Shold Swing (SS) value of TFET can be reduced to below 60 mV/dec as shown in Fig. 3. The nature of steep slope characteristics in Tunnel Field Effect Transistors (TFETs), promising

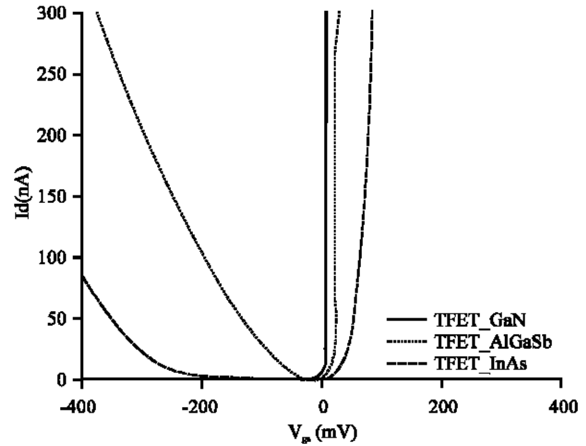

Fig. 4: Comparison of I_d vs V_{gs} characteristics of 20 nm GaN/InN, AlGaSb/InAs HTFET and InAs Double gate TFET

a new opportunity to replace the MOS-diodes in the design of RF rectifying system (Cavalheiro *et al*., 2015; Hemour *et al*., 2014).

Figure 4 shows the comparison of Id Vs Vgs characteristics of 20 nm GaN/InN HTFET, AlGaSb/InAs HTFET and InAs Double gate TFET device. It is clearly exhibits that GaN/InN Hetero junction TFET has very low threshold voltage of 0.096 V in forward bias and very less or negligible leakage of current in the reverse conduction. By having the steep-slope switching characteristics in HTFET which can improves the conduction current I_{on} and its unique unidirectional tunneling conduction makes the leakage loss to be minimized.

Tunnel fet based rectifier design: The drawbacks and limitation of current Mosfets technology and in order to meet the requirements of efficient rectifier under sub MW RF input operation, a 20 nm GaN/InN HTFET based rectifier is proposed and designed because of having the advantage of characteristics such as lower sub-threshold swing, low voltage operation and unidirectional tunneling.

A compact Verilog-A Model of GaN/InN Hetero junction Tunnel FET has been developed (Lu *et al*., 2015) and being utilized in the circuit implementations for investigation. A multistage structure was designed using TFET device with 25 number of stages operating at frequency of 900 MHz is used to employ the proposed rectifier as shown in Fig. 5. A 50 ohm antenna impedance is included in-front of rectifier in this design. The cross connected differential drive rectifier topology is chosen.

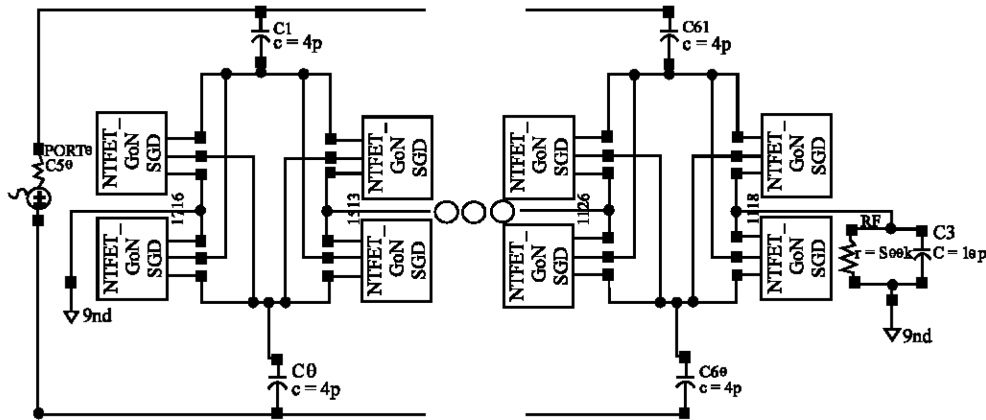

Fig. 5: Schematic of 25 stages GaN/InN HTFET cross connected rectifier

RESULTS AND DISCUSSION

The proposed multistage rectifier circuit is simulated in cadence spectre and obtained an output voltage of 2 V, 4 μA while performing a transient analysis with a time taken of 10 μ sec approximately as shown in Fig. 6. The obtained output voltage of 2 V is sufficient to run the RFID processing circuitry or charging the ultra low power battery circuit. The capacitance in each stage of the circuit influences a significant role in controlling the output current delay to the load. The variation of output voltage with different value of capacitance is shown in Fig. 7. To have an efficient RF-DC rectifier circuit, few design parameters were examined such as number of stages, width of HTFET, DC current of known load values and the sensitivity. Figure 7 also shows the number of stages vs output voltage. As per the simulation increasing the number of stages will increase the output voltage for certain stages and it becomes saturated and becomes decreasing.

At a constant RF input of -15 dBm, the output voltage increases to 2.7 V when increasing the stages to 50 stages, after adding the stages further, the output voltage becomes stable. The variation of the HTFET width was also examined in Fig. 8 which show the optimal value of 50 μm was observed for a maximum output voltage. The variation of the output dc current is also an important factor for the Rf-DC rectifier. To perform it in the simulation, the output load resistor value is sweeped from 100-1 MΩ in the simulation as shown in Fig. 8. It shows that when the resistor value increases the load current becomes decreasing and an optimal value of 500 KΩ is chosen to produce a load current of 4 μA drawn by the processing circuitry.

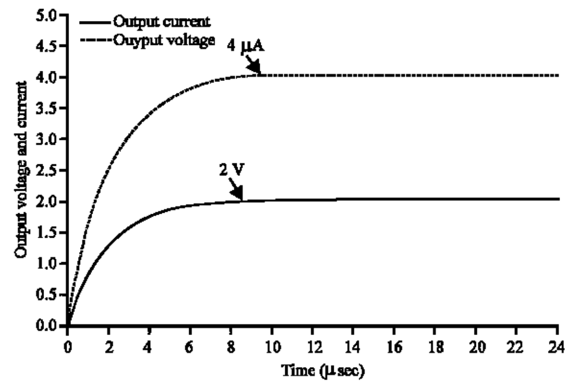

Fig. 6: Transient simulation of output voltage and current

To compare the operation of other rectifiers, power conversion efficiency is the most important factor. The following Eq. 6 is used to calculate the efficiency of the RF to DC rectifier:

$$\eta = \frac{P_{out}}{P_{in}} = \frac{\text{DC Power}}{\text{RF Power}} = \frac{\left(\frac{1}{T}\right)\int\left(V_{out} \times I_{out}\right)dt}{\left(\frac{1}{T}\right)\int\left(V_{in} \times I_{in}\right)dt} \quad (6)$$

The maximum power conversion efficiency obtained from the proposed rectifier is 57% at 80 stages as illustrated in the Fig. 9. Further increasing the stages, the efficiency becomes decreasing. The proposed circuit is optimized and produce an output voltage of 2 V, 4 μA, at 25 stages itself with an efficiency of 26.8%. The performance comparison of other related researches are are summarized in the Table 1. This optimized 25 stages can also achieved a highest sensitivity value of 35 dBm to produce a minimum variable output voltage.

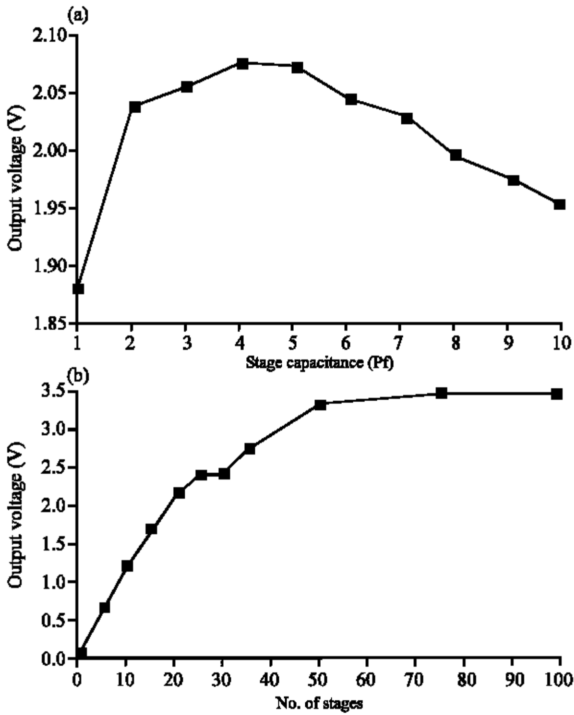

Fig. 7: Variation of output voltage vs. capacitance and No. of stages

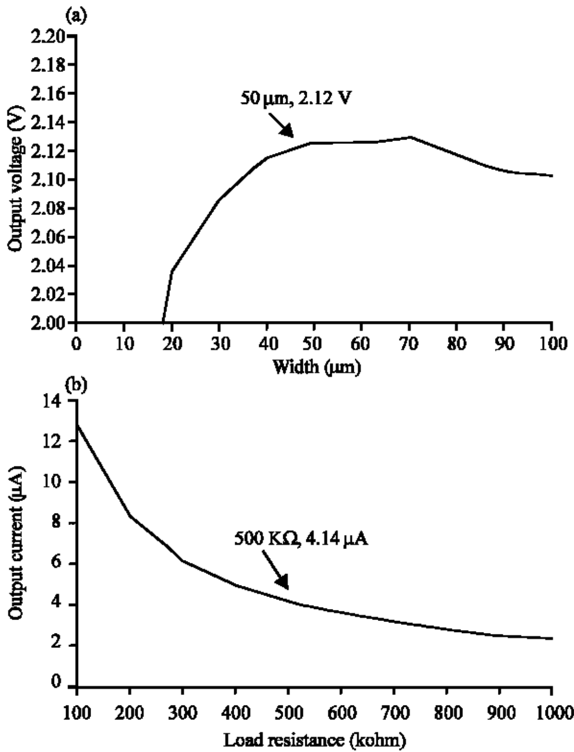

Fig. 8: Output voltage vs. width and current vs. load resistance

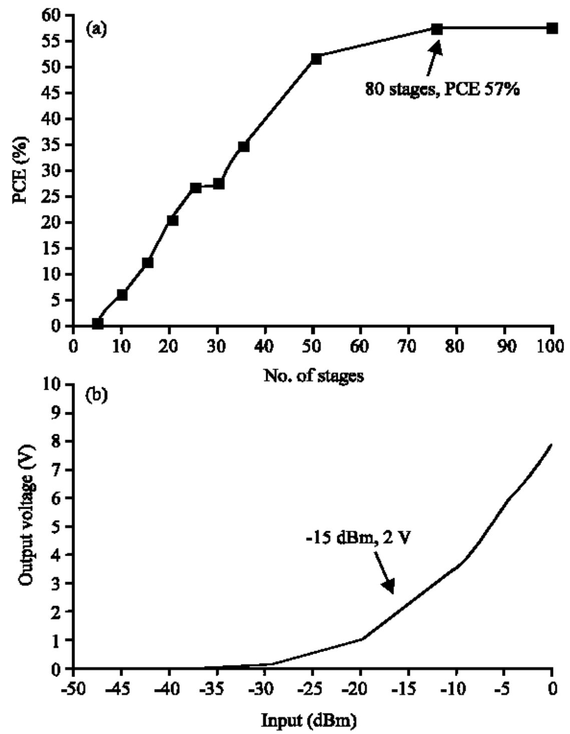

Fig. 9: PCE vs. No.of stages and output voltage vs. Input (dBm)

Table 1: Summary of performance comparison with other related research study

Reference/ year	Asl and Zarifi (2014)	Wang *et al.* (2015)	Cavalheiro *et al.* (2015)	Rsearcher (2016)
CMOS fabrication	180 nm CMOS	40 nm CMOS	20 nmGaSb/ InAs HTFET	20 nm GaN/In NHTFET
Device Vth	-	0.45 V	Sub 0.25	0.096
Rectifier topology	2-T doubler circuit	Full wave dickson	Proposed 4-T topology	Cross connected
RF frequency	900 MHz	900 MHz	900 MHz	900 MHz
RF input power/voltage	0.35 V	0.4-0.55 V	-55 to -5 dBm	-50-0 dBm
Output DC voltage	2 V	1.34 V	0.58 V @-20 dBm	2 V, 4 μA
PCE	10%	44%	61%@-43 dBm	57%@-15 dBm
Sensitivity	-	0.39V	-50 dBm	-35 dBm
No. of stages	13	7	-	25

CONCLUSION

In this study, the challenges faced by the RF CMOS rectifier were discussed and the limitations of the current mosfets technology has been addressed. A GaN/InN steep slope tunnel FET based RF to DC rectifier was proposed and simulated for the RF powered applications. The proposed tunnel FET device and 25 stages rectifier structure was employed in this method to generate DC output voltage. The DC output voltage variation of the proposed multistage circuit was investigated through

various design parameters such as number of stages input dbm, width of TFET, capacitor values and DC current of known load values. The maximum PCE obtained was 57% at the stages of 80 and achieved a highest sensitivity of -35 dBm. An efficient RF-DC conversion circuit was designed by analyzing the results extracted. To produce an output voltage of 2 V, the circuit is optimized to 25 stages, at a sensitivity of -15 dBm, operating frequency of 900 MHz with PCE of 26.8%.

ACKNOWLEDGEMENT

Researcher would like to thank Collaborative Micro-Electronic Design Excellence Centre (CEDEC), USM for supporting Cadence EDA tools

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