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Hardware Implementation and Testing of PAPR Reduction Using Order Bit Selector and Trellis Structure

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Abstract: Orthogonal Frequency Division Multiplexing (OFDM) is one of the well known and widely using multicarrier modulation method in digital communication system. In OFDM, the important parameter to be considered before transmission is to minimize the Peak Average Power Ratio (PAPR). In this study, the design and implementation of OFDM system along with Fragmentary Control Transmit (FCT), order bit selector and trellis structure is used to reduce the PAPR. The modified OFDM system is implemented on an FPGA board. The implementation results show the study of RTL schematic and test bench of the design. The results obtained from the proposed system have been compared with the existing system. It has been observed that the proposed system considerably better than the existing system.

Key words: Order bit selector, fragmentary control transmit, trellis structure, OFDM, PAPR, FCT

INTRODUCTION

One of the multicarrier modulation technique used in wireless communication is orthogonal frequency modulation. It as has been accepted for several wireless standards because of its advantages such as large spectral efficiency, robustness against multipath fading and less complexity in implementation. OFDM is a good modulation scheme for high data rate communication system. However, the practical implementation of OFDM is limited to certain extent because of its high Peak Average Power Ratio (PAPR) (Han and Lee, 2005). Due to its high PAPR it demands for excess transmitter power amplifier which has a very good linear range. It also demands for increased complexity design of data converters. Due to increase of sub carrier the high PAPR is obtained which is not effective. The existing schemes include Active Constellation Extension (ACE) (Krongold and Jones, 2003), Tone Reservation (TR) (Chen *et al*., 2011) and Tone Injection (TI) (Abdullah *et al*., 2011; Gayathri *et al*., 2017a, b) amplitude clipping and filtering (Wahab and Ain, 2010) and multiple signal representation techniques such as Iterative flipping algorithm (Tellado, 1999), Partial Transmit Sequence (PTS) (Muller and Huber, 1997; Cimini and Sollenberger, 2000), Selective Mapping (SLM) (Bauml *et al*., 1996). These techniques achieve PAPR minimization at the cost of increase in transmit power of signal and Bit Error Rate (BER). The data loss and computational complexity also increases.

Peak average power ratio: OFDM will have many modulated sub carriers which lead to problem of high PAPR. The coherent summation of N modulated sub carriers, peak power is increased by N than the average power in the base band signal. Hence, the intricate wrap of the OFDM transmitted signal is written as:

$$S(t) = \frac{1}{\sqrt{Y}} \sum_{m=0}^{M-1} M_m e^{j2\pi m\Delta f},\ 0 \le t \le MT \qquad (1)$$

Where:
j = It is given by ↓ -1
△f = The spacing of subcarrier
MT = It is given by the effective data block duration

PAPR is described as the proportion of maximum instantaneous power to its average power during OFDM symbol duration. The peak average power ratio of OFDM symbol can be represented as:

$$PAPR = \frac{\max_{0\le t\le NT}\left[|x(t)|^2\right]}{1/NT\int_0^{NT}|x(t)|^2\,dt} \qquad (2)$$

where, x(t) is input signal. The idea behind scaling down PAPR is to decrease the maximum power of signal x(t). Since, predominance of the system demands the discrete-time signals, dealt is sampled by amplitude in most of the peak average power reduction techniques. The time domain L-times oversampled samples are

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derived by an LN-point Inverse Fast Fourier Transform (IFFT) of the given data block by considering zero-padding.

FPGA implementation: A Field-programmable Gate Array (FPGA) is an integrated circuit design, after manufacturing it the designer will configure the design. The configuration of FPGA is by using a specified Hardware Description Language (HDL). Any logical function can be implemented using FPGAs. FPGA consists of programmable logic components such as logic blocks and a reconfigurable interconnect which connects the block together. It is like numerous logic gates that can be connected in different configurations. The simple and complex combinational functions are performed by configuring the logic blocks. In many of the FPGAs, the logic blocks consist of block of memory or memory elements (Lakkannavar, 2012; Reddy and Reddy, 2013). Along with digital functions, some FPGAs also have analog features. The slew rate and drive strength are the most common analog feature which allows the designer to set slow rates and faster rate on lightly and heavily loaded pins, respectively on high-speed channels. The data convertors can be integrated along with signal blocks in some mixed signal FPGA (Kaur and Mehra, 2012; Farahani and Eshghi, 2007).

Figure 1 depicts the Atrix-7 FPGA board. The FPGA used for this project implementation is Artix-7. The Artix 7 family FPGA is fabricated on 28 nm high performance, low power product which is used for mainly bio medical instruments, military radios and some compact wireless system. One of the high end features of Artix-7 FPGAs is integration of advanced Analog Mixed Signal (AMS) technology. It has eight 7 segment display, 16 switches and 16 output LED. The board can be connected to computer using Jtag cable where the communication happens between the system and the Atrix 7 board.

PAPR reduction approaches: There are two main categories to reduce PAPR in OFDM signal namely signal distortion technique and signal scrambling technique.

Signal distortion techniques: One of the most effective and simple technique to minimize PAPR is amplitude clipping and filtering. The logic behind this is to set a threshold value, if the signal is above the threshold value then the amplitude peak is clipped off. If the threshold value is more than the samples clipped will be less which decreases the CCDF. If the CCDF decreases the clipping threshold increases and PAPR reduces. Clipping is a non linear process where the distortion is viewed as noise. Another approach to reduce PAPR is peak windowing technique. Here, the Gaussian shaped window is multiplied to a huge signal peak to minimize PAPR. The

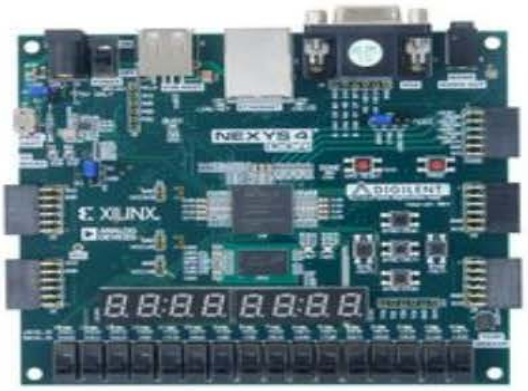


Fig. 1: Atrix-7 FPGA board

obtained spectrum is a convolution of indigenous OFDM and window spectrum. This technique scales down PAPR at a demand of raise in bit error rate.

Signal scrambling techniques: Linear codes are also used to reduce PAPR. In this method the proper codeword is chosen for transmission. Coding scheme uses a known data block with constellation modulation such as QPSK and PSK. The code word which is having high peak power is blocked from transmission. This method is useful only for limited number of sub carriers where PAPR reduction is achieved.

The main objective of tone injection approach is to expand the size of constellation and map the individual constellation to its analogues points. For every symbol in the data block there are many constellations which are mapped in extended constellation. The amount of scaling down of PAPR is dependent on the modified symbols in the data block. As this method uses the same frequency band for injected signal, it is more complicated when compared to tone reservation. Due to injected signal the power requirement and the implementation complexity increase. Tone reservation is one of the efficient methods used for minimization of PAPR. The fundamental concept is to reserve the tone both at transmitter and receiver. In tone reservation the main aim is to know the value of time domain signal with the help of convex optimization problem which can be determined using linear programming.

Active constellation technique is another method used for PAPR reduction. The outer signal constellation is expanded towards outside of the indigenous constellation, so, the PAPR is scaled down. This can be implemented in different modulation techniques such as QAM, QPSK and MPSK. The combination of additional signals can be used for peak cancellation. This method reduces the bit error rate and no side information is required for transmission. But it demands for a larger

constellation size in modulation technique. One of the probabilistic schemes used for PAPR reduction is selected mapping. This method creates a similar OFDM signals in time domain which are asymptotically independent. For these parallel input data the phase sequence are multiplied and then IFFT is applied for each data. Out of that many data series the one having a less PAPR is chosen and transmitted. Each data block is weighted with a unique phase sequences which results in 'S' different blocks of data. Along with these altered data block the one with less PAPR is selected for transmission along with the corresponding phase vector as side information. The reduction of PAPR relies on the design of phase factor and number of phase sequences.

In OFDM the powerful probabilistic based PAPR reduction methods is Partial Transmit Sequence (PTS). In this scheme the actual data X is splited into N non-overlapping sub blocks. In each individual sub-block the sub carriers are weighted by a phase factor. The selection of phase factors make sure the PAPR is reduced. The flow of PTS algorithm is the OFDM sub carrier is split into M separate sub series. For every sub series the OFDM signal is generated by taking IFFT. The OFDM signal combined with weighted phase factor b_i. By using optimization algorithm the phase factors are generated. To retrieve the data at the receiver, receiver should have the generation scheme.

MATERIALS AND METHODS

Proposed algorithm: The binary data is the input to the OFDM system. The stream of binary data is given to the convolution encoder. The encoded samples are modulated using QAM modulator. After modulation the discrete cosine transform and wavelet transform is applied in order to minimize the PAPR of OFDM system. The output is then applied the conventional OFDM and PTS technique. The output from PTS technique is given to the AWGN channel and at the receiver end the inverse procedure of the transmitter will be done and finally the BER is calculated (Gayathri *et al*., 2017a, b).

Order bit selector: In communication systems the simplest way of channel coding technique is convolution coding. By virtue of its high coding gain and performance it is frequently used in wireless communication systems. The convolution coding is suitable for noisy channel such as Additive White Gaussian Noise (AWGN). In order to control the error the channel encoding is used. The basic building block of the convolution encoder is a shift register. It requires less hardware and storage memory. The convolution encoder is mainly defined by 3 variables namely, n, k, L where 'n' is number of input bits,

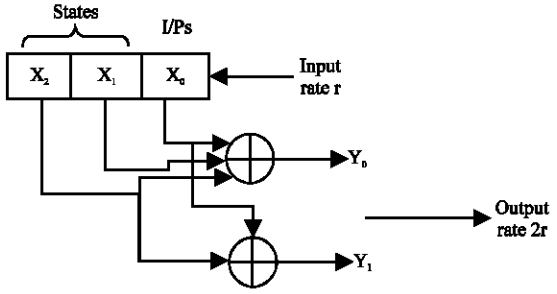


Fig. 2: Block diagram of convolution encoder

'k' is number of output bits and L is number of shift registers used as memory elements which are also called as constraint length. The code rate r is given by r = k/n. Figure 2 shows the sketch of convolution encoder for (n, k, L) = (2, 1, 2).

To obtain output at the encoder the two previous input bits and one present input bit are used. The output Y_0 and Y_1 is generated by using modulo-2 addition which is denoted by:

$$y_0 = x_0 \oplus x_1 \otimes x_2$$
$$y_1 = x_0 \oplus x_2 \quad (3)$$

After convolution coding the order bit selector is used to select the QAM constellation such that the PAPR is reduced.

Trellis diagram with Viterbi decoder: At receiver for convolution encoder viterbi decoder is used. Viterbi decoder uses two basic operation synchronization and quantization. The synchronization is used to know the range limits of code word and symbol. The quantization is used to quantize the analog signal and converter to digital using quantization square. There are two types of quantization techniques used in viterbi decoder. They are:

- Hard decision
- Soft decision

Hard decision: The decoding process uses the trellis diagram and Hamming distance. It is quantized into one bit precision either 0 or 1. The Hamming distance is used to measure the distance between the expected data at the decoder and the data transferred from the encoder.

Soft decision: The information when transmitted over a Gaussian channel is decoded using probability decoding. It uses multi bit quantization for received bits. If there 3 or 4 bits of quantization the performance is better than the hard decision. The Euclidian distance is used to measure the distance between the bits. Figure 3 shows the internal

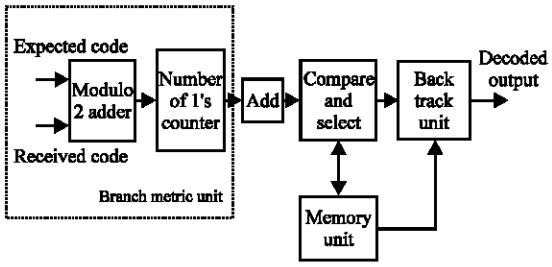


Fig. 3: Internal architecture of viterbi decoder

flow diagram of viterbi decoder. The functional blocks of viterbi decoder are branch metric unit, add compare and select unit, memory unit and back track unit. The steps involved in the viterbi decoder are as follows:

- The two parallel bits are inputs to the viterbi decoder
- The Hamming distance of the expected code and received cod is calculated by using modulo 2 additions. Number of one's is counted to measure the distance
- The previous stage and present values are added and compared to select with the minimum path value to reach the next node
- The each stage calculation is stored in the memory for further processing
- The back track unit is used to compare and track the optimal path value and the corresponding output is produced

Trellis diagram: Figure 4 shows the general trellis diagram used in decoder. It has four rows of horizontal dots where each row depicts one state of encoder. The solid line joining the dots illustrate the input transition bit is one and the dotted line connecting the dots represent when the input transition bit is zero. To achieve better performance soft decision is used. The distance between the received codes and all possible codes are computed. Here, the Hamming distance is used to compute the distance. The computation of Hamming distance is easy, it counts how many bits are different from received code to the all possible codes. The output of the hamming distance can be 0, 1 or 2. At each unit of time the hamming distance is computed and it is called as branch metric. These values are stored and accumulated to compute the optimal path. The FPGA flow includes the following steps.

Design entry: To achieve the proposed system the HDL language such as verilog is used.

Synthesis: The proposed design is synthesized into a hardware circuit that includes the logic blocks.

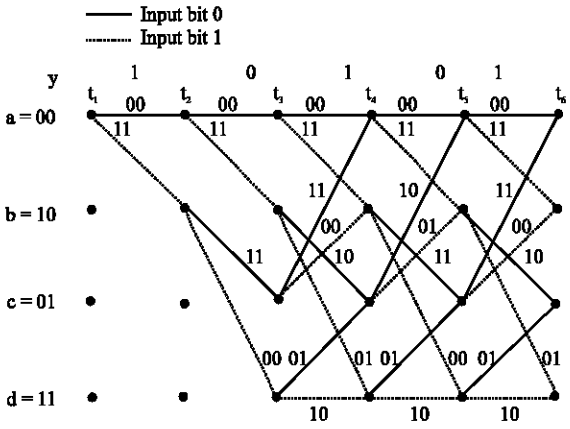


Fig. 4: Trellis structure

Functional simulation: The synthesized circuit is verified with its functional working.

Implementation: The logical blocks are placed into the actual FPGA with the help of netlist. It also chooses interconnecting wires in the chip to make the required connections.

Programming and configuration: The proposed circuit is programmed on to a FPGA chip by fusing the switches that composed of logical blocks and establish the required wiring connections.

RESULTS AND DISCUSSION

Quadrature Amplitude Modulation (QAM): Figure 5a shows the RTL schematic of QAM modulator and demodulator. The QAM is a combination of amplitude and phase shift keying. Here, the bits entering to the modulator is divided into two equal parts namely quadrature and in phase which is multiplied by cosine and sine values, respectively. These 2 modulated signals are combined at the source and then transmitted. At the receiver the two signals are separated and sampled at every time instant. Then the decision is made accordingly it is one or zero. For the different phase shift different mux is been used as shown in the Figure 5a. The input data is 8 bits for those bits the sine and cosine values are generate and multiplied in order to get the different phase shift. These two multiplied signals are summated and then transmitted.

Figure 5b depicts the simulation results of QAM modulation. Here, we can observe that the rst line should be always high in order to obtain the output. After 15.65 nsec the output is obtained. At every falling edge of the clock we can observe the output change.

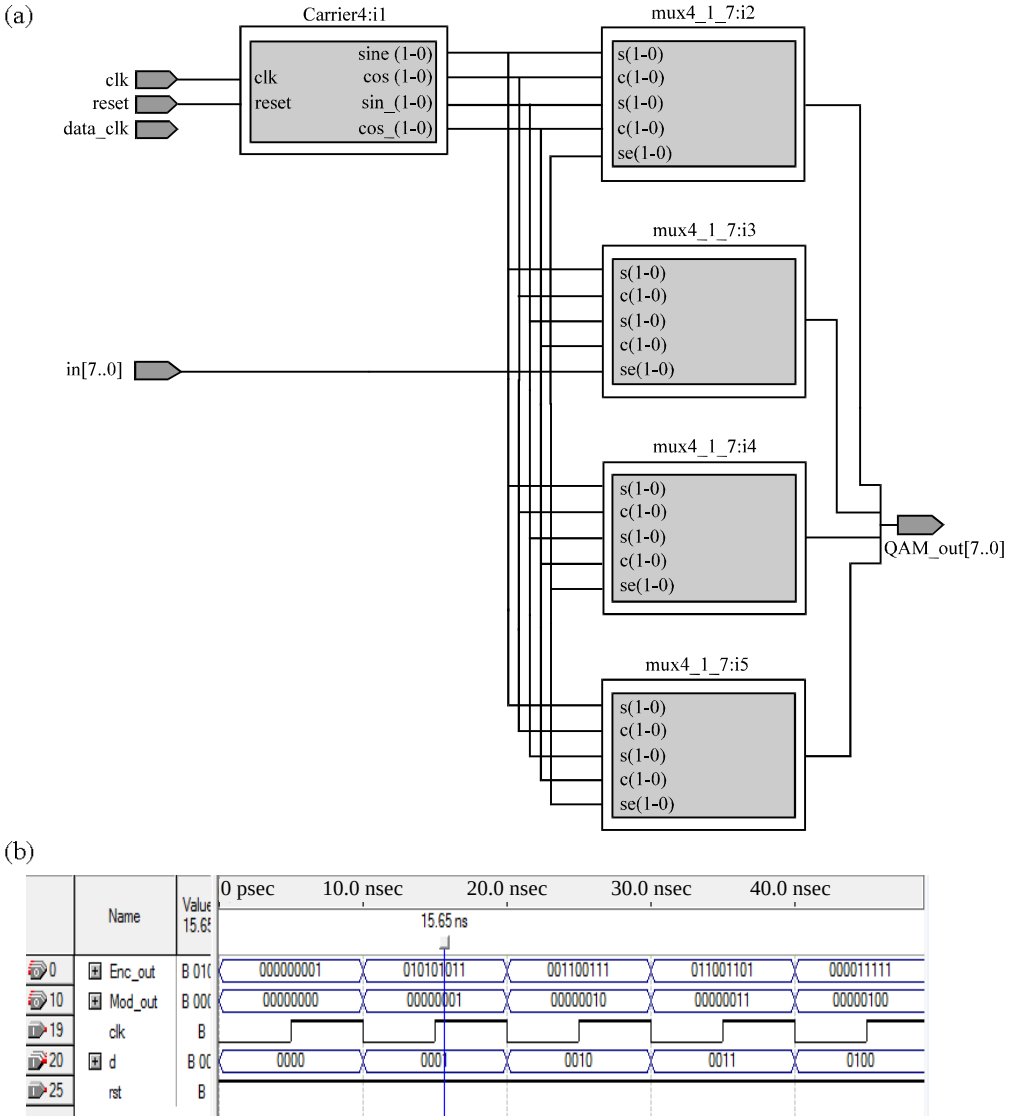


Fig. 5: a) RTL Schematic of quadrature amplitude modulation and b) Simulation results of quadrature amplitude modulation

Order bit selector: In the presented method, the data input is converted into binary stream. The binary stream is encoded by using the order bit selector technique as shown Fig. 6a. This example uses the rate 2/3 feed forward order bit selector depicted in the Fig. 6a.

OFDM: Figure 7b shows the simulation results of conventional OFDM. The random 5000 samples are taken at the input of the OFDM and the output of the OFDM is modulated and then transmitted. These 5000 samples which is entering the modulator is divided into 8 bits of data. The white colour oval in Fig. 7b shows the change in modulated output for every different 8 bits of the incoming input.

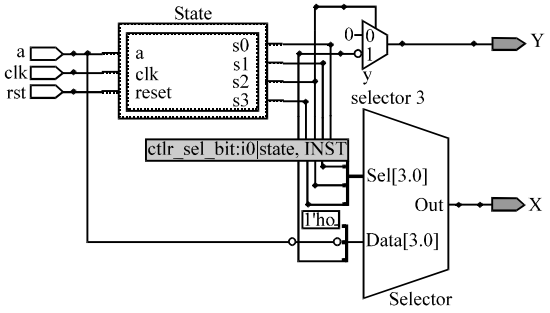
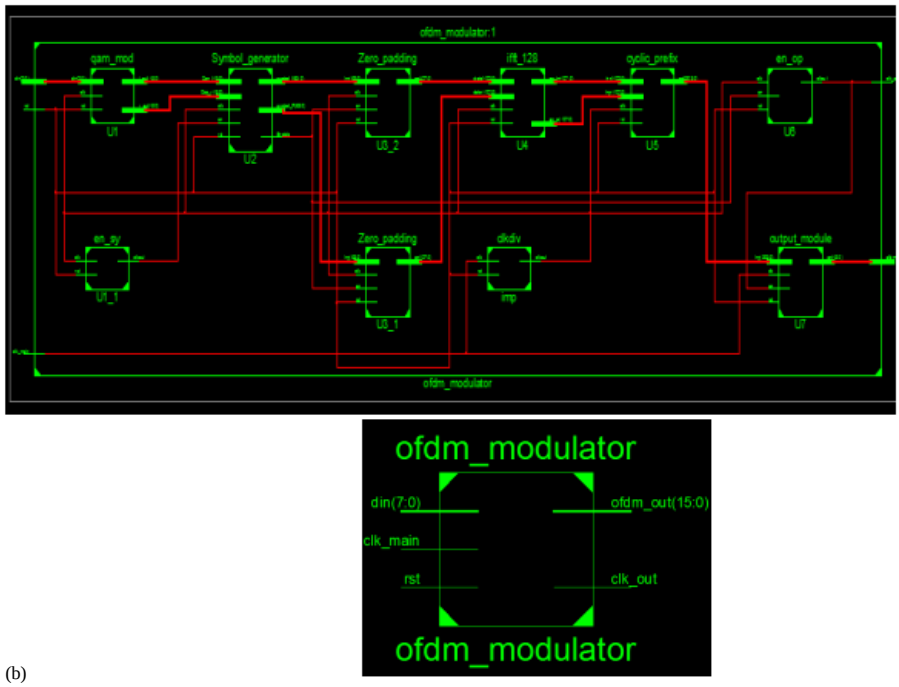


Fig. 6: A RTL schematic of order bit selector

Figure 7a shows the RTL schematic of conventional OFDM modulator. The input is modulated using QAM

(a)



(b)

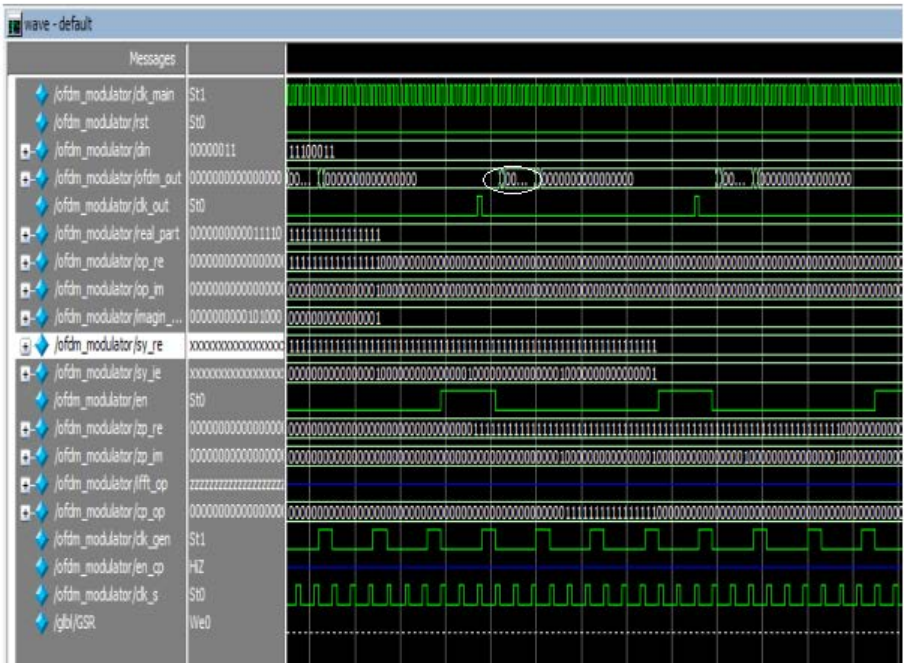
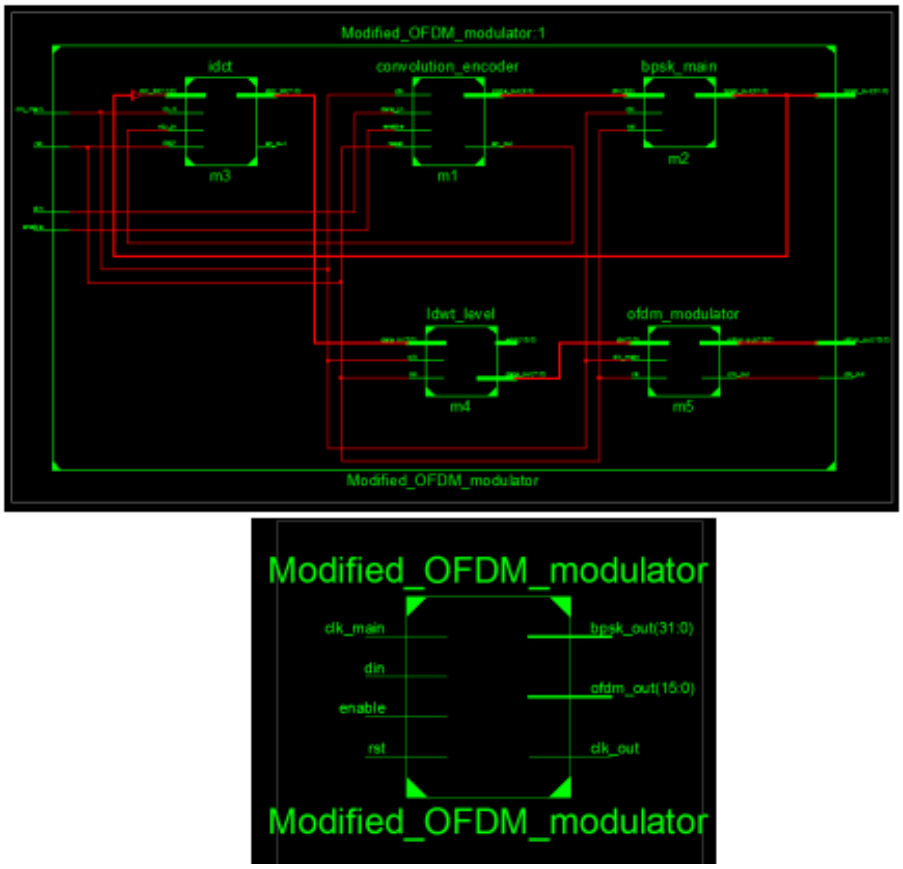


Fig. 7: a) RTL schematic and top view of OFDM system and b) Simulation result of OFDM system

modulator. After modulation the symbols are generated where each symbol are of 8 bits. The output of the symbol generator block is given as the input to the zero padding and then the 128 point IFFT is calculated. The output of IFFT is fed to cyclic prefix. In order to avoid ISI and ICI the cyclic prefix is done. Then finally the output module gives the conventional OFDM output.

Proposed OFDM system: Figure 8a depicts the simulation results of presented OFDM system. The random 5000 samples are taken at the input of the OFDM and the output of the OFDM is modulated and then transmitted. For the same conventional OFDM the IDCT and IWPT are combined and then the modulated signal is obtained.

(a)



(b)

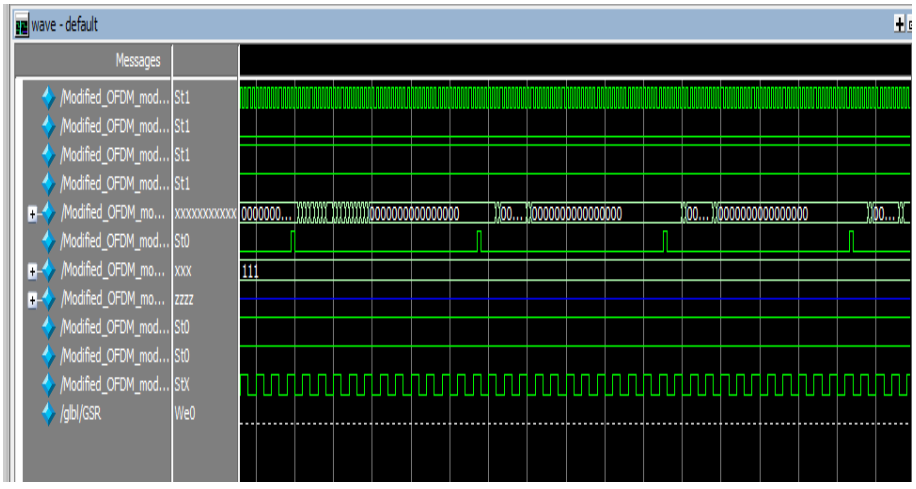


Fig. 8: a) RTL schematic and top view of proposed OFDM system and b) Simulation result of proposed OFDM system

Figure 8b shows the RTL schematic of modified OFDM modulator. The input is given to the convolution encoder. The output of convolution encoder is modulated using BPSK. The output of the modulator is given to the IDCT for auto correlation. The output of the IDCT is given to the wavelet transforms and then the final output is taken after the conventional OFDM modulator. The white colour oval shape on the Fig. 8b shows the output of the modified OFDM for every change in the input. We can observe that after 16 clock cycles we can see the output of the OFDM modulator.

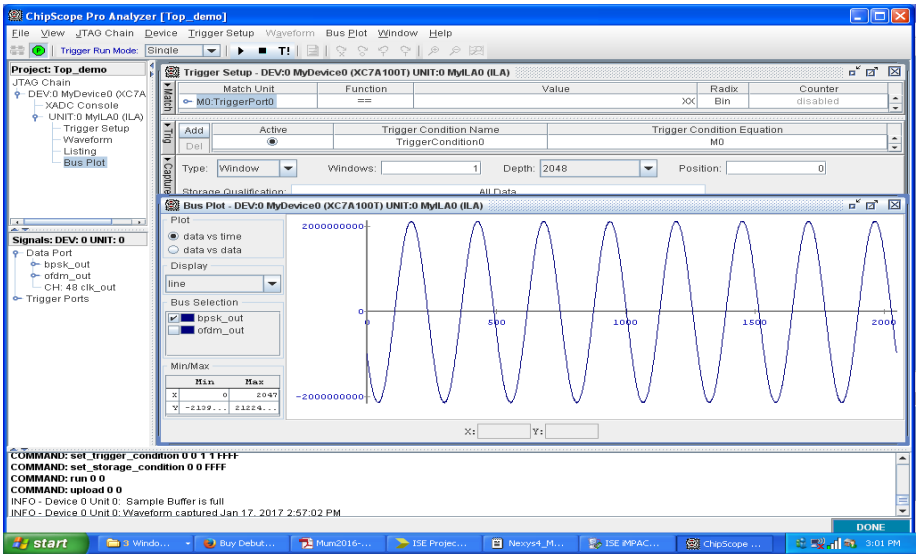


Fig. 9: Chipscope pro-result

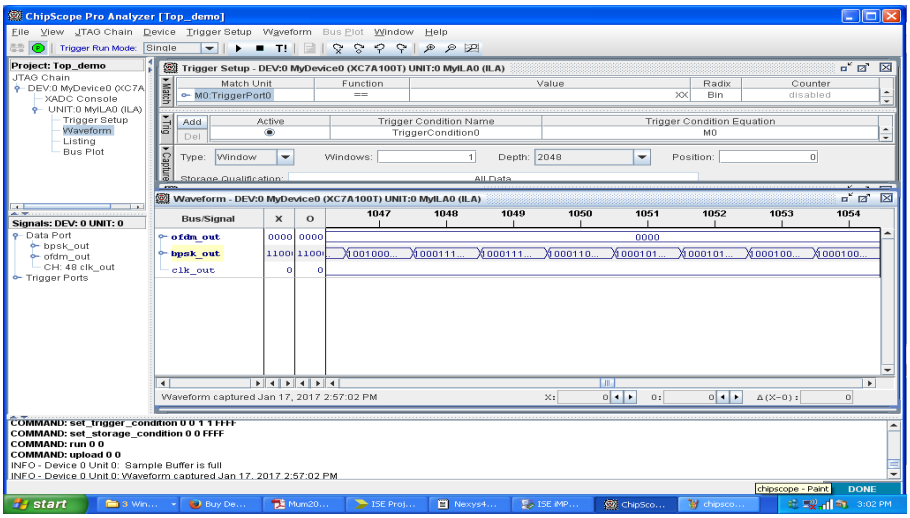


Fig. 10: OFDM result on chipscope pro

Chip scope is embedded software logical analyser for intermediate signal. The results of modulation technique on chip scope pro are shown in Fig. 9. Figure 10 shows the entire proposed design result on chip scope.

The FPGA board is connected though the JTAG cable. The entire code is converted into bitmap file and then it is dumped on to the selected FPGA board. Figure 11 shows the code dumped on to the FPGA successfully. Figure 11 shows the output on FPGA board. Once, the enable pin is high for the given input the outputs will be displayed on LED.

The area utilised for the proposed design is shown in Table 1 and 2. The estimated number of slice registers,

Table 1: Device utilization data

Device utilization summary (estimate values)

Logic utilization	Used	Available	Utilization (%)
Number of slice registers	1962	126800	1
Number of slice LUTs	6989	63400	11
Number of fully used LUT-FF pairs	1350	7601	17
Number of bonded IOBs	53	210	25
Number of BUFG/BUFGCTRLs	3	32	9
Number of DSP 48E1s	30	240	12

Table 2: Timing summary

Particulars	Values
Speed grade	-3
Minimum period	17.366 nsec
Minimum input arrival time before clock	1.298 nsec
Maximum output required time after clock	35.678 nsec
Maximum combinational path delay	No path found

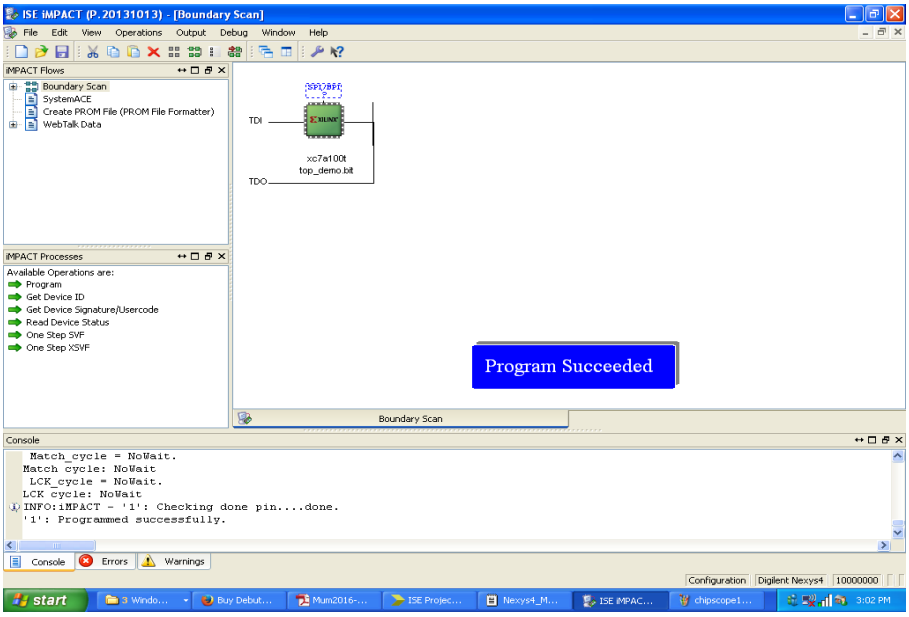


Fig. 11: Verilog code implemented on FPGA board

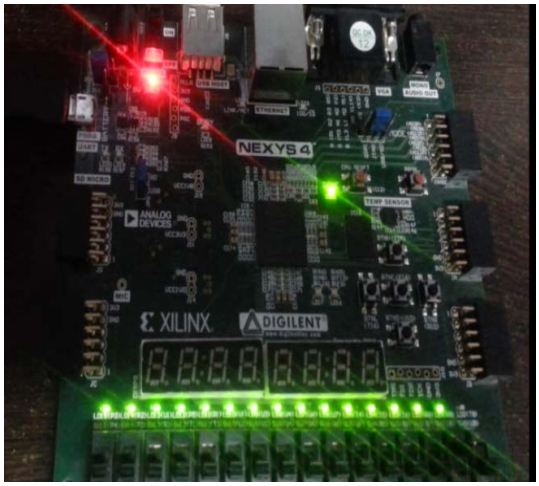


Fig. 12: Output on FPGA board

LUTs and IOBs are given in table. It shows that hardly 12% of the overall device is used for the proposed design. The timing report of the entire design is shown in Table 2. The speed grade of the selected FPGA is-3. The maximum operating frequency is 57.584 MHz. The clock to output delay is 35.678 nsec. In the proposed design there is no combinational path delay.

CONCLUSION

In digital communication system OFDM is an well organised multi carrier modulation method. In this study, we have presented modified OFDM system for PAPR minimization. In most of the PAPR reduction techniques there is a small amount of reduction in PAPR but the computational complexity has increased along with the BER. One of the major contributions during the development of the proposed system is the integration of FCT, order bit selector and trellis structure. The overall performance of the system is improved and we can say that the presented system is efficient and better in terms of reduction of PAPR and improvement in BER. The proposed system is simulated, synthesized and implanted on to FPGA board. The hardware implementation of the design shows the complexity of the proposed design. It can be seen that the overall device utilization is almost 12.5% of the selected FPGA. It can be observed in the result that it has been able to achieve the reduction in the PAPR with reduced hardware complexity.

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