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Review Paper on Wireless Network-on-Chip Architecture

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Abstract: As fabrication technologies continue to provide smaller transistors, the number of processing cores that in multi-core processing systems increased. Large amount of data is transferred between these processing cores using Network on Chip (NoC). Fast NoCs are required for this task. Recently, wireless networks concepts is proposed to be used in NoCs. In the past decade, attention has been paid to Wireless Network on Chip (WiNoC). This research investigates the latest improvements in the field of WiNOC since the year 2014. It is intended for this research to cover the state of the art of the latest proposed research in this era. Several research study have been studies in this research. The study's focus varied on different topics starting from system level down to the circuit levels. All of these levels have been covered in this research. Tens of research papers have been studied in preparation for this research. Only ten study which have vital contributions are presented. The discussed contributions varied on different levels starting form circuit level up to application level. Challenges and suggestions for future research are presented at the end of this study.

Key words: WiNOC, MPS, parallel processing, architecture, latency, power area, CMOS

INTRODUCTION

Adaptive using advanced fabrication technologies con-tributes to reduce size, increase speed and decrease power consumption of transistors. This improvement led to produce more complex integrated circuits where complete computer system has been built on a single IC (system-on-chip). The SoC contains all functional elements of a computer system including a processor on chip memory and all other peripheral components (Martin and Chang, 2001). The multi-core-system-on-chip is a more sophisticated version of SoC. This system is an integration of a number of one or more types of heterogeneous processing units, general purpose processors, DSPs or specific processors (Devigo *et al*., 2015). These processing units (cores) simultaneously cooperate to implement complex tasks. It consists of a number of hardware processing cores that cooperate to process large scale tasks simultaneously. As a parallel computing system, SoC is demanded on many scientific and commercial applications like weather forecasting, bioinformatics applications, data analysis, CAD or video rendering.

To get high efficiency of this multiple processor system on chip, processing units (cores) have to be connected by a high efficiency network. This network should satisfy special requirements. These requirements are high bandwidth, low latency and low power consumption. Figure 1 shows an example of multi-core

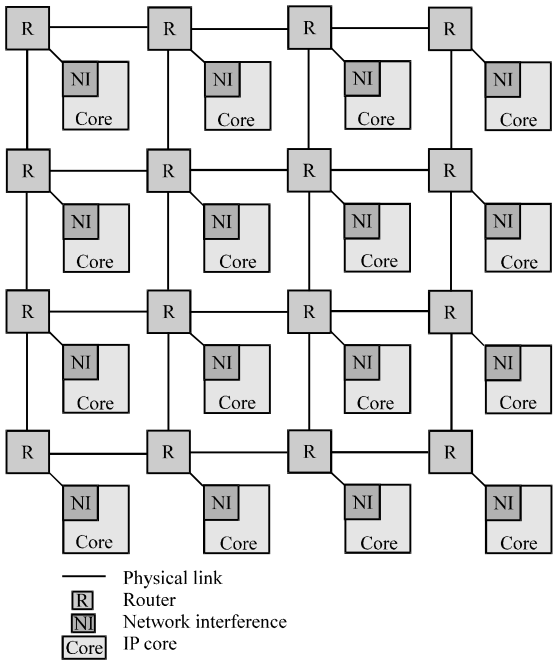

Fig. 1: An example of multi-core system on chip. It consists of a number of processing cores that are connected using connection links. In this particular case 2D mesh network is used (Liu *et al*., 2012)

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system on chip. It consists of a number of processing cores that are connected using connection links. In this particular case 2D mesh network is used. The links are connected using routers that are distributed at each cross. The processing cores are connected to the network through the network interface unit.

Conventional electrical interconnects that use metal wire has several problems such as high latency and limited off-chip bandwidth. They also, dissipate high energy compared to performing a single floating point operation. Wireless and photonic interconnects are strong candidate to solve this problem. This research investigates the latest update in this tropic and it focuses on the research study published, since, the year 2014.

Motivation: WiNoC has been an emerging technique in multi-core processing system. The performance of such system can be increased by providing a high speed communication networks. In the past decade, attention has been paid to WiNoC. This research investigates the latest research in the field of WiNOC, since, the year 2014. It is intended for this research to cover the state of the art of the latest proposed research in this era. Several research study have been studies in this research. The study's focus varied on different topics starting from system level down to the circuit levels. All of these levels have been covered in this research.

Research questions: The goal of this research is to study the WiNoCs and how they can be adopted in the NoC. In addition, it studies the architectures and performances of the recently proposed research. The four main questions of this research is trying to answer are:

- Why do wireless network have advantages over conventional electrical networks?
- How are the concepts of WiNoC can be adopted in NoC and what are the recently proposed architectures?
- What are the latest state of the art contributions?
- What are the challenges facing improvements of WiNoC?

MATERIALS AND METHODS

wireless networks: Several factors stands by suggesting the wireless link over wired in muli-core processing systems. In this study, we will try to analyze some of these factors. Most of the information in this study has been adopted from research by Abadal *et al.* (2015) and Laha *et al.* (2015). The study is tries to answer the first two research questions that this research is trying to answer: Why do wireless network have advantages over conventional electrical networks? And how are the concepts of WiNoC can be adopted in NoC and what are the recently proposed architectures?

It has been observed that when the distance of electrical meta wire links increases, the capacitance and resistance also increases. In addition, electrical wires require a number of inverters to serve as repeaters while the signal is propagated. These two factors, wire distance and repeaters, represents some of the reasons behined the high energy per bit that the conventional electrical link has. For this reason, long distances electrical wires suffer from high energy dissipation and high latency. In addition to these factors, wired links required number of repeaters and switches that in order to use them in a network. These components consumes substance amount of the overall energy fed into the network. For comparison purposes the energy transferred bits module is used. Figure 2 shows the energy per bit for three main interconnect technologies including electrical, wireless and photonic. This figure has been adopted from a research by Abadal *et al.* (2015). The energy per bit in this figure for the electrical and photonic links is calculated using the DSENT modeling and simulation tool (Sun *et al.*, 2012). The energy data for the wireless link is estimated using trends in wireless interconnect technology. Such data are available at Kaya *et al.* (2013). According to the data in this figure wireless interconnects have constant and low energy per bit compared to the conventional electrical links for more than 10 mm distance. It is also shown that

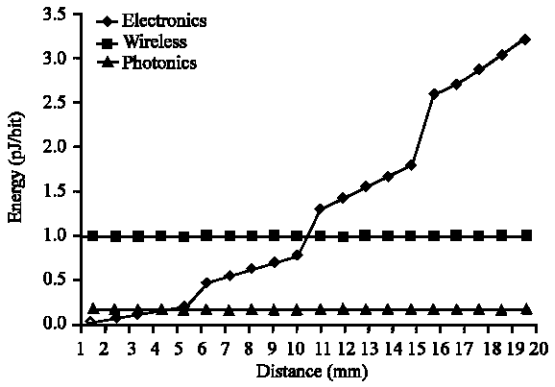


Fig. 2: Energy per bit for three interconnect technologies candidate for building NoC on multi-core systems: electrical (blue color), wireless (red color) and photonics (green color). It is clear how the energy consumed in the electrical networks is dramatically increased as the number of transferred bits is increased (Laha *et al.*, 2015)

the energy consumed by the wireless links is independent of the number of transferred bits. In the other hand, energy consumed in the electrical links is dramatically increased as the number of transferred bits is increased. Photonic interconnects show low energy dissipation per bit. In the same time, however, this does not include the energy consumed by the laser and the energy consumed in other devices such as splitters. Counting these extra energy costs in addition to the transmitting energy of the photonics will push the photonics out of the comparison by high difference. In this case the wireless links arethe stronger candidate unless small, low-power and cheep lasers guns can be fabricated on silicon substrates. For this reason, wireless interconnects have two advantages over the photonic in terms of the technology required for fabricating such networks and power consumed per bit transferred of it.

In addition to energy, several other factors are important in evaluating wireless links. Both bandwidth and latency are important factors for network on chip technologies. Wireless signals propagate very fast compared to their technologies. With near the speed of light, data transferred over wireless links can be received in one clock cycle considering all the time starting form after modulation to receiving the signal by the transducer of the receiver. Meanwhile, electrical links that use metal wires could take about three or four cycles to transmit a signal for 20 mm within the same chip. The number of cycles is increased to order of hundreds at transmitting signals between chips. Bandwidth is an important factor based on what the inter connects technologies are compared. In this factor, the wireless technology is limited by the frequency bands available for such communication tasks. In wireless, channels each with different frequency band is required to increase the bandwidth. In the other hand the bandwidth of the electrical connections can be directly increased by adding extra wires. However, this will increase the area of the systems and power dissipated by these wires. From the obove discussion, it is easy to see that wireless networks have limited bandwidth but every efficient power consumption and low latency when they are used for long distance communication that are more than 10 mm.

For this reason, wireless networks have been used in the multi-core processing systems in addition to the conventional wire networks for the long distance communication for their favorable characteristics, low power consumption and low latency. Several other benefits that wireless links have over other type of connections such as:

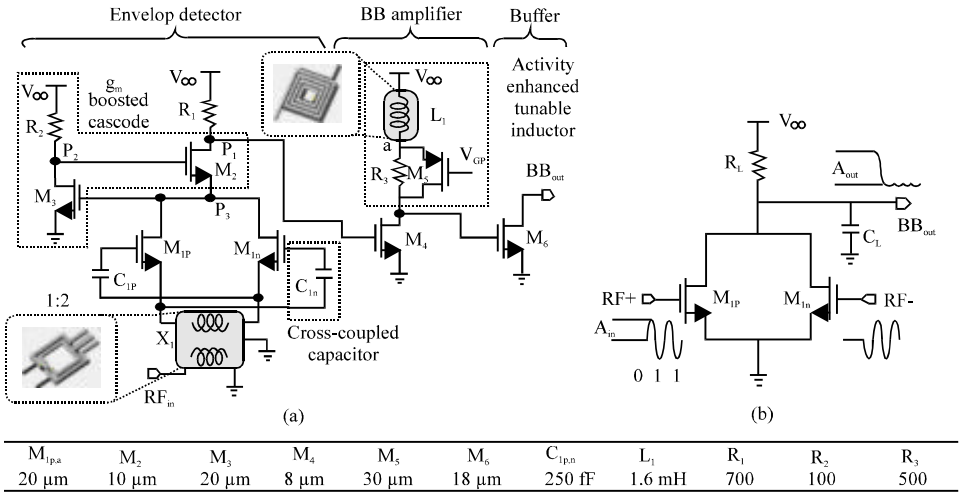
- Low power consumption for long distance on-chip communication
- Wireless networks are compatible with CMOS fabrication technologies
- Can adopt existed network architectures
- Easy to design and build compared to photonic connections

Wireless network on chip: Over the last five years, many research study suggested techniques to improve the WiNOC. The goal of all of these efforts is to introduce network modules that are efficient to use in the current commercial parallel computing systems. This study is trying to answer the second question that is raised in research motivation part. What are the latest state of the art contributions? Several techniques have been suggested each with different level such as:

- Circuit level
- Transceiver level
- Architecture level
- Application level

This study introduces the research that has been suggested at each of these levels.

Circuit level: Different hardware components are used in the WiNoC including transceivers, routers or antennas. These components form most of the costs of the WiNoC in terms of area and power consumption. Designing these components specifically for the WiNoC could improve these metrics. Different novel and circuit level components designs have been proposed. By Yu *et al.* (2015) proposed circuit level On Off Keying (OOK) demodulator. OOK has low complexity architecture compared to other modulators. It is also considered on the top of the most energy efficient modulation circuits when it is used for communication of distance of order of millimeters. It is already discussed that most of the WiNoC designs require specific performance metrics such as small area overhead, low power consumption of about 1 pJ per bit and high bandwidth. In order to achieve such requirements, Yu and his team pro-posed an OOK demodulator with a novel differential envelop detector ED topology that has dual gain-boosting techniques. In addition, it is equipped with a single-stage Base Band (BB) peaking amplifier. This amplifier is provided with Actively-Enhanced Tunable Inductor (AETI) load which is used to extend the RX bandwidth. Figure 3a shows the proposed OOK circuit schematic. The proposed OOK is fabricated using a 1P9M 65-nm CMOS technology. The area of the overall system is 0:25 with the external pads while the active area is about 0:043. The measurements of the on-wafer tests are taken using cascade summit-11000 probe station. An Agilent PNAX network analyzer is used for S-parameter measurement up to 67 GHz.



$M_{1P,n}$	M_2	M_3	M_4	M_5	M_6	$C_{1P,n}$	L_1	R_1	R_2	R_3
20 µm	10 µm	20 µm	8 µm	30 µm	18 µm	250 fF	1.6 mH	700	100	500

Fig. 3: a) Schematic of the proposed On Off Keying (OOK) demodulator. The sizes of the component of the design are listed in the figure. These sizes are based on the 60 nm technology and b) Schematic of conventional differential envelop detector (Yu *et al*., 2015)

The PNAX is used to generate the 60 GHz carrier signal. The BB data is analyzed by an Agilent N4960A Bit-Error-Rate Tester (BERT). A Tektronix DSA8300 sampling oscilloscope is used for the evaluation of the demodulated BB output from the OOK demodulator. Results show that the peak data rate of the proposed modulator is 18.7 Gb/sec. This speed comes at low power cost bit-energy efficiency of 0.25 pJ/bit. This means that the overall power consumed was 4.6 mW that is taken from a 1-V supply. The researcher claimed that this OOK demodulator has a high data rate and very low power consumption compared to the state of the art modulators. Research has been conducted to improve the antennas used in WiNoC. Almost all of the WiNoC architectures use millimeter-wave omeni antennas that use token passing protocol to control access to the shared wireless medium. This protocol allows only one point to point communication at a time which limit the performance of the network. In this scheme a number of non-overlapping channels are required in the same chip to cover the demand of data transfer in the mullti-core chip which requires complex filters in the transceivers. This solution is costly in terms of power and area. Mondal *et al*. (2017) have proposed directional antennas that allows multiple wireless interconnect pares to communicate simultaneously to improve performance and energy-efficiency. To avoid interference, the Wireless Interface (Wis) are placed according to an algorithm that is designed for this specific purpose. This algorithm is alos responsible for the routing operations for network. The architecture uses directional Planar Log-Periodic Antennas (PLPAs). The proposed Directional Wireless Network-On-Chip (DwiNoC) architecture is shown in Fig. 4. It is built based on small

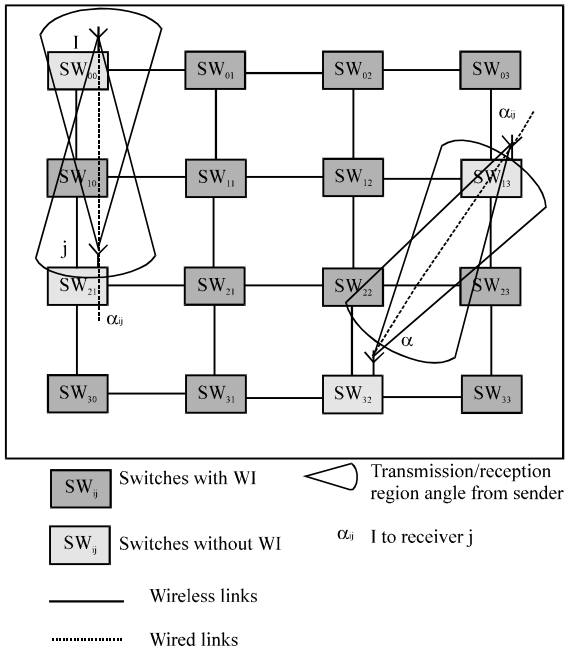


Fig. 4: The proposed directional wireless network-on-chip (DwiNoC) architecture. It is built based on small-world network topology (Mondal *et al*., 2017)

world network topology. In this topology wire links are used between nodes in sub networks while the directed wireless links are used to connect between the sub networks. The proposed DWiNoC architecture is tested using cycle accurate simulator. It is used to models the progress of the data flits accurately over each clock cycle. HFSS tool is used to produce results of the PLPA

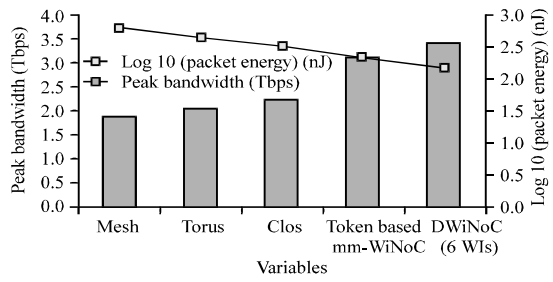


Fig. 5: Maximum obtained bandwidth and power consumed per transmitted packed of the proposed NoC architecture and several other NoC architectures. All of these networks have the same system size of 64-core (Mondal *et al*., 2017)

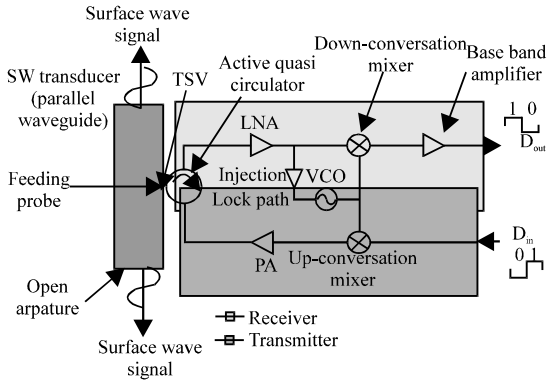


Fig. 6: Block diagram of the proposed transceiver (Agyeman *et al*., 2015)

antenna. These characteristics are used to produce an accurate model of the energy consumption, bandwidth and reliability for the network.

Two system sizes of 64 and 256 cores are considered in the experiments. Results showed that the proposed DWiNoC overcomes other conventional NOC in terms of peak band-width and power consumption. Figure 5 shows simulation results of energy dissipation and peak bandwidth of a 64 core system. This system is tested using uniform random traffic distribution. The figure also compare different other NoC architectures such as mesh touros, Clos and mm-Wave WiNoC. It is clear from the figure that the proposed research has gain over all other networks.

Transceiver level: In addition to the circuit level, efforts have been paid to improve the transceivers and transducers used in the WiNoC. Transceivers represent important components of any wire-less networks. They come with high cost of area and power consumption. For this reason, several research groups have been working on improving the transceivers in WiNoC. Agyeman *et al*. (2015) proposed a novel transducer design to generate wireless signals with high signal strength. This research is focusing on reducing error rate of the WiNoC to the point where it is competitive with the conventional NoC. Conventional wire network have extremely low Bit Error Rate (BER). It is estimated to be of around 10-14 while the error rate of millimeter-wave is of around 10-7 as it is estimated by the research presented in this paragraph.

Losing one message in multi-core systems could lead to high effects on the performance of the whole system. For this reason, this research group is trying to improve the BER of the WiNoC by proposing a WiNoC fabric with a novel transceiver. This device is used to launch surface wave signals into a commercially available thin metal conductor. This material is coated with a low cost dielectric material. For a reliable transmission, the proposed transceiver should have a low power consumption circuit with a wide bandwidth and high data throughput. The proposed transceiver is shown in Fig. 6. It is an update of low-power non-coherent On-Off Keying (OOK) modulator. An up-conversion mixer and a Power Amplifier (PA) are embedded in the transmitter. In the other side, the receiver is equipped with a Low Noise Amplifier (LNA), a baseband amplifier and a down conversion mixer. A single injection-lock Voltage Controlled Oscillator (VCO) is used for both the receiver and transmitter to reduce the area and power consumption of the proposed design. The proposed research is tested using cycle-accurate experiments. An extended version of Noxim simulator which is an open source system simulator is used to perform the experiments. Results showed that the proposed transducer has a very high band width range of 45-60 GHz. The tested device is also found to have high efficiency in terms of average packet delay and power consumption compared to other mm-wave WiNoCs.

Architecture level: A number of research groups have suggested architecture level improvements to increase the efficiency of the WiNOC. Most of these improvements focus on reducing latency and power consumption while keeping an eye on the area of the architecture. The wireless transceivers and the associated antenna imply power and area overhead. Therefore, the number wireless links that can be used within the multi-core system on chip is limited. Rezaei *et al*. (2014) proposed a hierarchical WiNoC. They called it hierarchical wireless-based architecture and for short they gave it the acronym HiWA. In the HiWA, the network is divided into groups of smaller networks, subnets. The communications within the subnets are carried over wire links. A single-hop wireless connection

Table 1: Latency results of the proposed algorithm. The numbers in this table are normalized to the dama results to ease comparison (Rezaei *et al*., 2015)

Variables	NN (Mondal *et al*., 2017)	BN (Agyeman *et al*., 2015)	INC (Rezaei *et al*., 2014)	DAMA
AWD	1.25	1.30	1.42	1.00
AWMD	1.29	1.32	1.36	1.00
NMRD	1.24	1.62	1.21	1.00
ICR	1.52	1.21	2.01	1.00

channel is used for communication between the nodes. This means that both wired and wireless links are used in this hybrid network.The proposed HiWA is based on a 2D mesh that is divided into square subnets. Each subnet is connected to a center baseline router. The router in each subnet is replaced with wireless routers that communicate with the neighbour subnets. Two different size HiWA: 225 and 256 are built. Figure 7 shows the 256 56 nodes HiWA. The nodes without color are baseline connection nodes while the green nodes are wireless and red presents the borders of each block. The wireless routers placement is designed in such a way to decrease the number of the wireless routers that that are required to perform the inter-subnets communication. The goal of this step is to improve the performance of the network and energy efficiency. An algorithm is custom designed for this purpose. In addition to the router placement, several other aspects of the architecture have been considered. An addressing method is used for routing packets between the nodes. The system is managed using a routing algorithm that also take in account avoiding deadlock in the routing the packet around the network.

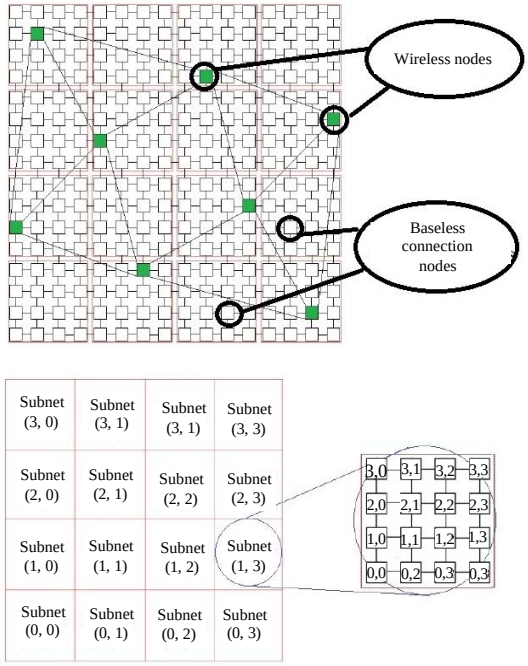


Fig. 7: Hierarchical Wireless Network Architecture HiWA; a) 256 nodes HiWA (The white nodes are baseline connection nodes while the green nodes are wireless and red presents the borders of each block) and b) Physical structure of the 256 nodes HiWA along with its addressing method (Rezaei *et al*., 2014)

Application level: The contributions in these levels try to design the code in such a way that is efficient to be implemented on systems that utilizes WiNOC. In multi-core systems, applications will enter and leave as sets of communicating tasks at run time might. In some of these cases the overall system might face a highly dynamic research load. The tasks load is controlled by the map-ping of the system manager. It is the manager's responsibility to allocate application's tasks onto the system in a way that efficiently utilize the system resources. Rezaei *et al*. (2015) proposed a Dynamic application Mapping Algorithm (DMA) for WiNOC systems. The goal of this research is to reduce both internal and external congestion. Congestion has a negative impact on the network performance which dramatically affects on the delay of the system. Without an efficient mapping mechanism, the wireless routers will be heavily used very. The proposed algorithm has been implemented on the HiWA that is already presented in this study (Rezaei *et al*., 2014). The tests included different scenarios with several applications. The number of tasks within the applications varied from 4-35 tasks. Task graph generator tool is used to generate the tasks. The tests are performed on an open source simulator (XMulator). Several metrics have been used in evaluating the algorithm such as Average Manhattan Distance (AMD), Average Weighted Manhattan Distance, Mapped Region Dispersion (MRD), Nor-malized Mapped Region Dispersion (NMRD) and Internal Congestion Ratio (ICR). Table 1 shows comparison results of the latency of the proposed algorithm against other algorithms. It can be seen that the DAMA is more efficient than the NN algorithm by 25% in average of all evaluation tests. It has also shown that DAMA has 40 and 20% improvements compared to the BN algorithm at reducing congestion. In the same time, DAMA has 50 and 15% gain over the INC in internal and external congestion, respectively.

RESULTS AND DISCUSSION

This study discusses the results obtained in from all the research presented in the previous study. Several challenges are facing using the NiWoC in commercial application. It is important keep in mind that the technologies utilized for electrical wire NoC are much more optimized compared to the technologies used with the nanophotonic or WiNoC devices (Abadal *et al*., 2015). The technologies used in WiNOC are still in their infancy. They could be improved in the following years. The fourth question raised at the beginning of this paper answered here. The challenges and improvement aspects of the WiNoC can be grouped into levels.

Circuit level: Most of the circuits presented for the WiNoC are merely updated versions of the circuits used in traditional networks. Novel and optimized circuit topologies that are designed specifically for WiNoC could lead to a important improvements in reducing the area and power consumption. The underlying technology limits the performance of the wireless transceiver that is proposed so far in the literature. The raises the question about the compatibility between the proposed circuits and the CMOS technologies used for the multi-core systems.

Transceiver level: Transceivers and transducers are important components of the WiNOC. They consume much of the power of the network and require large area of the chip. For this reason, a transceiver design that tries to trade-offs between transceiver energy consumption, radiated power in one side and received power in the over side is highly recommended to improve energy efficiency.

Architecture level: Several architectures have been adopted for WiNoC. Most of them are based on the traditional network typologies such as 2D mesh torus and tree. These typologies might look good fits for the WiNoC at the schematic level. However, high schematic level does not necessarily reflect the actual substrates fabrication level. It is vital to keep in mind this fact while designing such architectures.

Application level: To the best of my knowledge almost all the research that has been presented, so, far lacks testing mechanisms at the application levels. The designs proposed in the field are tested on simulation software under hypothetical scenarios and with randomly generated data. A standard application level bench mark is required for evaluation and comparison with other research.

CONCLUSION

Parallel processing has been heavily used for divers of application including weather forecast, data mining and machine indulgent. The multi-core system on chip is one of the highly growing era of parallel processing. Such systems contains number of processing units that collaborates to process large amount of data concurrently which acquires data transfer between these processing units. Wireless network on chip has been presented as a solution for the demand high traffic communication in the multi-core system on chip. It is used for its promising characteristics such as high bandwidth, small area and low power consumption. However, WiNoCs are still evolving to reduce their complicity and overcome the performance of the conventional wire NoC. This research is trying to study the improvements that have been made to the designs of the WiNoC in the past half decade. A number of research study that have important contribution in this field has been presented. The focus of these contribution varied on different levels between circuit and technology level up the application level. At the end of this research the challenges that are facing the improvement of WiNoC are discussed along with some points for future improvements.

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