Journal of Engineering and Applied Sciences 13 (1): 58-63, 2018
ISSN: 1816-949X

2D Symmetric16×8 SRAM with Reset

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Abstract: SRAM is one of the basic element used in memory. Large memories are needed as more amount of information to store in today's life. The on-chip memory is increasing for every generations of processors and systems. In VLSI design metrics are area, cost, portability, speed and power. To meet specification many topologies are existing for basic SRAM cell design. In this study basic 6T SRAM is considered for which additional transistors are added to reset the memory using reset pin. The back to back inverter circuit of SRAM is driven on both sides. For this circuit two additional transistors are added to enable based on row-sel and coln-sel inputs. To increase the speed of operation of the circuit additional circuit gate level body biasing circuit. This modified basic SRAM cell is used to design for 16×1 SRAM memory later extended for 16×8 memory. The circuit is designed with GPDK45 and simulated by cadence spectre simulator.

Key words: SRAM, body biasing, multi bit SRAM, portability, transistors, specification

INTRODUCTION

Memories play significant role in daily life for storing more information. The information can be data, images or videos. For the memories with less access time are preferred, thus increased the research for high speed memory elements. There are different memory elements like SRAMs (Yadav *et al*., 2013) and DRAMs. As the refreshing cycles (Bortolotti *et al*., 2014) are not needed for SRAMs, its significance increased compared to DRAM cells. Because of this reason various SRAM structures like 6T, 8T, 9T, 10T and 12T are designed. These circuits have designed for achieving design metrics like power area and speed. The 6T, 7T and 8T SRAM provides good read stability with less noise margin (Sah *et al*., 2015) whereas 9T SRAMs provides more write stability (Athe and Dasgupta, 2009). From Calhoun *et al*. (2010), it is marked that the power consumption is varied with width of the transistors.

Biasing circuits: In circuit of SRAM design maintain of power and delay are very important. The SRAM topologies are selected depending on the application in which it is used. Apart from SRAM topologies use of different biasing adds stability to the circuit output. To boost the performance of low power designs the body biasing methods can be used, it also progresses strength against process and temperature variations.

PMOS-VDD and NMOS-GND biasing: The basic technique for biasing any circuit is simply connecting the bulk of PMOS to VDD and NMOS bulk to ground (Mann *et al*., 2010). This differs the threshold voltage of the transistors which rises the performance. This technique increases both static and dynamic leakage powers.

Dynamic biasing: To reduce the leakage power as above biasing method (Kim and Roy, 2002; Kirolos and Massoud, 2007) Dynamic Threshold (DTMOS) is ideal. DTMOS provides low leakage current, high current drive at low voltages. But DTMOS surges miller capacitance, body resistance and bounds the power supply below 0.7 V.

Body biasing by GLBB: In this study, the biasing technique is gate level body biasing (Taco *et al*., 2016). In GLBB the output of the circuit is fed to additional circuit which produces body biasing voltage V_B. This V_B is applied as common biasing voltage for allthePMOS and NMOS substrates. This method the supply voltage vdd controls the threshold voltage as the output directly depends on it. As per (Taco *et al*., 2015) the substrates of PMOS and NMOS are supplied with VDD and GND, respectively. The drains of PMOS and NMOS are connected to GND and VDD, respectively. The biasing voltage is generated at source-source connection of the

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both the transistors. This technique increases two transistor count intern increases area, power and cost. However, this increases the speed of the circuit.

MATERIALS AND METHODS

Sram implementaion: The basic 6T SRAM cell consists of inverter driven inverter circuit with write control. For the basic circuit two additional transistors are added with active low reset input (rst-l) (Basha *et al*., 2016). When rst-l = 0 PMOS transistor is on and ground (0) value is wrote into SRAM cell. When rst-l = 1, NMOS is on and the data in input is wrote into the SRAM cell. To pass the data in into SRAM cell three pass transistors are added which are controlled by write, row-sel, coln-sel inputs. The output is read from the memory when read = 1. The inverter driven inverter circuit is driven from the both sides with symmetric circuit. The modified 6T SRAM cell is shown in Fig. 1.

Figure 2 shows the GLBB circuit added for the circuit shown in Fig. 1. Here, the output signal is added to gate terminals of the additional circuit (Basha *et al*., 2016).

The source-source output is taken for generating the biasing voltage V_B. This voltage is applied to all the transistors substrate circuit.

Two decoders are used in the circuit shown in Fig. 3. One decoder is driven with A3, A2 address lines to generate row selector signal and the second decoder is driven with A1, A0 address lines to generate column selector. The output line of the basic element are tied together to generate Dout signal. For designing 16×1 memory the modified circuit shown in Fig. 1 and 2 are

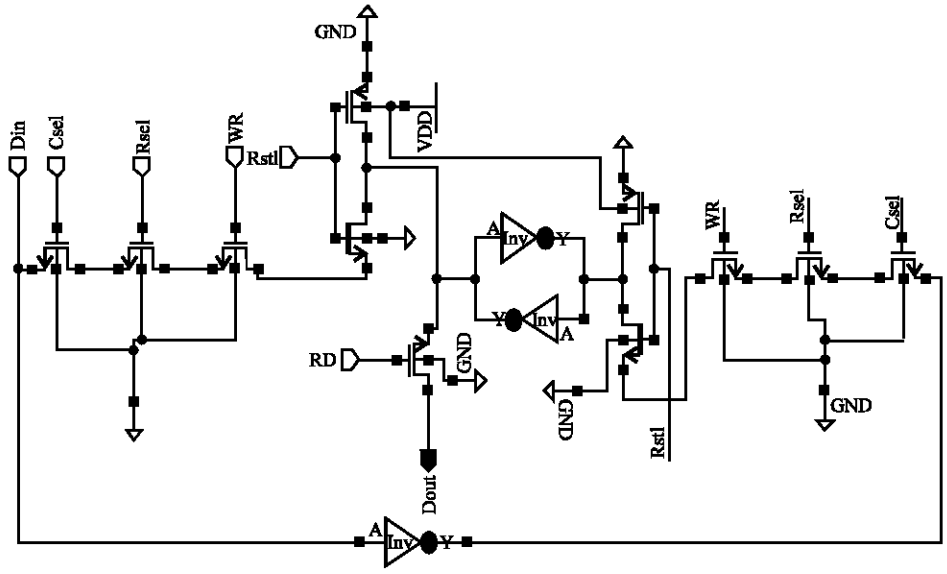

Fig. 1: Modified basic SRAM cell with reset

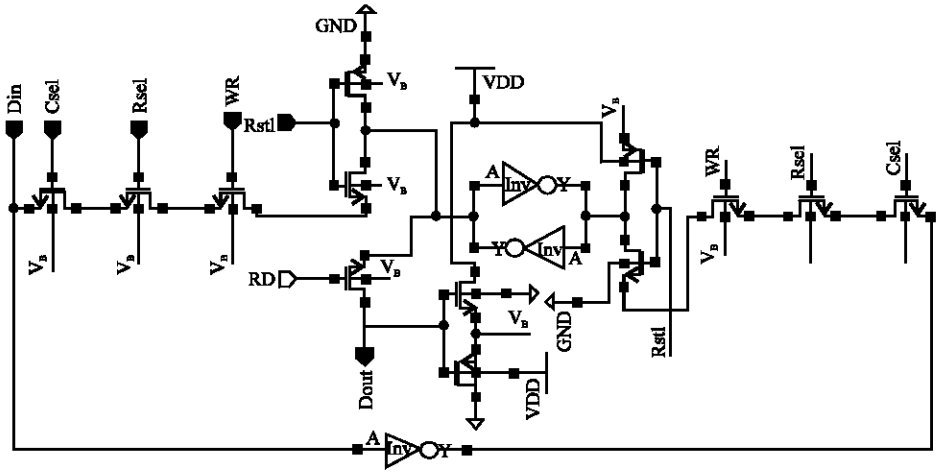

Fig. 2: Biased modified SRAM cell with reset

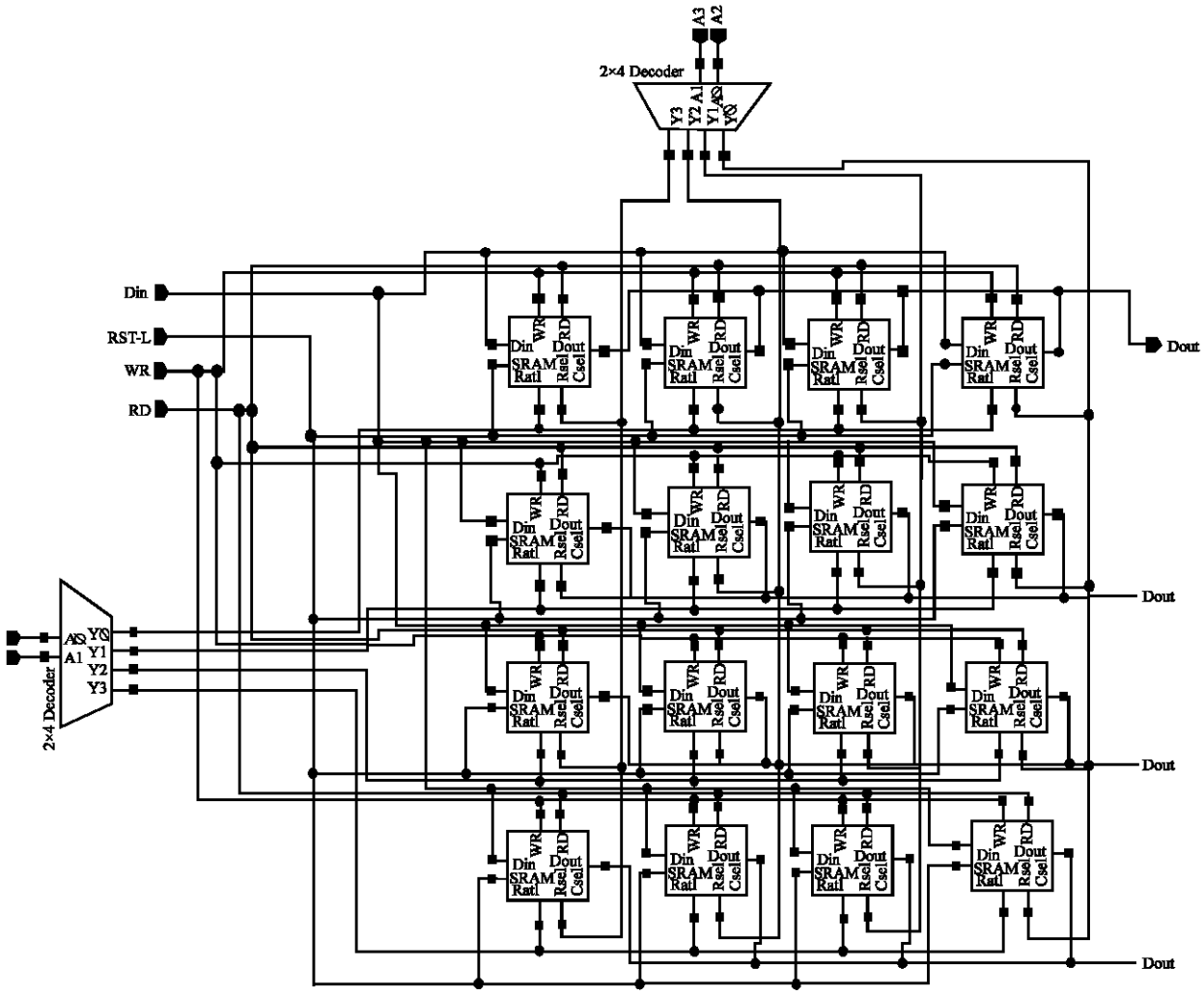

Fig. 3: The 16×1 SRAM memory

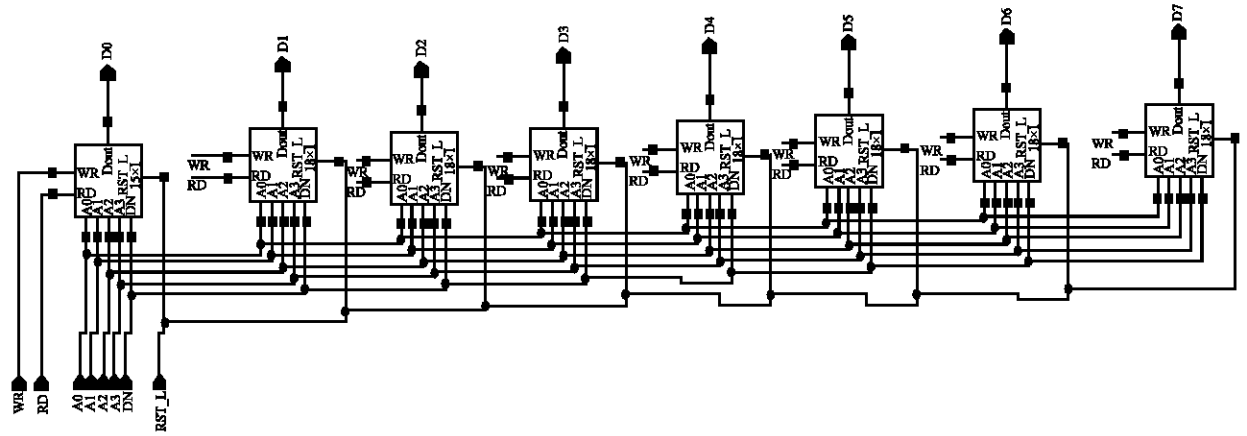

Fig. 4: The 16×8 SRAM memory

used and tested separately to check the effect of biasing circuit and the results are discussion later. Figure 4 shows the 16×8 memory. In this 8 block of Fig. 3 are cascaded to design 16×8 memory. Except data input and output lines are different and remaining signals are common for all the blocks.

RESULTS AND DISCUSSION

The 45 nm technology 2D 16×8 SRAM is designed using GPDK45. The circuit is designed using Cadence Virtuoso tool schematic editor. The designed circuit is simulated spectre tool. The circuit is verified for different combinations test vectors for input signals and the circuit is verified for functionality. The circuit is analyzed for speed and power at various temperatures for both the cases without and with biasing.

Figure 5 shows the simulation results of modified basic 6T SRAM cell for different combination of input signals. The simulation results are same for both without and with biasing circuits.

Figure 6 shows the simulation results of 16×1 SRAM cell. Figure 7 shows the simulation results of 16×8 memory. Here, the circuit is tested for random pattern for addressing line and tested by writing and followed by read operation.

The circuit is simulated at different temperatures. It shows the power is varied with respect to temperature and delay is insensitive to temperature. It is noticed that as the temperature is increased the power is decreased.

Table 1 lists the power and delay at different temperatures. Table 2 shows the comparative analysis for 16x1 memory block of Fig. 3 in terms of power and delay values.

Table 4 shows the average power of SRAM cell and 16×1 memory by changing the transistor with different configuration like normal, fast-fast, slow-slow, fast-slow, slow-fast and static. In this notation the configuration for

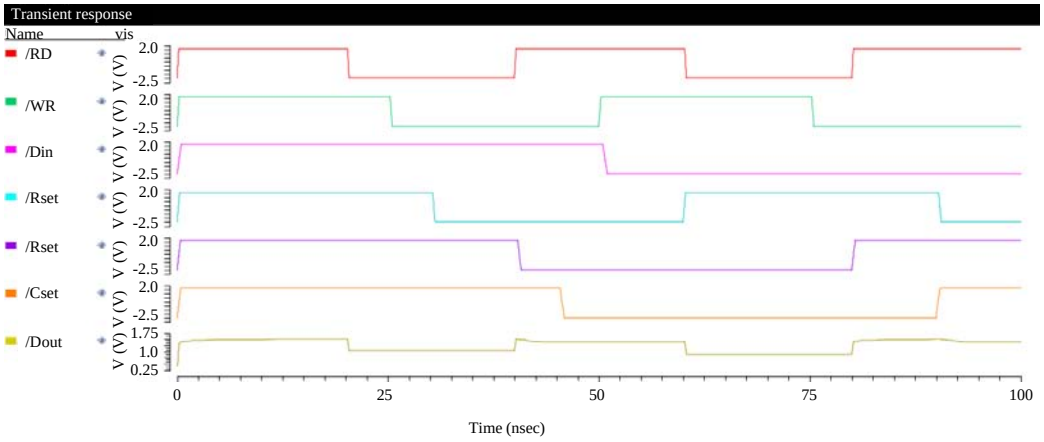

Fig. 5: Basic SRAM simulation results

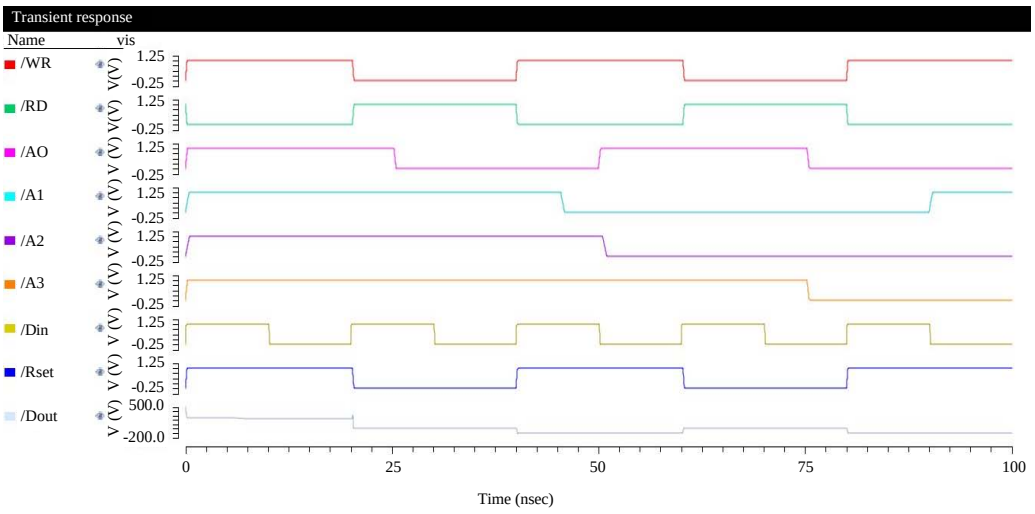

Fig. 6: The 16×1 SRAM simulation results

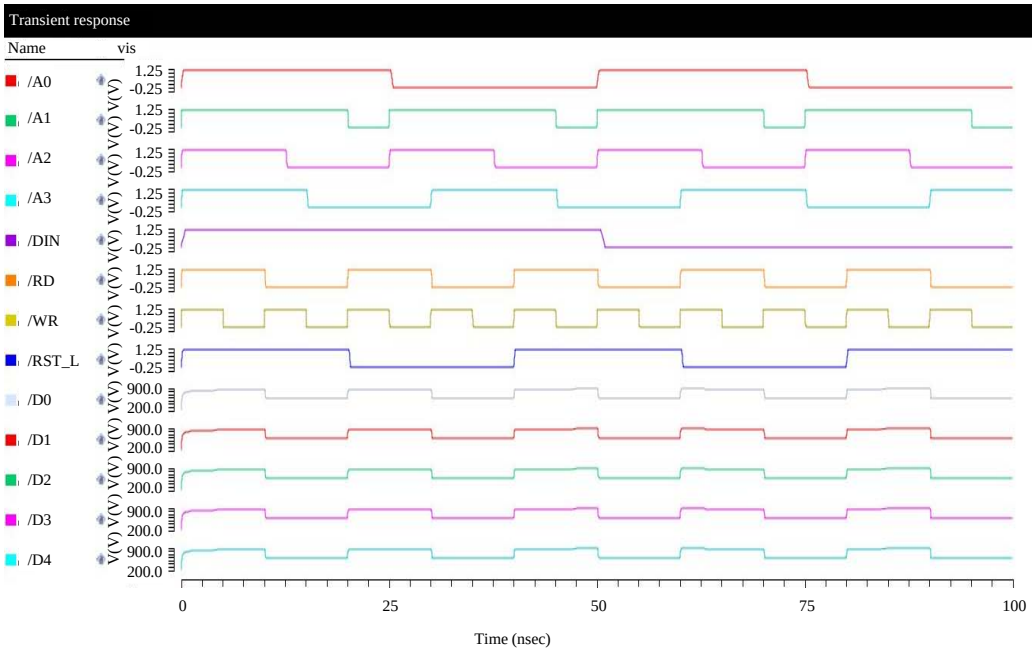

Fig. 7: The 16×8 SRAM simulation results

Table 1: Modified basic SRAM analysis

Temparature (°C)	Power (uW)	Delay (nS)
25	10.54	15
27	10.48	15
29	10.42	15
31	10.36	15

Table 2: The 16×1 SRAM analysis

Temp.	Power (uW)		Delay (nS)	
(°C)	Without biasing	With biasing	Without biasing	With biasing
25	74.44	108.0	137	70
27	74.19	107.4	137	70
29	73.94	106.8	137	70
31	73.70	106.2	137	70

Table 3: The 16×8 SRAM analysis

Transistor types	SRAM cell	16×1 SRAM
MC (normal)	10.480	107.4
FF	14.070	144.4
SS	7.230	75.02
FS	9.322	87.28
SF	11.440	125.1
TT (static)	10.480	107.4

Table 4: Power comparison

Temp.	Power (uW)		Delay (nS)	
(°C)	Without biasing	With biasing	Without biasing	With biasing
25	324.3	858	319	168
27	323.2	853.3	319	168
29	322.2	848.7	319	168
31	321.2	844.2	319	168

PMOS-NMOS transistors. The input frequency and output frequencies are shown in Table 5 here frequency in MHz.

Table 5: Input and output frequency

Circuit	Din frequency	Dout frequency
SRAM	16.67	6.667
16×1	50.00	25.000

CONCLUSION

This study designed and simulated for 16×8 SRAM memory block. The designed starts with basic 6T SRAM cell with modifications for reset (active low) operation. Then the circuit is added with additional circuit for biasing voltage. After verifying the circuit for functionality 16×1 SRAM memory cell is designed and extended for 16×8 size. All the circuits designed are simulated and analyzed for both without and with biasing voltage. Later the circuits are simulated to analyze the temperature effect on power and speed. Further, SRAM cell and 16×1 memory cells are simulated by changing the configuration of PMOS and NMOS transistors. Here, it is noticed the increased in power when the circuit is biased with common bias voltage with increase in speed. The power can be lowered by applying low power technology in future.

REFERENCES

Athe, P. and S. Dasgupta, 2009. A comparative study of 6T, 8T and 9T decanano SRAM cell. Proceedings of the IEEE Symposium on Industrial Electronics and Applications, October 4-6, 2009, Kuala Lumpur, Malaysia, pp: 889-894.

Basha, D. K., M. Rajanikanth, A.P. Reddy and V.S. Rao, 2016. 2D symmetric 6T SRAM with reset. Proceedings of the IEEE International Conference on Recent Trends in Electronics, Information and Communication Technology (RTEICT), May 20-21, 2016, IEEE, Bangalore, India, ISBN:978-1-5090-0774-5, pp: 348-352.

Bortolotti, D., H. Mamaghanian, A. Bartolini, M. Ashouei and J. Stuijt *et al.*, 2014. Approximate compressed sensing: ultra-low power biosignal processing via aggressive voltage scaling on a hybrid memory multi-core processor. Proceedings of the 2014 International Symposium on Low Power Electronics and Design, August 11-13, 2014, ACM, La Jolla, California, USA., ISBN: 978-1-4503-2975-0, pp: 45-50.

Calhoun, B.H., J.F. Ryan, S. Khanna, M. Putic and J. Lach, 2010. Flexible circuits and architectures for ultralow power. Proc. IEEE., 98: 267-282.

Kim, C.H. and K. Roy, 2002. Dynamic Vt SRAM: A leakage tolerant cache memory for low voltage microprocessors. Proceedings of the International Symposium on Presented Low Power Electronics and Design, August 12-14, 2002, Purdue University, West Lafayette, Indiana, pp: 1-4.

Kirolos, S. and Y. Massoud, 2007. Adaptive SRAM design for dynamic voltage scaling VLSI systems. Proceedings of the 50th Midwest Symposium on Circuits and Systems MWSCAS, August 5-8, 2007, IEEE, Montreal, Quebec, Canada, ISBN: 978-1-4244-1175-7, pp: 1297-1300.

Mann, R.W., S. Nalam, J. Wang and B.H. Calhoun, 2010. Limits of bias based assist methods in nano-scale 6T SRAM. Proceedings of the 2010 11th International Symposium on Quality Electronic Design (ISQED), March 22-24, 2010, IEEE, San Jose, California, USA., ISBN:978-1-4244-6456-2, pp: 1-8.

Sah, R.K., I. Hussain and M. Kumar, 2015. Performance analysis of a 6T SRAM cell in 180nm CMOS technology. IOSR. J. VLSI. Signal Process. IOSR-JVSP., 5: 20-22.

Taco, R., I. Levi, M. Lanuzza and A. Fish, 2016. Low voltage logic circuits exploiting gate level dynamic body biasing in 28nm UTBB FD-SOI. Solid State Electron., 117: 185-192.

Taco, R., M. Lanuzza and D. Albano, 2015. Ultra-low-voltage self-body biasing scheme and its application to basic arithmetic circuits. VLSI Des., 2015: 1-10.

Yadav, S., N. Malik, A. Gupta and S. Rajput, 2013. Low power SRAM design with reduced read/write time. Intl. J. Inf. Comput. Technol., 3: 195-200.