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Effect of Threshold Roll-Off on Static Noise Margin of Sram Cell

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Abstract: The threshold roll-off is a vital phenomena to be considered for any low-power and small-scale circuit design. With the advancement of the fabrication processes the channel length of the transistors is reducing rapidly, this reduction in the channel length affects the threshold voltage of the transistors very severely. To evaluate the effect of channel reduction on the threshold voltage this study analyzes the threshold roll-off by taking SRAM cell into consideration. The reason behind choosing SRAM cell is that now the IC's are fabricated using System on Chip (SOC) design technique and currently approximately 70-80% of the SOC area are covered by memories only. One of the most important figure of merit for SRAM cell is its Static Noise Margin (SNM) and hence, the effect of threshold-roll is implemented with respect to SNM of the SRAM cell.

Key words: Threshold roll-off, sub-threshold current, SRAM cell, System on Chip (SOC), Static Noise Margin (SNM), phenomena, transistors

INTRODUCTION

In the current digital integrated circuit designing a complete system is being implemented on the chip which is formally known as System on Chip (SOC). Nowaday, the designed SOCs usually contain memory in its larger part of the area (roughly 70-80% of its total area), Hence, it is very crucial to take the memory part in a very effective way as the memory cells are very compact compared to other logic parts present in the chip. The care should be taken in such a manner that even if a single cell is defective then it must be identified otherwise it may affect the adjacent cell and may damage the functionality of the whole memory component (Zhang *et al*., 2010; Shih *et al*., 2005; Lundstrom, 2003; Chang *et al*., 2003; Ito *et al*., 2003; Zhao and Cao, 2006; Ishii *et al*., 1998; Shee *et al*., 2014; Austin *et al*., 1998).

However, as the fabrication process of the integrated circuits are advancing quickly, it affects the size of the transistors or other components present in that chip. Presently many vendors are working on <20 nm process technology which directly has impact on the size of transistors short channel length is one of the impacts of this scaling. Due to continuous scaling of the various parameters the threshold roll-off comes in the design issue and this issue may affect the behavior of the component or the entire system very badly.

An SRAM cell is taken in this case to analyze the effect of threshold roll-off on its static noise margin as the SNM of the SRAM cell is very crucial design issue for the cell stability and how effectively an SRAM cell can read and/or write is determined by its SNM analysis only. If the SNM of the cell is not properly optimized it may degrade overall functionality of the entire memory of the IC.

MATERALS AND METHODS

Threshold roll-off: According to the classical theory of the transistors in the channel region for depletion charges the gate voltage has to be compensated before making the channel to go into strong inversion. This gate voltage is responsible for the constitution of the threshold voltage given in Eq. 1:

$$V_T = V_{FB} + 2\varphi_F + \frac{\sqrt{2\varepsilon_0\varepsilon_{si}\, qNA}}{C_{ox}}\sqrt{2\varphi F} \quad (1)$$

Where:
VFB = The Flat Band Voltage
NA = Accepter concentration
φ = F Fermi level

However, a very small amount of the depletion charges caused by the source and drain junction present near the source and drain region, this in turn increases the leakage current. For long channel transistors, this effect is negligible while comparing to the overall depletion

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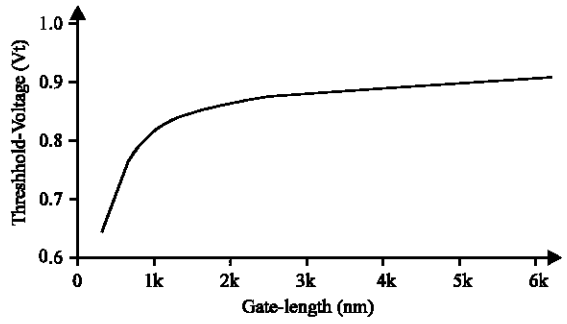

Fig. 1: Threshold roll-off w.r.t gate length

Table 1: Geometric parameters

Gate length (nm)	16 nm	22 nm	32 nm	45 nm
Dielectric thickness	1.2e-9	1.4e-9	1.6e-9	1.8e-9
Junction depth	5e-9 7	2 e-9	5e-8	1.4e-8
Channel depletion thickness	5e-9	7.2 e-9	5e-8	1.4e-8

Table 2: Parameters

Gate length (nm)	16 nm	22 nm	32 nm	45 nm
EI	1.00055	1.04	1.0061	1.0000154
VT-roll	1.886 φD	1.963 φD	1.899 φD	1.888 φD

charges. This effect comes into the design where transistor channel length or gate length is short as shown in Fig.1.

The other factors which affect the threshold roll-off include gate-oxide thickness, channel-depletion depth and junction-depth as the length of the channel becomes shorter. By optimizing inner junction and depletion depth, the threshold roll-off may be controlled till a certain extent. Another most critical effect is charge sharing in short channel transistors. Empirically, the Threshold roll-off approximately calculated is given by Eq. 2:

$$V_T = 0.64(\varepsilon_{si}/\varepsilon_{ox})(\varphi_D)(EI) \quad (2)$$

where, φ_D D is source to channel junction built in voltage and EI is known as electrostatic integrity of the device and calculated using:

$$EI = 1+\frac{xj^2}{L^2}.\frac{t_{ox}}{L}.\frac{T_{dept}}{L} \quad (3)$$

where, T_{depl} is the depletion depth in the channel. Hence, from above equation, we can conclude that by reducing the value of EI in the device structure the threshold roll-off voltage can be reduced. The modeling for transistors is related to its device geometric parameters as shown in Table 1.

The calculated values of EI and VT-roll are shown in Table 2. From this expression, it is also clear that the threshold roll-off depend largely on source to channel

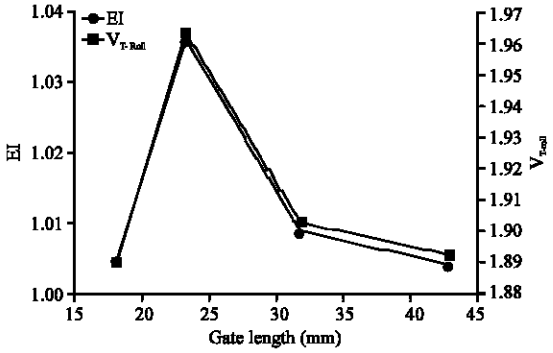

Fig. 2: Variation of $V_{T\text{-}Roll}$ and El w.r.t gate length

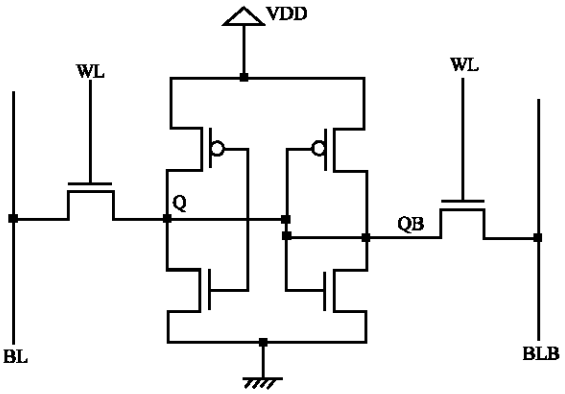

Fig. 3: Basic single port SRAM cell

built-in voltage (φ D) rather than electrostatic integrity only (if EI is somehow maintained nearly equal to 1 as it is always desired).

The source to channel built-in voltage (φ D) can be calculated using in Eq. 4 and by varying the involved parameters the VT-Roll can be controlled as per the requirements:

$$\varphi_D = V_{tm} * \ln(SD*N_D/n_i^2) \quad (4)$$

Where:

SD = Substrate Doping

N_D = Donor density

n_i = Intrinsic carrier concentration

The final graph is plotted between gate length, EI and $V_{T\text{-}Roll}$ as shown in Fig. 2. By observing the obtained graph it can be concluded that the variation is almost constant w.r.t. EI as well as φ D. Hence, the $V_{T\text{-}Roll}$ is not only dependent on EI but also it depends on the value of φ D and by controlling the value of it the $V_{T\text{-}Roll}$ can also be controlled.

Sram cell: The basic single port SRAM cell is shown in Fig. 3. It consists of two inverters connected back to back

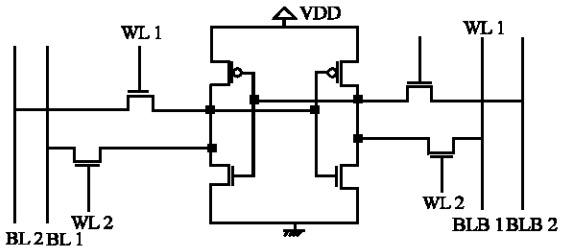

Fig. 4: Double port SRAM cell

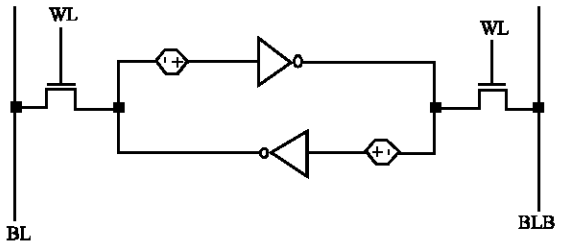

Fig. 5: Arrangements of SRAM cell for measuring its SNM

and this connection is responsible for the reinforcing the cell and make it suitable for data retention. The Bit-Lines (BL and BLB) are used for reading and writing the data from the memory while the Word Line (WL) is used for selecting the particular cell of the memory.

The above cell is just a single read/write cell, however now most of the memories contain double or dual port read/write cell as shown in Fig. 4. Double port SRAM cell increases the memory density to a higher extent.

The two ports present in the given cell is able to access the cell independent to each other but to achieve this the bit lines (also known as access lines) and word lines should be duplicated. In the above cell, two extra pass transistors are required to control the access of the second port (Inaba *et al*., 2002; Khakifirooz and Antoniadis 2006; Abd-Elhamid *et al*., 2006; Pavlov and Sachdev, 2008; Farkhani *et al*., 2014) (Table 3).

Static noise margin: For SRAM cell, its SNM is a key figure of merit. The SNM can be calculated by drawing a largest possible square in between the two Voltage Transfer Characteristics (VTC) of the back to back connected inverters the configuration can be shown in Fig. 5.

Where the voltage source is given as noise voltage source. The side length of the square which is usually given in volts represents the SNM of the cell. When the given noise voltage is increased and becomes more than SNM, the state of the SRAM cell may alter and the data may lost which is not a desired result. Furthermore, since

Table 3: Parameters

Device name	Mos size W/L (nm)
PMOS	200/70
NMOS	66/22
Supply voltages (V)	
V_{DD}	3.8
Word Line (WL)	1.6
Bit Line (BL)	1.6

the cell perform both read as well as write operation of the data the SNM also characterized as read as well as write margin. In the case of read margin the SNM is calculated when the word line voltage is set high and the bit lines are also recharged to its high value on the other hand the write SNM is defined as the minimum bit-line voltage required to change the stored data of the cell.

RESULTS AND DISCUSSION

The above single and double port SRAM cell is simulated using HSPICE simulator and their threshold roll-off is maintained by varying the device parameters as shown in Eq. 2 and 3. The noise margin simulation is also performed to measure the effective SNM of both the cell with respect to the optimized threshold roll-off. The standard 22 nm process technology is used for the modeling of transistors. The various other major parameters are noted in Table 3.

Figure 6a shows the value of supply voltage is given to VDD and WL port of the cell. In Fig. 6b, the bit line signal is shown, However, the output can be observed by Fig. 6c which shows the value at Q and QB node of the SRAM cell.

Now, Fig. 7a, b shows the voltage transfer characteristics of the inverters used in the SRAM cell design. As it can be clearly seen from Fig. 7b that how the threshold roll-off affects the VTC of the inverter and this further influence the SNM of the cell (Hassanzadeh *et al*., 2013; Dhilleswararao *et al*., 2014; Wang, 2011; Madiwalar and Kariyappa, 2013; Sil *et al*., 2008; Sil *et al*., 2007; Wang and Choi, 2011; Nii *et al*., 2004; Premalatha *et al*., 2015; Wong, 2011).

Figure 7 and 8a, b show the static noise margin of the single port and double port SRAM cell respectively. This is obtained by taking the VTC curve of the inverter connected back to back as shown in Fig. 5. The square drawn in between the two VTC will be used for calculating the SMN value in volts.

Since, the design is working under the optimized threshold roll-off condition, so, it is necessary to check the current flow through the circuit. Figures 9a, b represent the current flow w.r.t. the supply voltage for single and double port SRAM cell, respectively. Now finally, Table 4 can summarize the obtained results of the two cells w.r.t. threshold roll-off.

Table 4: Parameters

Single SRAM cell		Double SRAM cell	
Variables	Values	Variables	Values
Read margin	340 mV	Read margin	310 mV
Write margin	290 mV	Write margin	250 mV
SNM	380 mV	SNM	320 mV
Current (max.)	≈110 μW	Current (max.)	≈260 μ W

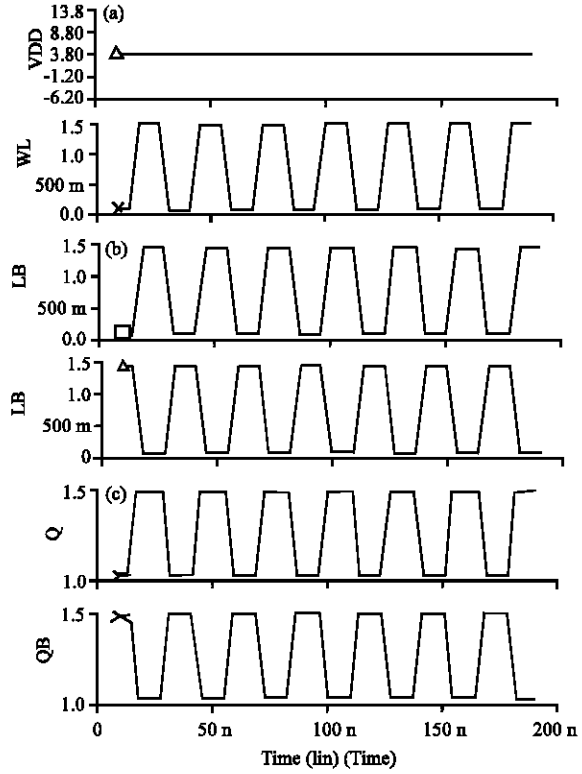

Fig. 6: Values of super voltage

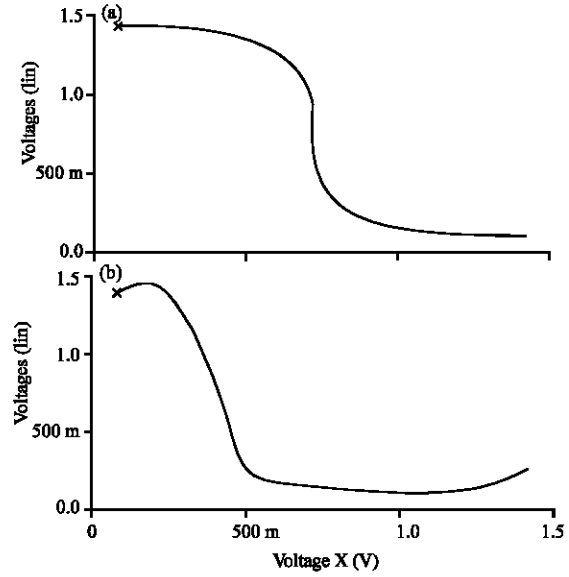

Fig. 7: Voltage transfer charecterstics

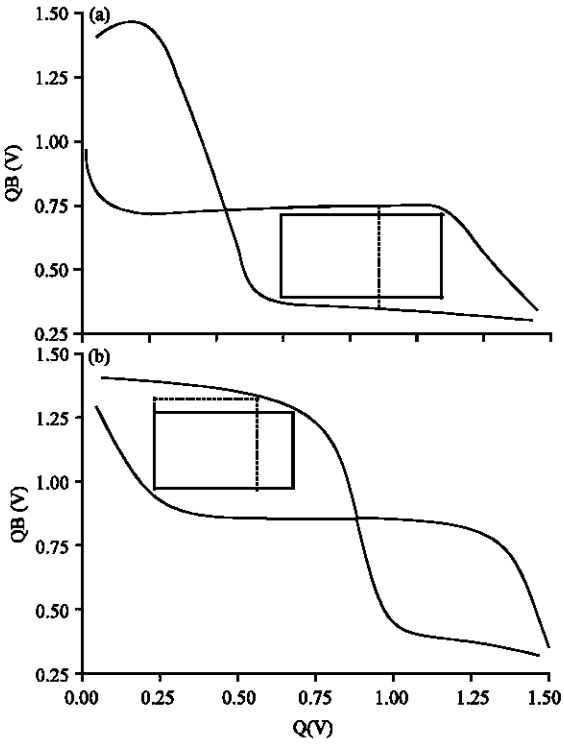

Fig. 8: Static noise margin

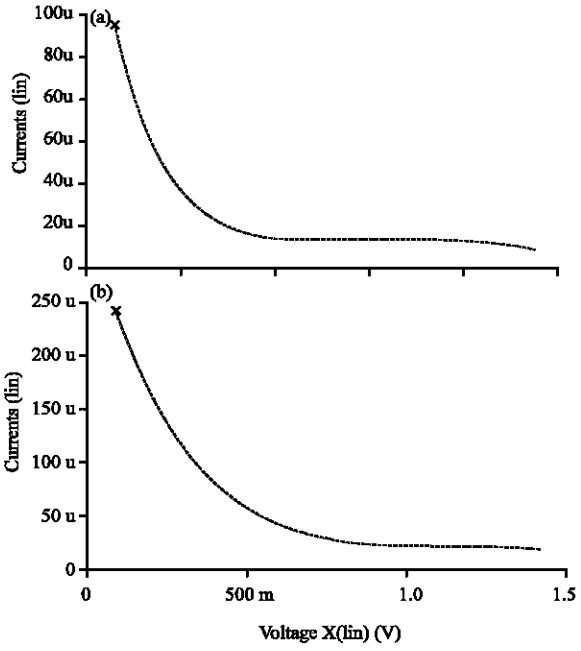

Fig. 9: Current flow

CONCLUSION

This study presents the static noise margin analysis of two different SRAM cell by optimizing the threshold

roll-off of the MOS device used in the cells. The threshold roll-off directly affects the sub-threshold current of the device which inturn affects the device performance in our case the SNM of the SRAM cell is chosen, since, the SNM of the cell is a key parameter design issue for stability and data retention of the cell. If the SNM is low the data which is stored into the cell may lost quickly and our memory may not work as desired. Hence, the device parameters are optimized and that the obtained SNM of the cell is suitable for memory cell design and proper data retention application.

REFERENCES

Abd-Elhamid, H., B. Iniguez, D. Jimenez, J. Roig and J., Pallares *et al*., 2006. Two-dimensional analytical threshold voltage roll-off and subthreshold swing models for undoped cylindrical gate all around MOSFET. Solid State Electron., 50: 805-812.

Austin, B.L., X. Tang, J.D. Meindl, M. Dennen and W.R. Richards, 1998. Threshold voltage roll-off model for low power bulk accumulation MOSFETs. Proceedings of the IEEE 11th Annual International Conference on ASIC, September 16-16, 1998, IEEE, Rochester, New York, USA., pp: 175-179.

Chang, L., Y.K. Choi, D. Ha, P. Ranade and S. Xiong *et al*., 2003. Extremely scaled silicon nano-CMOS devices. Proc. IEEE., 91: 1860-1873.

Dhilleswararao, P., R. Mahapatra and P.S.T.N. Srinivas, 2014. High SNM 32nm CNFET based 6T SRAM Cell design considering transistor ratio. Proceedings of the 2014 International Conference on Electronics and Communication Systems (ICECS), February 13-14, 2014,IEEE,Coimbatore,India isBN:978-1-4799-2321-2, pp: 1-6.

Farkhani, H., A. Peiravi and F. Moradi, 2014. A new asymmetric 6T SRAM cell with a write assist technique in 65nm CMOS technology. Microelectron. J., 45: 1556-1565.

Hassanzadeh, S., M. Zamani, K. Hajsadeghi and R. Saeidi, 2013. A novel low power 8T-cell sub-threshold SRAM with improved read-SNM. Proceedings of the 2013 8th International Conference on Design and Technology of Integrated Systems in Nanoscale Era (DTIS), March 26-28, 2013, IEEE, Abu Dhabi, United Arab Emirates isBN:978-1-4673-6039-5, pp: 35-38.

Inaba, S., R. Katsumata, H. Akatsu, R. Rengarajan and P. Ronsheim *et al*., 2002. Threshold voltage roll-up/roll-off characteristic control in sub-0.2-/spl mu/m single workfunction gate CMOS for high-performance DRAM applications. IEEE. Trans. Electron. Devices, 49: 308-313.

Ishii, K., E. Suzuki, S. Kanemaru, T. Maeda and K. Nagai *et al*., 1998. Suppressed threshold voltage roll-off characteristic of 40 nm gate length ultrathin SOI MOSFET. Electron. Lett., 34: 2069-2070.

Ito, T., K. Suguro, T. Itani, K. Nishinohara and K. Matsuo *et al*., 2003. Improvement of threshold voltage roll-off by ultra-shallow junction formed by flash lamp annealing. Proceedings of the 2003 International Symposium on VLSI Technology Digest of Technical Papers, June 10-12, 2003, IEEE, Kyoto, Japan, Japan, pp: 53-54.

Khakifirooz, A. and D.A. Antoniadis, 2006. Transistor performance scaling: The role of virtual source velocity and its mobility dependence. Proceedings of the 2006 International Conference on Electron Devices Meeting IEDM'06, December 11-13, 2006, IEEE, San Francisco, California, USA., pp: 1-4.

Lundstrom, M., 2003. Device physics at the scaling limit: What matters? MOSFETs. Proceedings of the IEEE International Conference on Electron Devices Meeting IEDM'03 Technical Digest, December 8-10, 2003, IEEE, Washington, USA., pp: 33.1.1-33.1.4.

Madiwalar, B. and B.S. Kariyappa, 2013. Single bit-line 7T SRAM cell for low power and high SNM. Proceedings of the 2013 International Multi-Conference on Automation, Computing, Communication, Control and Compressed Sensing (iMac4s), March 22-23, 2013, IEEE, Kottayam, India isBN:978-1-4673-5089-1, pp: 223-228.

Moore, G.E., 2006. Cramming more components onto integrated circuits. IEEE. Solid State Circuits Soc. Newsletter, 20: 33-35.

Nii, K., Y. Tsukamoto, T. Yoshizawa, S. Imaolka and H. Makino, 2004. A 90nm dual-port SRAM with 2.04/spl mu/m/sup 2/8T-thin cell using dynamically-controlled column bias scheme. Proceedings of the 2004 IEEE International Conference on Solid-State Circuits Digest of Technical Papers ISSCC, February 15-19, 2004, IEEE, San Francisco, California, USA., pp: 508-543.

Pavlov, A. and M. Sachdev, 2008. CMOS SRAM Circuit Design and Parametric Test in Nano-Scaled Technologies: Process-Aware SRAM Design and Test. Vol. 40, Springer, Berlin, Germany isBN:978-1-4020-8362-4, Pages: 192.

Premalatha, C., K. Sarika and P.M. Kannan, 2015. A comparative analysis of 6T, 7T, 8T and 9T SRAM cells in 90nm technology. Proceedings of the 2015 IEEE International Conference on Electrical, Computer and Communication Technologies (ICECCT), March 5-7, 2015, IEEE, Coimbatore, India isBN:978-1-4799-6084-2, pp: 1-5.

Shee, S., G. Bhattacharyya, P.K. Dutta and S.K. Sarkar, 2014. Threshold voltage roll-off and DIBL model for DMDG SON MOSFET: A quantum study. Proceedings of the 2014 IEEE International Symposium on Students Technology (TechSym), February 28-March2, 2014, IEEE, Kharagpur, India isBN:978-1-4799-2608-4, pp: 381-385.

Shih, C.H., Y.M. Chen and C. Lien, 2005. An analytical threshold voltage roll-off equation for MOSFET by using effective-doping model. Solid State Electron., 49: 808-812.

Sil, A., S. Ghosh and M. Bayoumi, 2007. A novel 8T SRAM cell with improved read-SNM. Proceedings of the IEEE International Workshop on Circuits and Systems Northeast NEWCAS, August 5-8, 2007, IEEE, Montreal, Quebec, Canada isBN: 978-1-4244-1163-4, pp: 1289-1292.

Sil, A., S. Ghosh, N. Gogineni and M. Bayoumi, 2008. A novel high write speed, low power, read-SNM-free 6T SRAM cell. Proceedings of the 51st Midwest Symposium on Circuits and Systems MWSCAS, August 10-13, 2008, IEEE, Knoxville, Tennessee, USA. isBN:978-1-4244-2166-4, pp: 771-774.

Wang, D.P., H.J. Liao, H. Yamauchi, Y.H. Chen and Y.L. Lin *et al*., 2007. A 45nm dual-port SRAM with write and read capability enhancement at low voltage. Proceedings of the 2007 IEEE International Conference on SOC, September 26-29, 2007, IEEE, Hsin Chu, Taiwan, Taiwan isBN:978-1-4244-1592-2, pp: 211-214.

Wang, W., Z. Yu and K. Choi, 2011. High SNM 6t CNFET SRAM cell design considering nanotube diameter and transistor ratio. Proceedings of the 2011 IEEE International Conference on Electro-Information Technology (EIT), May 15-17, 2011, IEEE, Mankato, Minnesota, USA. isBN:978-1-61284-465-7, pp: 1-4.

Wong, H., 2011. Nano-CMOS Gate Dielectric Engineering. CRC Press, Boca Raton, Florida, USA., Pages: 229.

Zhang, K.J., K. Chen, W.T. Pan and P.J. Ma, 2010. A research of dual-port SRAM cell using 8T. Proceedings of the 2010 10th IEEE International Conference on Solid-State and Integrated Circuit Technology (ICSICT), November 1-4, 2010, IEEE, Shanghai, China is BN:978-1-4244-5797-7, pp: 2040-2042.

Zhao, W. and Y. Cao, 2006. New generation of predictive technology model for sub-45 nm early design exploration. Proc. Electron Devices Trans., 53: 2816-2823.