Journal of Engineering and Applied Sciences 13 (14): 5826-5830, 2018
ISSN: 1816-949X

Design of Class E Power Amplifier Using SXA389BZ for Broadband Applications

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Abstract: Transmitter generally requires a power amplifier at its output stage. Application suchas telemetry of biological signals involves low power with low supply voltage into it. Low power circuits used in this transmission application requires larger loads to match with the output with high DC feed inductance when compared to high power amplifiers. Traditional power amplifier design for low power application uses various classes of amplifiers to avoid the output filters that degrade the efficiency. Class-E amplifier is anonlinear switching type power amplifier which produces high efficiency with the lowpower consumption. A new design methodology of Class-E power amplifier is proposedin this project which operates to the narrowb and range of 2.4-2.45 GHz and broadband range of 6.78 MHz-2.45 GHz is proposed. In the narrowband design inductance constraint is removed by varying the supply voltage. The broadband model is accomplished by high power and low power transistor. The efficiency of the power amplifier is increased by increasing the order of the input and output matching network. The circuits are simulated using Advanced Design Systems (ADS-2011).

Key words: Class-E power amplifier, gain, output voltage, broadband applications, transistor, ADS

INTRODUCTION

With the increase in the use of hand held communication devices, a high efficiency power amplifier is needed at the transmitter output stage. Low power application circuit generally considered to have low efficiency when compared with high power circuits. Application such as telemetry of biological signals involves low power with low supply voltage into it. Low power amplifier circuits used in this transmission application require larger loads to match with the output with high DC feed inductance when compared to high power amplifiers. Thus, the power amplifiers designed for low power application has lower efficiency than high power circuits.

Power Amplifier (PA) is very challenging to researchers as it requires for providing high power with high efficiency. PA is generally a DC to AC converter which is driven by its input signal (Suetsugu and Kazimierczuk, 2008). During last few years, the field of interest of microwave design has shifted to monolithic circuit from the arena of hybrid components (Lee *et al*., 2010) this reduces the cost of power amplifier. This change is due to the advancement of semiconductor technology which makes the monolithic designsto be delivered in the hardware as they are manufactured in bulk numbers. Thus, the substrates employing monolithic circuits are selected by system requirement (Brama *et al*., 2008; Deen *et al*., 2007) other cause is that all RF and microwave designs can easily be implemented by CAD methods improves the circuit-modeling techniques. These changesmake the Microwave Monolithic Integrated Circuits (MMIC) to be "Time to market" Class-E power amplifier provides high efficiency topology (Gracia *et al*., 2013; Chuang *et al*., 2015). Class-E amplifier is a non linear switching type power amplifier makes transistor to actas a switch. Vs is the switch voltage (Rivas *et al*., 2011), Cj0 is the drain-to-source capacitance at V_s equal to 0 and V_{bi} is the built-in potential of the MOSFET (Kazimierczuk and Jozwik, 1989) the rectifier process achieving developing the value of power and voltage current and power input is 0-15 mW is used.

POWER AMPLIFIER DESIGN

The design values are based on the analytical derivation of ideal Class-E PA. The proposed circuit is designed in order to increase the efficiency ofthe circuit. From Fig. 1 instead of RF Choke the DC feed inductance is used, so that, the constrained produced by the inductance (L0) in the conventional class-E PA is relaxed. The aim of the design work focus on optimization of high output level withlow output power and high efficiency. The low output power is obtained by removing the

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inductance constraint with DC feed inductance, so that, the inductance value is smaller. The harmonic rejection produced by the amplifier is reduced by the series resonant network. The efficiency of the circuit is increased by varying the supply voltage. The variation in supply voltage has great impact on the transistor further varies the output power efficiency. The PA requires both input and output matching network. The output is always matched with the load resistance of 50 Ω. The circuit is generally divided into three stages: Pre-driver stage, PA stage.

Pre-driver stage is the mandatory stage to the PA since, the output power depends on the input signal. The switching transistor is driven by the input signal. The CMOS inverter acts as the pre-driver stage. Due to the large loading capacitance the inverter consumes high power, thus, degrades the overall efficiency.

The FET Model chosen for the work is Bi-SIM Model which works with the model file of 90 nm technology. The model file for both NMOS and PMOS Model of the corresponding technology are used. The plot obtained shows the graph between the Drain Current, DC power consumption with bias voltage. The DC analysis of BISIM Model shows that the curve plotted by sweeping the values of VGS and the corresponding output between the drain and source ismeasured. The value of power consumption of the device is also plotted.

From Fig. 2, the current probe IDS used to measure the current values and the voltage probe is placed in drain and gate of MOSFET device and the device measured the current and voltage values and the power consumption of the device is shown.

From Fig. 3, the process of BISIM FET Model-DC analysis drain current versus the bias curve and the result shows the drain current and voltage values increases and the value of voltage gate values also increased and the device voltage is measured the current of drain values starts from zero value and the voltage values reaches the VGS = 3 V and the drain voltage reaches the 5.000 V.

The DC power consumption values from Fig. 4, the DC power increases the value the voltage drain VDS and the MOSFET device also gets increased, the value of 0.0025 power and the VGS reaches upto SIM values of VGS is 3.000 V.

From Fig. 5, the proposed Class-E power amplifier shows the three different stages and the first one is pre-driver stage the model of device is connected and the process of current probe used for the current values and the input voltage of sinewave changes and the condition of VDC values of voltage values for reducing the leakage the current values and second process shows the process

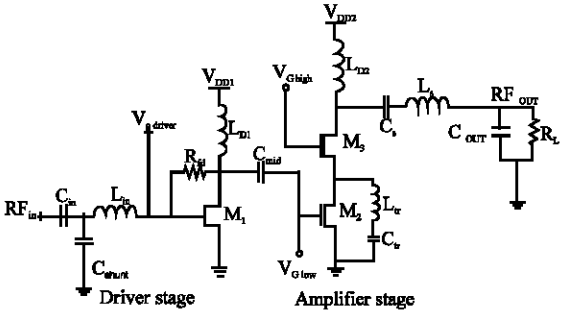

Fig. 1: Circuit diagram of power amplifier

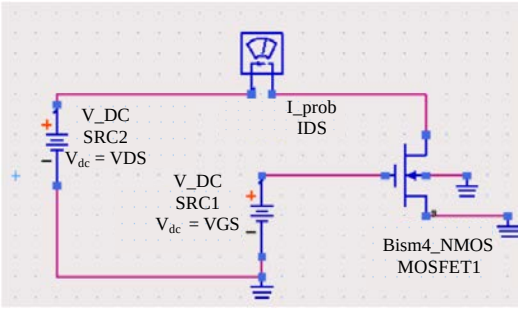

Fig. 2: Schematic of BISIM FET Model-DC analysis

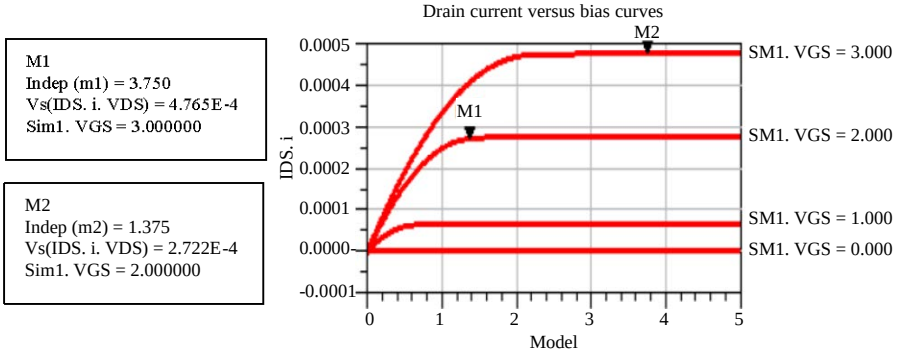

Fig. 3: ID-VDS curve

of single device connected to the inductance for the purpose of reducing the negative resistance and the process can increase the value of sine, the process of third process is power amplifier used for increasing the overall values of the design and boosting the device to get high amplifier and less distortion and the function of capacitance used to reduce the leakage of current and the process of the device achieves high efficiency.

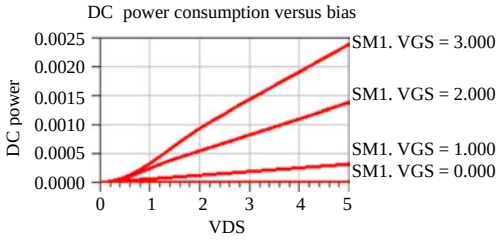

Fig. 4: DC Power-VDS

The process of proposed circuitry results shows the time period of the first is 1 GHz and the sinewave is measured and the second is output value 1.07 is the output value and the time period is 500, the voltage output 1 is the process 1.35 V value is achieved for the same 500 nano second timeperiod and the output voltage values of power amplifier shows the combination of the three stages of the design is pre-driver stage and the power amplifier stage is main and the blue curve shows the output voltage vo and the red curve shows the output value of the overall design and the output increased to 2.4 GHz and the voltage value is decreased to the 0.32 V. The overall design of the power amplifier using the BISIM model determines the function of boosting the output values and the power amplifier and four figure of result are shows the BISIM FET Model transistor (Fig. 6).

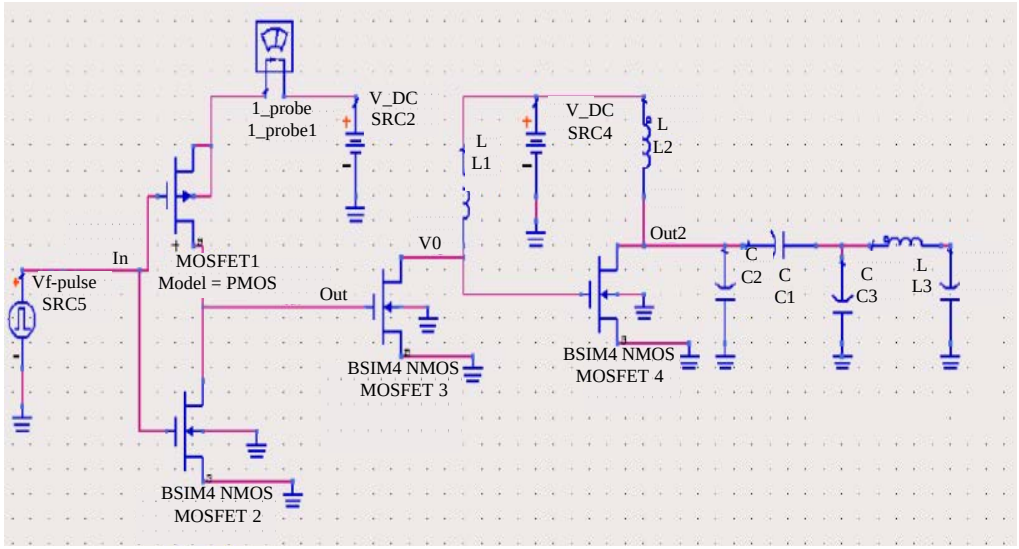

Fig. 5: Circuitry of the proposed Class-E power amplifier

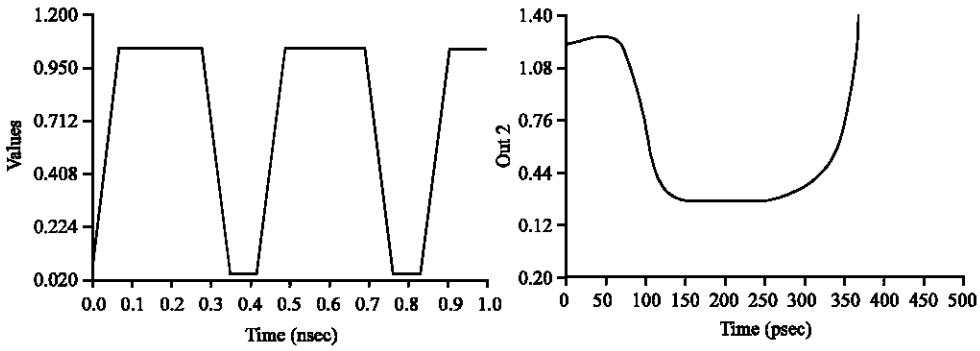

Fig. 6: Continue

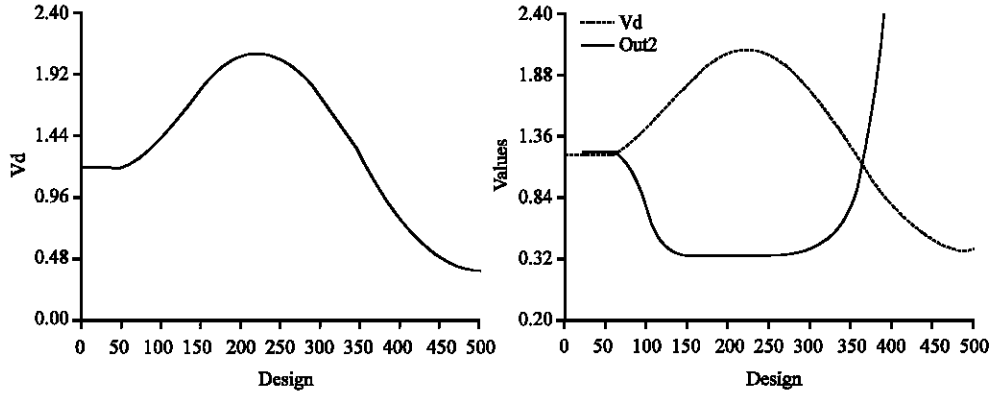

Fig. 6: Results obtained at three stages of proposed design

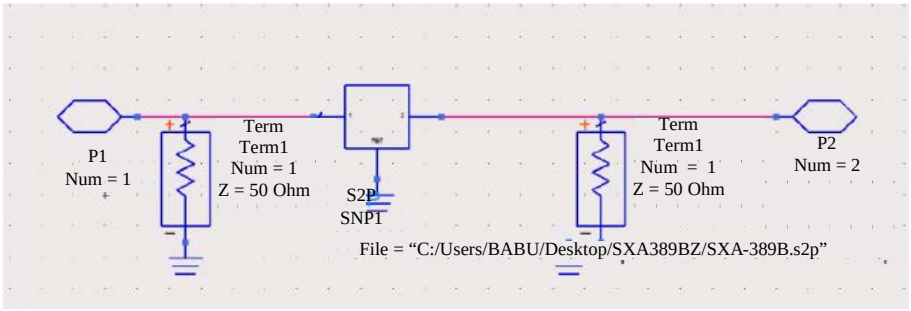

Fig. 7: S Parameter of SXA389BZ-schematic

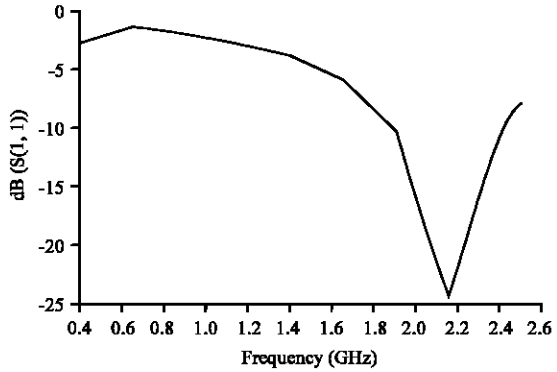

Fig. 8: S11 of SXA389BZ

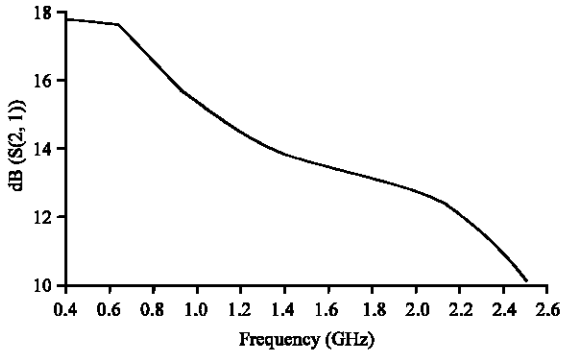

Fig. 9: S21 of SXA389BZ

The process of measuring the value of s parameter using the SXA389BZ device for the S11 and S21 values are measured, the SNP1 is the small symbol of the device and the port 1 is the input port and the port 2 is the output port and the terminator is used for the impedance value and the process of placing both side measuring the s parameter. From Fig. 6, the device is copied in the system (Fig. 7).

From Fig. 8, the S11 parameter is measured the value of return loss is achieves the -24 dB for the frequency of 2.1 Ghz and achieves good return loss for the efficient frequency value and the dB value starts from the -4 dB to -24 dB values the curve of the device is good in the design.

From Fig. 9, the process of the insertion loss or transmission loss shown dB (S(2, 1)) at the frequency of 2.4 GHz achieves the process of the 18 dB value and the condition of the s parameters are the achieved.

CONCLUSION

The narrowband power amplifier is designed using BSIM Model transistor and the broadband power

amplifier for high power application is designed using RF3931 GaN-HEMT and for low power application SXA3489BZ is used. From the DC analysis of narrowband and broadband power amplifier, the power consumption is measured. It is found to be 0.010 W with 1 V power supply for BSIM model transistor and the drain efficiency is 43% and the s parameter value for S11 is -24 dB and for S21 is 18 dB value.

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