Journal of Engineering and Applied Sciences 13 (15): 6167-6172, 2018
ISSN: 1816-949X

A New Combination Method to Error Detection and Correction Using VHDL

Adham Hadi Saleh, Wisam Najm Al-Din Abed and Adnan M. Taha
Department of Electronic Engineering, College of Engineering,
University of Diyala, Baqubah, Iraq

Abstract: In this study, we proposed a new technique to detect and correct single and burst errors using Hybrid Automatic Repeat-Request (HARQ) which mainly depended on merging of CRC (Cyclic Redundancy Check) and Hamming code at the same time, single error covered by FEC (Foreword Error Correction) using Hamming code while burst error would be covered by retransmitted. The Xilinx ISE 10.1 simulator was used for simulating VHDL (VHSIC (Very High Speed Integrated Circuit) Hardware Description Language) code for both the transmitter and receiver sides. The transmitter and receiver circuits has been designed and implemented successfully.

Key words: CRC, Hamming coding, HARQ and VHDL, transmitter, implemented, burst error

INTRODUCTION

In any communication systems based on (information theory and coding theory) must be able to transfer data with acceptable accuracy, so, error control technique is one of the most important part at any communication systems (Anonymous, 2018).

Basically to corrected error it's need to be detection it firstly when system is transmit information it's send original data and extra bit to ensure that the original data arrived successfully. This extra bits represented the remainder of division of original message (CRC method) or comes from parity check method (one dimension or two dimension) or any other methods using to detect and corrected errors (Forouzan, 2011).

Error correction can be realized basic in two ways: Automatic Repeat Request (ARQ) and Forward Error Correction (FEC). Sometime ARQ and FEC can combined this method is called Hybrid Automatic Repeat-Request (HARQ) (Anonymous, 2018; Forouzan, 2011).

In this study, we solve the problem of undetected state in Hamming code with single error and in CRC technique be merging this two techniques in one technique two ensure the original data arrived successfully in the same time data corrected using Hybrid Automatic Repeat-Request (HARQ) by merged of Hamming Forward Error Correction (FEC) to single bits and Automatic Repeat Request (ARQ) by send an Acknowledgement to transmitter to resending data where system design using VHDL to implementation it at progressive steps.

Comparison with related work: A literature survey for many previously published works in this field are designed error detection and correction systems but with separated technique and different data rate such as error detection and correction using CRC technique only (Shukla and Bergmann, 2004; El-Medany, 2012; Sprachmann, 2001; Saleh *et al*., 2018; Nair *et al*., 1997) or error detection and correction using Hamming technique only (Zhang and Ding, 2011; Fitriani *et al*., 2016; Shep and Bhagat, 2013; Saleh, 2015) and many other works. These studies are design CRC and Hamming as separate system. In this study, the system designed by combination CRC and Hamming are in one new technique system using VHDL and increased data input to get high data rate with high reliability.

MATERIALS AND METHODS

This system have an input data 24 bits (3 byte) that passes through a transmitter circuit which is consist of a combination coding method based on (CRC and Hamming) coding and at the receiver the incoming data (38 bits) will be passed through a receiver circuit that merge Hamming decoding and CRC decoding methods, Hamming decoding circuit that correct all single error and cancelled all extra bits added at the Hamming encoder circuit (this cancellation may be moving burst error get at redundancy bits itself) then data bits will arrived to CRC decoder circuit which detect all other type of errors and sending an acknowledgment to the sender to retransmitted of data. This design will be increase the accuracy, performance and reliability of the system, the transmitter and receiver system designed using VHDL.

Transmitter circuit: The block diagram and general design of transmitter circuit is shown in Fig. 1.

Corresponding Author: Adham Hadi Saleh, Department of Electronic Engineering, College of Engineering, University of Diyala, Baqubah, Iraq

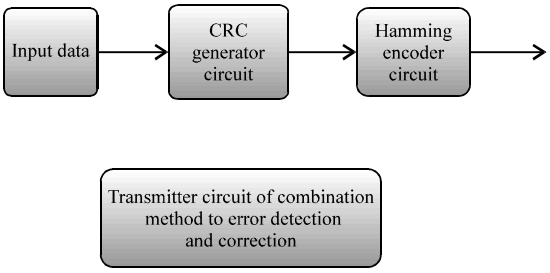

Fig. 1: Block diagram transmitter circuit of combination method to error detection and correction

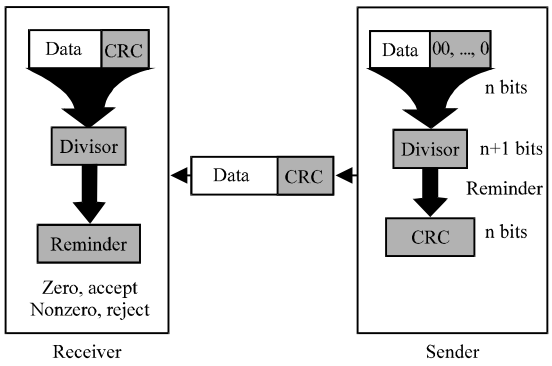

Fig. 2 : CRC generator and checker

CRC generator circuit: The main part of CRC technique is binary division that is different from another methods to error detection that is based on parity check. The cyclic redundancy check depends on the division remainder at the transmitter (CRC generator circuit) that is added to transmitted data. The basic block diagram and general design of CRC generator-checker is shown in Fig. 2 (Forouzan, 2011).

In this study, the CRC generator and checker circuits are designed with X^8+X^2+X+1 divisor polynomial that is used at Asynchronous Transfer Mode (ATM) header. The CRC method-based framing re-using the header (CRC) is improving the efficiency of a pre-standard (ATM) protocol links which is present in ATM and other similar protocols to provide framing with no overhead adding on the link. In ATM this is known as the Header Error Control/Check (HEC) field (Rhee, 1989; Goresky and Klapper, 2002).

RESULTS AND DISCUSSION

Hamming encoder circuit: Hamming code is one of the most important method to error detection and correction method based on add extra bits to the transmitted data, it is an efficient method when the data rate is low like in computer memory, the redundancy bits is added to the original data according to an even or odd parity method to generated redundancy bit. The redundancy bits number are depended on information data bits as shown (Saleh, 2015):

$$2^r \geq m+r+1 \quad (1)$$

where, r is redundancy bits and mi s data bits, so to transmitted 32 bits (original data bits (24) bits and CRC remainder 8 bits) according to Eq. 1 we need 6 redundancy bits (R1, R2, R4, R8, R16 and R32) these redundancy bits based on even parity check which are grouped as showing in equations:

$$\begin{aligned}R(1)= &DATA(1)\oplus DATA(2)\oplus DATA(4)\oplus\\ &DATA(5)\oplus DATA(7)\oplus DATA(9)\oplus DATA(11)\\ &DATA(12)\oplus DATA(14)\oplus DATA(16)\oplus DATA\\ &(18)\oplus DATA(20)\oplus DATA(22)\oplus DATA(24)\oplus\\ &DATA(26)\oplus DATA(27)\oplus DATA(29)\oplus DATA\\ &(31)\end{aligned} \quad (2)$$

$$\begin{aligned}R(2) = &DATA(1)\oplus DATA(3)\oplus DATA(4)\oplus\\ &DATA(6)\oplus DATA(7)\oplus DATA(10)\oplus DATA\\ &(11)\oplus DATA(13)\oplus DATA(14)\oplus DATA(17)\oplus\\ &DATA(18)\oplus DATA(21)\oplus DATA(22)\oplus DATA\\ &(25)\oplus DATA(26)\oplus DATA(28)\oplus DATA(29)\oplus\\ &DATA(32)\end{aligned} \quad (3)$$

$$\begin{aligned}R(4) = &DATA(2)\oplus DATA(3)\oplus DATA(4)\oplus\\ &DATA(8)\oplus DATA(9)\oplus DATA(10)\oplus\\ &DATA(11)\oplus DATA(15)\oplus DATA(16)\oplus\\ &DATA(17)\oplus DATA(18)\oplus DATA(23)\oplus\\ &DATA(24)\oplus DATA(25)\oplus DATA(26)\oplus\\ &DATA(30)\oplus DATA(31)\oplus DATA(32)\end{aligned} \quad (4)$$

$$\begin{aligned}R(8) = &DATA(5)\oplus DATA(6)\oplus DATA(7)\oplus\\ &DATA(8)\oplus DATA(9)\oplus DTA(10)\oplus\\ &DATA(11)\oplus DATA(19)\oplus DATA(20)\oplus\\ &DATA(21)\oplus DATA(22)\oplus DATA(23)\oplus\\ &DATA(24)\oplus DATA(25)\oplus DATA(26)\end{aligned} \quad (5)$$

$$\begin{aligned}R(16) = &DATA(12)\oplus DATA(13)\oplus\\ &DATA(14)\oplus DATA(15)\oplus DATA(16)\oplus\\ &DATA(17)\oplus DATA(18)\oplus DATA(19)\oplus\\ &DATA(20)\oplus DATA(21)\oplus DATA(22)\oplus\\ &DATA(23)\oplus DATA(24)\oplus DATA(25)\oplus\\ &DATA(26)\end{aligned} \quad (6)$$

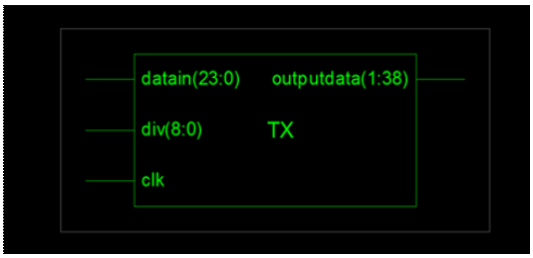

Fig. 3: Transmitter block diagram

Table 1: Ttransmitter circuits output data

Random data bits	The transmitted data
Hex 654321	Hex 0315464306
Hex FFFFFF	Hex 1BFFFFFE4F
Hex AAAAAA	Hex 2D6A95540A
Hex F0F0F0	Hex 0F83A1E166

Table 2: Pins description of the transmitter circuit

Signal	Direction	Size	Description
CLK	Input	1	Clock signal that clocks all internal component
DIV	Input	9	Input divisor data represented in binary bit stream
Datain	Input	24	Input data represented in binary bit stream
Output	Output	38	Output data of the transmitter circuit

Table 3: Summary of the transmitter circuit

Logic Utilization	Used
Number of slices LUTs	119
Number of bonded IOBs	70

$$R(32) = DATA(27) \oplus DATA(28) \oplus DATA(29) \oplus DATA(30) \oplus DATA(31) \oplus DATA(32) \quad (7)$$

The transmitter circuit output data is shown in Table 1, the transmitter block diagram is shown in Fig. 3, it's pins desecration is explained in Table 2, the summary of the transmitter circuit is shown in Table 3 and time simulation is shown in Fig. 4.

Receiver circuit: The receiver circuit is consist of two merged circuit: Hamming decoder and CRC checker as shown in Fig. 5.

Hamming decoder circuit: At the destination side the information data consist of 38 bits that are passed though Hamming decoder circuit which is detected and corrected single error and remove the redundancy bits added at the encoder circuit .

Hamming decoder circuit detect the single error by exoring, of received data and determine a position of error bit then correct it using a NOT gate then the receiver is removed the redundancy bit and forward the data to the next circuit in receiver system. As shown in equation:

$$2^0 = DATA(1) \oplus DATA(3) \oplus DATA(5) \oplus DATA(7) \oplus DATA(9) \oplus DATA(11) \oplus DATA(13) \oplus DATA(15) \oplus DATA(17) \oplus DATA(19) \oplus DATA(21) \oplus DATA(23) \oplus DATA(25) \oplus DATA(27) \oplus DATA(9) \oplus DATA(31) \oplus DATA(32) \oplus DATA(35) \oplus DATA(37) \quad (8)$$

$$2^1 = DATA(2) \oplus DATA(3) \oplus DATA(6) \oplus DATA(7) \oplus DATA(10) \oplus DATA(11) \oplus DATA(14) \oplus DATA(15) \oplus DATA(18) \oplus DATA(19) \oplus DATA(22) \oplus DATA(23) \oplus DATA(26) \oplus DATA(27) \oplus DATA(30) \oplus DATA(31) \oplus DATA(34) \oplus DATA(35) \oplus DATA(38) \quad (9)$$

$$2^2 = DATA(4) \oplus DATA(5) \oplus DATA(6) \oplus DATA(7) \oplus DATA(12) \oplus DATA(13) \oplus DATA(14) \oplus DATA(15) \oplus DATA(16) \oplus DATA(20) \oplus DATA(21) \oplus DATA(22) \oplus DATA(23) \oplus DATA(28) \oplus DATA(29) \oplus DATA(30) \oplus DATA(31) \oplus DATA(36) \oplus DATA(37) \oplus DATA(38) \quad (10)$$

$$2^3 = DATA(8) \oplus DATA(9) \oplus DATA(10) \oplus DATA(11) \oplus DATA(12) \oplus DATA(13) \oplus DATA(14) \oplus DATA15) \oplus DATA(24) \oplus DATA(25) \oplus DATA(26) \oplus DATA(27) \oplus DATA(28) \oplus DATA(29) \oplus DATA(30) \oplus DATA(31) \quad (11)$$

$$2^4 = DATA(16) \oplus DATA(17) \oplus DATA(18) \oplus DATA(19) \oplus DATA(120) \oplus DATA(21) \oplus DATA(22) \oplus DATA(23) \oplus DATA(24) \oplus DATA(25) \oplus DATA(26) \oplus DATA(27) \oplus DATA(28) \oplus DATA(29) \oplus DATA(30) \oplus DATA(31) \quad (12)$$

$$2^5 = DATA(32) \oplus DATA(33) \oplus DATA(34) \oplus DATA(35) \oplus DATA(36) \oplus DATA(37) \oplus DATA(38) \quad (13)$$

So, after applying the last equation at the received data, we can detected the error bit position (2^5 2^4 2^3 2^2 2^1 2^0) and corrected it.

Table 4: Receiver parameters and correct output data

Random received data	Hamming circuit SEDAN DC	CRC decoder RETRANS	Output data description
Hex 0315464306	0	Hex 00	Received data correct without error
Hex 1BFFFFFE4F	0	Hex 00	Received data correct without error
Hex 2D6A95540A	0	Hex 00	Received data correct without error
Hex 0F83A1E166	0	Hex 00	Received data correct without error
Hex 03154643016	1	Hex 00	Received data have a single error and it is detect and correct by forward error correction
Hex 0F13A1E166	1	Hex 34	Received data have a burst error and it is detect and correct by retransmitted

Table 5: Pins description of the transmitter circuit

Signal	Direction	Size	Description
Clock	Input	1	Clock signal that clocks all internal component
Divisor	Input	9	Input divisor data represented in binary bit stream
Hamin	Input	38	Input data represented in binary bit stream
Received	Output	24	Output data of the receiver circuit
Retrans	Output	8	Output signal (acknowledgement) send to transmitter system to retransmitted of data, if output signal HEX00 the received data is correct otherwise it's corrupted and need to retransmitted
Sedandc has a single	Output	1	Output signal(acknowledgment) mean that received data input error and it is detected and corrected

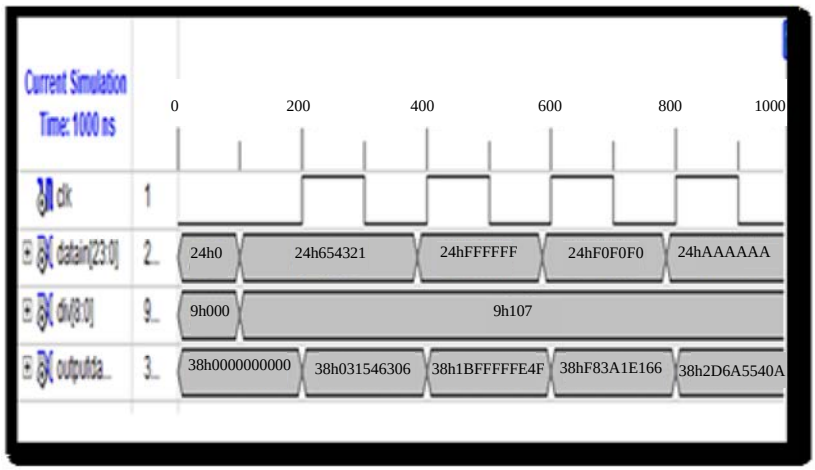

Fig. 4: Time simulation of transmitter circuit

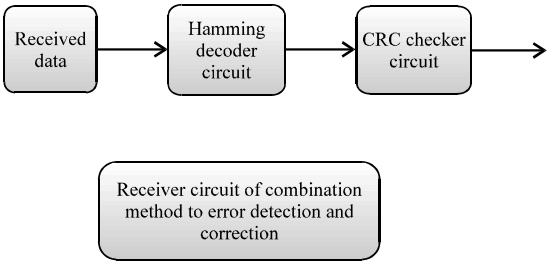

Fig. 5: Block diagram receiver circuit of combination method to error detection and correction

CRC checker circuit: At CRC checker circuit the incoming data unit (32 bits) from Hamming decoder circuit is divided by divisor that is used at the Transmitter system then to knowing if the received data unit is correct or corrupted, it is needed to checking the remainder of division If the CRC decoder checkers get a zero remainder then arrived data unit is correct, else it has been corrupted as shown before in Fig. 2 (Forouzan, 2011). An error data frame is corrected by sending an acknowledgment to sender to retransmitted data frame.

The receiver circuit parameters and correct output data is shown in Table 4, the receiver block diagram is shown in Fig. 6, it's pins desecration is explained in Table 5, the summary of the receiver circuit is shown in Table 6 and time simulation is shown in Fig. 7.

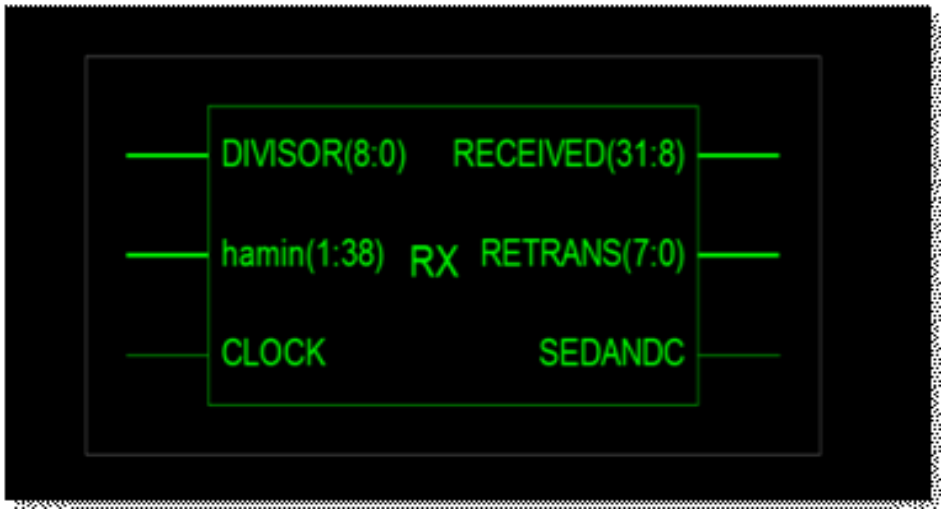

Fig. 6: Receiver block diagram

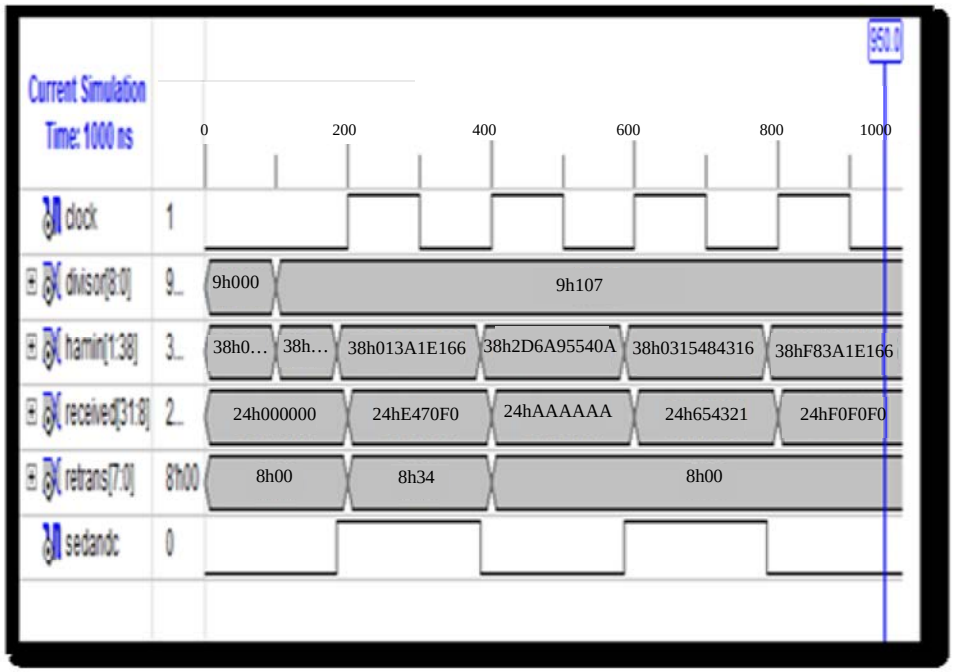

Fig. 7: Time simulation of receiver circuit

Table 6: Summary of the receiver circuit

Logic utilization	Used	Available	Utilization (%)
Number of slices registers	32	19200	0
Number of slices LUTs	260	19200	1
Number of fully used bit slices	32	260	12
Number of bonded IOBs	79	220	35
Number of BUFG/BUFGC TRLs	1	32	3

CONCLUSION

This study presents a mixed-error detection and correction method (Hamming coding and CRC) Hybrid Automatic Repeat-request (HARQ) the transmitter and receiver systems are designed and implemented using VHDL, successfully. The complete process of system design are shown in the previous sections. This model gives accurately, high reliability and ensure delivery as compared with other error detection and correction systems. The time simulation data result is match an expected output data that are explained. The proposed circuits show that low hardware usage are required which make them suitable to be integrated with any other system.

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