Journal of Engineering and Applied Sciences 13 (Special Issue 8): 6335-6340, 2018
ISSN: 1816-949X

Low Power Implementation of DTMF Chip by Using Power Gating Technique with Merge Flops

[1]Anuradha Shankar, [2]Srinivas Manchala and [1]N. Mohan Kumar
[1]Department of Electronics and Communication Engineering, Amrita School of Engineering, Coimbatore, Amrita Vishwa Vidyapeetham, Amrita University, 641112 Tmil Nadu, India
[2]Digicomm Semiconductor Pvt. Ltd., 560103 Bangalore, India

Abstract: With the advent of technology and increasing concern for designing low power devices, systems with longer sustaining battery life are the demand. This study focuses on design of low power DTMF chip which is extensively used in telecommunication systems. Firstly, the existing techniques are implemented and compared with the power gating technique that results in reduction in leakage power consumption by 96% and the overall power consumption by 7% compared to the design without low power intent. The addition of low power cells in power gating technique results in an increase in area by 15% at the placement stage and a placement density >100% after routing. An algorithm is proposed to improve the efficiency of power gating by restricting the impact of this increase in area due to addition of low power cells by using merge flip-flops.

Key words: Dual Tone Multi Frequency (DTMF), power gating, merge flops, dynamic power, leakage power, India

INTRODUCTION

Today, power is undoubtedly emerging as the major design goal in modern System-on-Chip (SoC) designs due to shrinking process technology. With every new process generation, applications are designed with billions of transistors packed in a single sliver of silicon. This has resulted in increased power densities at every process node having ramifications in system productivity which include-reduced reliability, shorter battery life and increasing costs in cooling the systems (Priya and Baskaran, 2013). The size and complexity of the SoCs make it imperative to manage power dissipation at every stage of the design development process starting from the architecture design to final design tapeout. The primary concern of the designers now lies in improving the performance and reducing the silicon area in order to reduce the silicon manufacturing costs.

Dual Tone Multi Frequency (DTMF) is a common signalling method that is used in all modern day telecommunication systems. It's used in dialing number pads and for configuring telephone exchanges from remote locations. All mobile phones generate DTMF tones provided connections are established. DTMF also finds applications in credit card systems, personal computers etc. All these applications are either portable and or handheld, hence, battery powered. So, it's highly desirable to design such systems with low power consumption.

As the process technology is decreasing from 90 nm and further below, system performance and density trends are being taken to new levels, yet, high power loss makes design of these devices, a difficult challenge. The total power dissipation comprising of dynamic and leakage power is a function of the switching factor α, capacitance C, voltage VDD and the transistor structure. While dynamic power is dissipation occurs only when there is switching activity in the circuit, leakage power dissipation occurs at all times. Also as the process technology shrinks the leakage power dominates dynamic power dissipation, thus, becoming the major source of power dissipation as can be seen in Fig. 1. Thus, the primary concern in this work is reducing the leakage power consumption at lower process technologies. In this study, low power consuming DTMF chip is designed by using power gating technique. Power gating , also called power shut off, switches off the power supply to selected functional blocks that are idle. Though the technique reduces leakage power by a large margin, it results in increase in area occupied by the cells in the design and hence increase in routing resources required. The proposed enhanced power gating technique compacts the area occupied by the cells by merging the flip flops (Liu *et al*., 2013) in addition to decreasing the power consumption.

Corresponding Author: Srinivas Manchala, Digicomm Semiconductor Pvt. Ltd., 560103 Bangalore, India

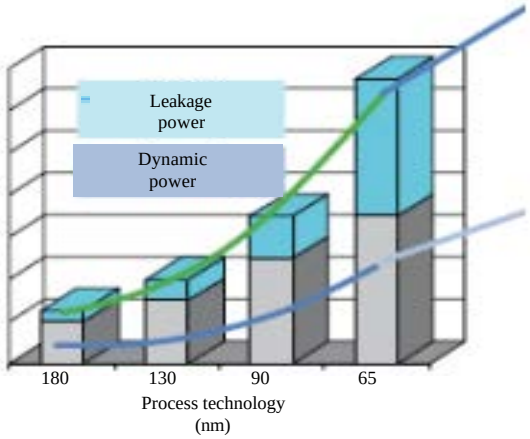

Fig. 1: Leakage vs. dynamic power trend (Liu *et al*., 2013)

MATERIALS AND METHODS

Low power methodology: There are several low power management techniques proposed that reduce power dissipation from which, the multi threshold voltage, Multi Supply Voltage (MSV) and Power Shut Off techniques (PSO) mainly reduce the leakage power. In this research, the MSV and PSO techniques are implemented using Common Power Format (CPF) which is a Silicon integration initiative (Si_2) standard for specifying power saving techniques starting from an early phase in design cycle (PFI., 2008).

Multi threshold Voltage (V_t): It is the most commonly used leakage power reduction method in which transistors having different switching thresholds are employed as shown in Fig. 2. The basic requirement for this method is cells with different threshold voltage libraries of same functionality as of the cell. Low threshold voltage cells have faster switching and higher leakage power dissipation. Such cells are placed on critical paths in the design to have lesser delays. High threshold voltage cells have slower switching and less leakage power dissipation. Such cells are placed on non critical paths. Multi V_t cell placement is done post clock tree synthesis stage. As shown in Table 1 below, the cells having larger transition are replaced with low V_t cells and the slack changes from -1.02 n to 0.001 n sec.

Multi Supply Voltage (MSV): Depending upon the performance requirements, certain portions of the chip are operated at different supply voltages. The functional blocks operating at different voltages are assigned to different voltage islands. MSV technique requires level shifters to translate the signal voltage levels from one voltage island to another to ensure signal integrity. The technique implementation involves following tasks (Fig. 3 and 4).

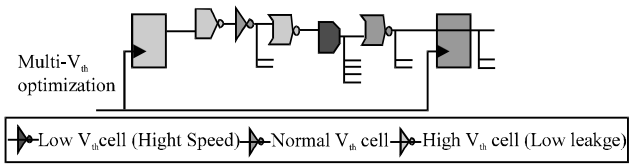

Fig. 2: Addition of multi threshold cells (Liu *et al*., 2013)

Table 1: Multi V_t example

		Slack (nsec)	
Cell type	Path (reg2reg)	Before	After
Low V_t cell placement	Path 1	-1.02	0.01
High V_t cell placement	Path 2	4.057	2.89

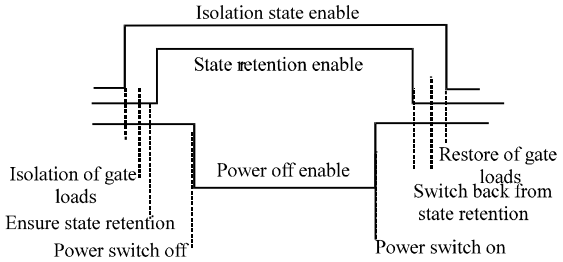

Fig. 3: Power gating off-on sequence

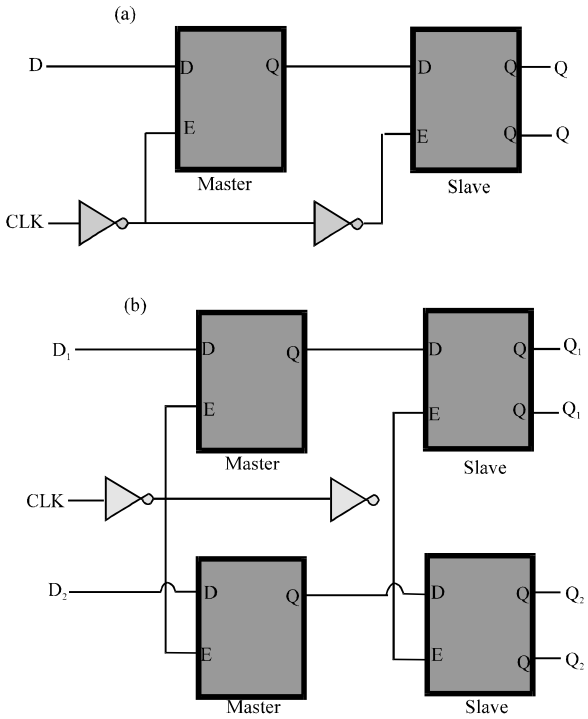

Fig. 4: Concept of flip flop merging (Liu *et al*., 2013): a) one-bit-flip-flop and b) Two-bit-flip-flop

Creation of power domains/voltage islands: This is done at the floorplanning stage. Every domain is associated with a set of library for that specific domain.

Placement and optimization: The tool honors the power domain boundaries and places and optimizes the cells only with libraries associated with each power domain.

Handling of the level shifter and isolation cells: Level shifters and isolation cells are inserted at the placement stage by committing the Common Power Format (CPF) file. The placement of these cells are controlled by rules defined in CPF.

Power Shut Off/Power Gating (PSO): As the name suggests, PSO technique involves completely powering off a functional block when they are idle. Creation of voltage islands and addition of level shifter and isolation cells are similar to that of the MSV technique in addition, to retain the states of the functional block being shut down, state retention registers are added through CPF as in Lakshmi *et al.* (2011). This involves replacing the normal flip flops in the domain being shut off with state retention flops. State retention flops function as normal flops when no power gating is employed. When a control to shut off the block is passed, the isolation cells separate that block from the design and the current state of the block is retained by these registers. Then the supply to the block is cut off as per the sequence. The sequence of state restoration when the power gating is removed is exactly opposite to the shut off sequence as shown in Fig. 3-5.

Proposed technique-power gating with merge flops: In the power gating technique, due to addition of low power cells like state retention flip flops, isolation cells and power switching cells the total area occupied by the standard-cells and the low power cells increases by 14%.

This results in a placement density >100% after routing stage which means loss of data as these cells sit outside the core area. For designs which have restricted area this is a serious issue. In order to improve the efficiency of power gating method, single-bit flip-flops are combined into multi-bit flip-flops. According to Liu *et al.* (2013), flip flops require lesser driving power with shrinking technology, which implies a single inverter can drive multi bit flops. Thus, merging has the advantage of decreased power consumption apart from compacting the area.

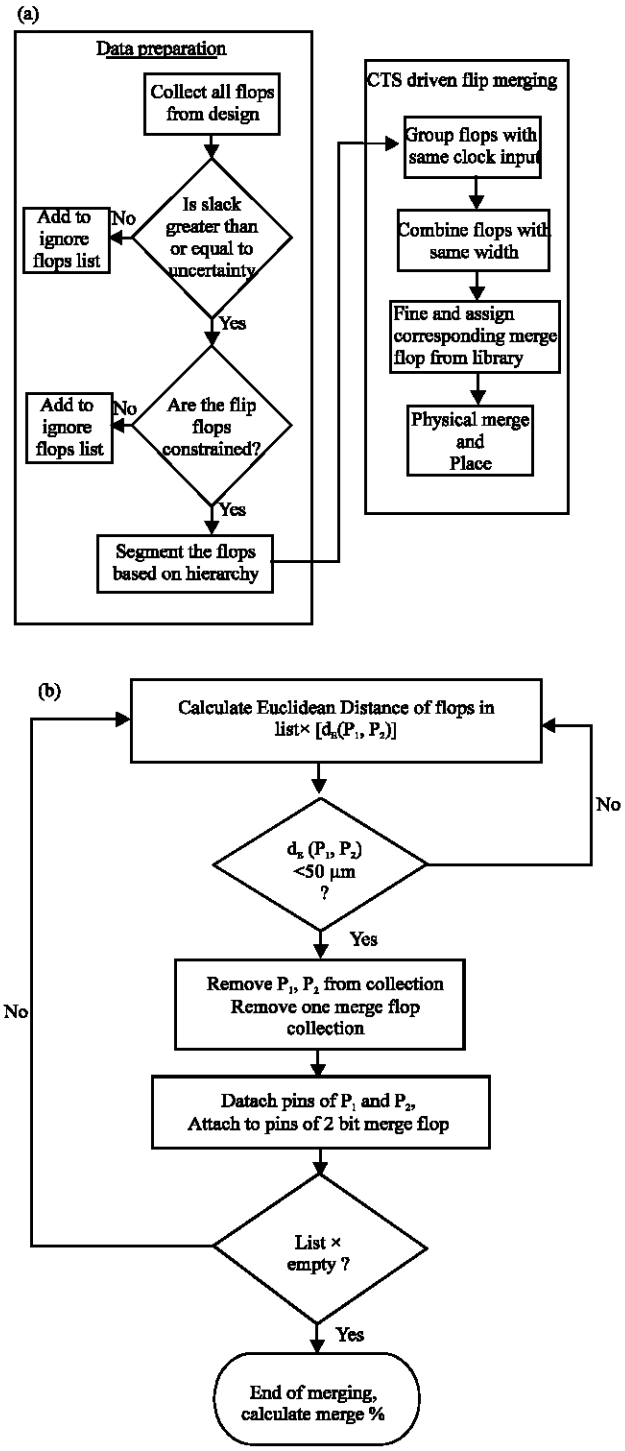

Fig. 5: a) Flowchart for the proposed technique and b) Sequence for physical merging of flip flops

In the proposed algorithm, this concept of merging the flip flops is used. Figure 4 shows how the two-bit merged flip-flop are formed using two single bit D flip

flops. As can be seen in Fig. 4, a single inverter drives two flip flops. The advantage of this technique is:

- Reduction of area occupied by the cells in the design
- Reduction in CTS wirelength due to merging of flops, which means minimizing the use of routing resources
- Reduced power dissipation in the clock network, i.e., decreased dynamic power consumption

Figure 5 below is the flow chart on the algorithm for merging flip flops. The overall process can be categorized into two main sections. Data preparation and flip flop merging

Data preparation: In this step, valid list of flip flops are created. In this step, out of all the available flops in the design only those flops that are suitable for merging are filtered out initially. So, those flops that which have slack value greater than or equal to uncertainty are selected first. This is an important consideration because only those flops can be used which do not violate the timing requirement of the design even after merging. The uncertainty value is taken as threshold in case there is any violation for this consideration. The flops which are constrained in the sdc file are also removed from the set of flops that can be merged. In this research, the flops that lie in false path or multicycle paths are also removed from the valid list of mergeable flip flops. Also, it is important to do the segmentation of the flops based on hierarchy to ensure that after merging, the placement of the flops is with minimum displacement.

CTS driven flip flop merging: In this algorithm, only those flip-flops which are part to the same clock tree path are merged, so as to ensure that functionality of design does not get disturbed even after the merging is done. All the mergeable single bit flip-flops are then associated with the two-bit merge flops that are available in the library. Then these flops are physically merged and placed in the region that lies at the mean position of flops being merged within the hierarchical module's boundary . The two bit merge flops are implemented after merging is as shown in Fig. 6 . The placement of standard cells is done based on

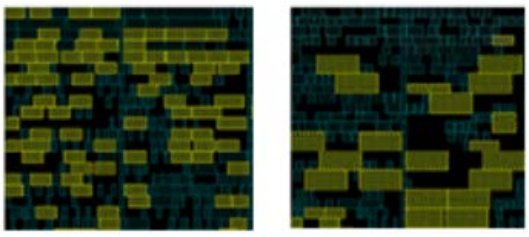

Fig. 6: Merging of single bit flops into 2 bit flops

Manhattan distance rule. Instead, using this algorithm, placement is explicitly directed by the Euclidean distance formula to place the cells after merging. The Euclidean distance calculates shortest path between two points while placing the cells, hence, minimizing the displacement.

RESULTS AND DISCUSSION

The low power implementation of DTMF chip is done using Cadence encounter and Si_2 standard CPF file is used to implement the low power rules. The merge flops implementation is as shown in Fig. 6. As shown in the figure, the area occupied by a single 2 bit merge flop is more than the single bit flop but due to reduction in number of inverters, the overall area gets reduced as shown in Table 2 for comparison between all the techniques. the multi Vt technique reduces leakage power by 40%, increasing the area by 2%. The MSV technique reduces leakage and dynamic power reasonably by 30 and 40%, respectively with a little impact on area (7%). Compared to the above two techniques Power gating technique has little effect on dynamic power consumption but largely reduces leakage power consumption by 96% because of which it is the most preferred method in lower technology designs. Though, this method increases area occupied by the standard cell by 14%. Table 3 is summary of merging technique. Due to the merging of flops, the total count of flip flops get reduced post merge. The efficiency of merging is calculated using the formula in Eq. 1:

$$\text{Merge\%} = \frac{\text{Number of flip flops after merging}}{\text{Total number of flip flops}} \quad (1)$$

Merging is said to be efficient if the merge percent is >80%. For the DTMF chip the merge percent is equal to 80% (612/862). By Shyu *et al.* (2013) and Santos *et al.* (2012) due to the displacement after merging the flip flops, the reduction in clock tree wirelength is suppressed by increase in signal wirelength. In the proposed algorithm, merging is only done for those flops which lie within the merge radius of 50 μm because the width of the region occupied by the largest hierarchical module is 50 μm. This ensures that the displacement after merging is restricted to the hierarchical module only.

Table 2: Merge statistics

Parameters	Before merging	After merging
Total number of flip-flops	862	612
Total signal and clock tree wirelength	55896 μm	39127.2 μm
Total clock tree capacitance (FF) (sink+buffer+wire)	1470	1367.1

Table 3: Comparison of area, leakage and dynamic power

Technique	Without low power	Multi V_t (Wei *et al.*, 1999)	Multi supply voltage (Mutoh *et al.*, 1995)	Power gating (Goran, 2014)	Proposed power gating using merge flops
Leakage power (mW)	0.004348	0.00254	0.00310	0.000176	4.758600
Dynamic power (mW)	7.273000	7.27300	4.36800	6.798000	0.000159
Area (μm^2)	538685.290000	547203.71200	578143.16800	666168.000000	59397600

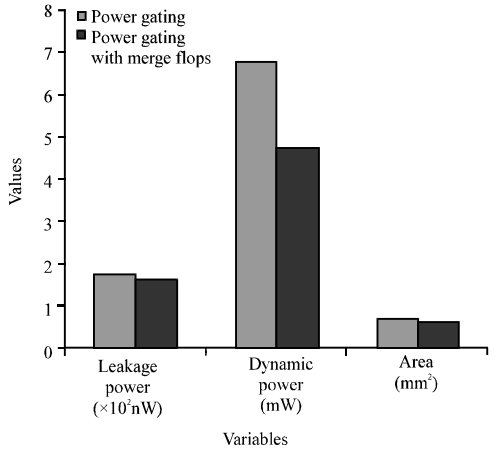

Fig. 7: Graph showing comparison between power gating and power gating with merge flops

Due to reduction in the number of flops, i.e., sink points, the clock tree wirelength also reduces and hence the sink capacitance. This results in decrease in routing wirelength as well as dynamic power consumption due to decrease in capacitance as shown in Table 3 for merge statistics.

Power gating is the most efficient technique for designs at lower technology nodes though the design has a considerable impact on the routing resources and area required. For the physical design of DTMF chip, the placement density after routing stage is 119% (666168/606656), which means power gating increases area by 14%. This is a critical issue as it means that cells sit outside the core boundary (Khosrow, 2007). To solve this issue, merge flops are used which decreases the placement density to 97.91% (593976/606656). According to Table 3, compared to power gating technique, the proposed technique using merge flops has the following advantages:

- Reduction of leakage power by 9.6%
- Reduction of dynamic power by 30%
- Reduction of area by 10%

Compared to Melikyan *et al.* (2016) which reduces the overall power consumption by 17% by employing power gating with multi V_t and MSV techniques, the proposed power gating technique with merge flops reduces the power only by 10% . Though by Wei *et al.*, (1999) the increase in area is 15% whereas the power gating technique proposed in this paper results in decrease in area by 10%. Hence, the power gating technique with merge flops is more efficient as it balances the tradeoff between area and power consumption as shown in Fig 7.

CONCLUSION

The results prove that the proposed technique reduces area by 10% compared to power gating technique at the routing stage thereby minimizing the use of routing resources. Apart from leakage power reduction, the proposed enhanced power gating technique also reduces dynamic power by <30%.

REFERENCES

Goran, P., 2014. A methodology for designing low power sensor node hardware systems. MSc Thesis, Brandenburg University of Technology Cottbus-Senftenberg, Senftenberg, Germany.

Khosrow, G., 2007. Physical Design Essentials. Springer, Berlin, Germany, ISBN:0-387-36642-3,.

Lakshmi, M.S., P. Vaya and S. Venkataramanan, 2011. Power management in SoC using CPF. Proceedings of the 3rd International Conference on Electronics Computer Technology (ICECT) Vol. 2, April 8-10, 2011, IEEE, Kanyakumari, India, ISBN:978-1-4244-8678-6, pp: 325-329.

Liu, S.S.Y., W.T. Lo, C.J. Lee and H.M. Chen, 2013. Agglomerative-based flip-flop merging and relocation for signal wire length and clock tree optimization. ACM. Trans. Des. Autom. Electron. Syst., Vol. 18, 10.1145/2491477.2491484

Melikyan, V., T. Hakhverdyan, S. Manukyan, A. Gevorgyan and D. Babayan, 2016. Low power open RISC processor with power gating, multi-VTH and multi-voltage techniques. Proceedings of the IEEE East-West Design & Test Symposium (EWDTS), October 14-17, 2016, IEEE, Yerevan, Armenia, ISBN:978-1-5090-0694-6, pp: 1-4.

Mutoh, S.I., T. Douseki, Y. Matsuya, T. Aoki and S. Shigematsu et al., 1995. 1-V power supply high-speed digital circuit technology with multi threshold-voltage CMOS. IEEE. J. Solid State Circuits, 30: 847-854.

PFI., 2008. A practical guide to low-power design-user experience with CPF. Power Forward Initiative, San Diego, California.

Priya, M.G. and K. Baskaran, 2013. Low power full adder with reduced transistor count. Intl. J. Eng. Trends Technol., 4: 1755-1759.

Santos, C., R. Reis, G. Godoi, M. Barros and F. Duarte, 2012. Multi-bit flip-flop usage impact on physical synthesis. Proceedings of the 25th Symposium on Integrated Circuits and Systems Design (SBCCI), August 30-September 2, 2012, IEEE, Brasilia, Brazil, ISBN:978-1-4673-2606-3, pp: 1-6.

Shyu, Y.T., J.M. Lin, C.P. Huang, C.W. Lin and Y.Z. Lin *et al*., 2013. Effective and efficient approach for power reduction by using multi-bit flip-flops. IEEE. Trans. Very Large Scale Integr. Syst., 21: 624-635.

Wei, L., Z. Chen, K. Roy, M.C. Johnson and Y. Ye *et al*., 1999. Design and optimization of dual-threshold circuits for low-voltage low-power applications. IEEE. Trans. Very Large Scale Integr. Syst., 7: 16-24.