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AWavelet-Based ADC/DAC Differential Nonlinearity Measurement Analysis

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Abstract: The quality of mixed signal devices such as ADC/DAC and their accurate performance in integrated circuits can be determined by testing static characteristics of differential nonlinearity behaviors. Because this testing is not trivial (it requires large number of samples) and extremely expensive, a new approached based on discrete wavelet transform is presented in this study. This proposed methodology of testing is especially, suitable for mixed signal devices due to the special properties of wavelet rescaling and shifting of a signal that allows for multiresolutions to lower number of samples needed to determine the DUT differential nonlinearity. Discrete wavelet transform has provided significant improvements over conventional testing techniques by decreasing computation complexity and reducing testing duration.

Key words: Analog-to-Digital Converters (ADCs), Digital-to-Analog Converters (DACs), differential nonlinearity testing, discrete wavelet transforms, properties, DUT

INTRODUCTION

Mixed signal devices provide the ability of operation across digital and analog domains by transforming analog/digital information into digital/analog format respectively (Mark, 2003; Burns and Roberts, 2001). While computers (PC) and Digital Signal Process (DSP) can only recognize and analyze digital data (discrete signal), human can only observe analog presentation of the signal. Therefore, mixed signal devices such as Digital-to-Analog Converters (DACs)/Analog-to-Digital Converters (ADCs) are the core elements of modern integrated digital systems and has wide uses ranging from simple audio circuit to most complicated precision instruments.

To ensure proper system performance, mixed signal devices need periodic testing and parameters evaluation. However, testing is extremely complex that cannot be easily modelled or predicted (Romas *et al*., 2016). It is time consuming and uses a lot of resources in today's equipment's (Yamaguchi and Soma, 1997; Gomez-Pau *et al*., 2015; Awada *et al*., 2010; Adamo *et al*., 2003; Vargha *et al*., 2001; Doyle *et al*., 2003; Marshall and Akujuobi, 2002; Akujuobi *et al*., 2007; Cherubal and Chatterjee, 2003; Serra *et al*., 2005; Raghuveer, 1998). In classical testing of mixed signal devices, it is common to include all codes produced by the devices for testing which may get unacceptably lengthy (Adamo *et al*., 2003; Vargha *et al*., 2001; Doyle *et al*., 2003) and higher computation complexity for higher resolution devices.

Generally, testing is based on examining output signal characteristics and measuring signal behavior. Signal analysis produces numbers of qualitative value that correspond to signal characteristics that can be used to determine the performance of DUT converters. Signal analysis can fall within one or more of three distinct techniques as follow:

Direct Current (DC) analysis: This is used to determine static characteristics of DUT such as code output voltage level, offset voltage, FSR.

Time domain analysis: Includes slew rate, pulse width and peak to peak voltage.

Frequency domain analysis: It determines frequency components such as tones, harmonics, noise, SNR and signal distortion.

In addition to these different techniques of signal analysis, wavelet transform which is traditionally used for data compression (Raghuveer, 1998; Adamou-Mitiche *et al*., 2016; Oliver *et al*., 2005) can be used in signal analysis due to its special properties of dilation and translation. In contrast with sinusoids fourier

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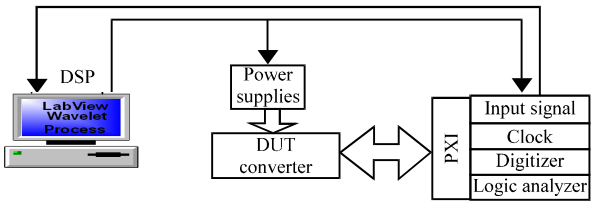

Fig. 1: Proposed DSP analysis using wavelet transform

transform, wavelets are localized in time and frequency domain which is suitable for non-stationary signal processing Oliver *et al* ., 2005 and other applications of signal diagnosis such as scaling, compression, extracting, de-noising and ability to capture the energy in few transform values (Akujuobi and Awada, 2008).

These properties of wavelets make it desirable in the evaluation of particular characteristic of mixed signal converters such as linearity performance with less data samples and less process complexity.

Static characteristics of mixed signal converters are usually one of the most important but not the sole source of defining errors and based on measuring the deviation of DUT output from ideal line (Adamo *et al*., 2003; Akujuobi *et al*., 2007). This task is not trivial, since, comparing the output with the input signal does not work (Awada *et al*., 2010). In this research, the focus is to enhancing mixed signal nonlinearity testing by developing wavelet testing algorithms for DSP and employing and automated testing control and data acquisition as shown in Fig. 1.

Literature review: Several works have been done to enhance statistical testing of ADC and DAC. Some focused on improving conventional methods such as Fourier transform and sinusoidal histogram (Adamo *et al*., 2003; Cherubal and Chatterjee, 2003; Xu, 1999; Lee *et al*., 2008; Wagdy and Awad, 1991). Histogram is the traditional method for obtaining noise free statistical characteristic measurements (Awada *et al*., 2010). However in histogram, most samples occur near the ends of histogram and large number of samples must be collected to increase the height of bins around the center (Burns and Roberts, 2001; Awada *et al*., 2010; Vargha *et al*., 2002). Even though, it is much faster than older Servo-loop, it is still not fast enough (Adamo *et al*., 2003). Fourier transform is based on mean value of collected samples to estimate ADC characteristics and any deviation caused by harmonics components hidden in noise floor, quantization effect and bit error can be summed into the total noise power which can affect the estimation of ADC characteristics (Romas *et al*., 2016; Awada *et al*., 2010).

Other methods have been proposed to reduce the number of input codes and reduce the necessary time for static testing of DAC. By Vargha *et al*. (2002), a technique was proposed to shorten the testing time of DAC by modeling reducing order model of DAC. By reducing the number of measurement points and using the collected points and DAC model to estimate the overall statistical characteristics. DAC model must feature much less than 2^n codes than that still captured for full behavior of DAC. Also, prior knowledge of error behavior of the DAC is needed to be included in the model. This approach requires appropriate mathematical simulated models of DAC to define the influence of each code on its actual output voltage (Balestrieri *et al*., 2006; Vargha *et al*., 2001). In the work of modeling, Vandenbussche *et al*. (1999) proposed simulation model of DAC output signal. Modeling was based on strictly complex mathematical interpretation. By Wikner and Tan (1999) DAC was modeled to show the effect of parasitic element and DAC components mismatching on the converter performance. However, other noise sources such as power supply and other hardware inputs were not included (Doyle *et al*., 2003).

By Jiang *et al*. (2004), the researcher proposed the uses of Dynamic Element Matching (DEM) in current steering and non-linearity testing of DAC. DEM reduce the effect of components mismatching by dynamically rearranging the interconnections of current sources. However, this design enable multiple analog outputs for one input code and the distribution of all possible output voltage are uniform except at the two ends (Xing *et al*., 2005). This method of rearranging interconnection of matching sensitive components is valid when enough analog output is available for one digital code which involves high complexity in control logic and longer testing time. On the other hand, others have focused on applying new testing techniques such as wavelet transforms (Awada *et al*., 2010; Marshall and Akujuobi, 2002; Gandelli and Ragaini, 1996). Through simulation process, wavelet transforms have shown improvements and very satisfactory results.

By Yamaguchi and Soma (1997) and Awada *et al*. (2010) wavelet transform was used to simulate ADC testing static and dynamic parameters and by Doyle *et al*. (2003), wavelet was used for DAC modeling. However, no serious work has been done to explore the strength of employing wavelet transform algorithms in real time automated testing of ADCs and DACs performance and parameters.

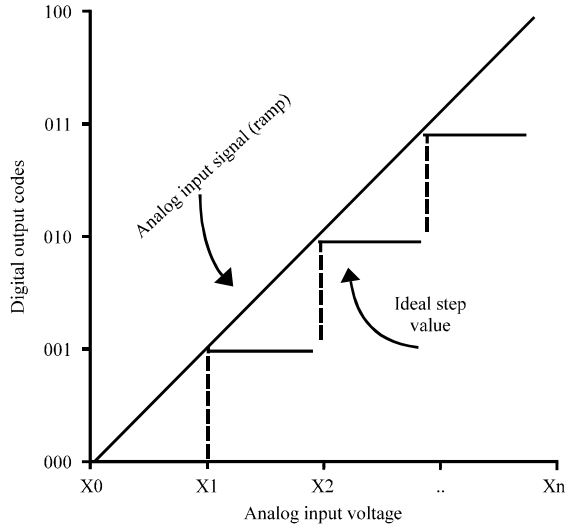

Fig. 2: Ideal ADC transition codes

Static characteristics of differential nonlinearity: Testing ADC non-linearity is basically evaluation DUT in term of analog input signal with respect to the corresponding increments output digital codes (Mark, 2003; Burns and Roberts, 2001). ADC is many to one mapping device. This means for ideal ADC, analog input is divided into interval of equal range of voltage increments that correspond to a specific output digital code as shown in Fig. 2. Width of increments is determined by the ADC one Least Significant Bit (1LSB) step size.

1LSB as shown in Eq. 1 is special property of the DUT and based on total output amplitude span of Full Scale Range (FSR) as in Eq. 2 and the DUT number of bits:

$$1LSB = \frac{FSR}{2^n - 1} \quad (1)$$

where n is the converter number of bits:

$$FSR = \text{Max voltage} - \text{Min voltage} \quad (2)$$

Thus, in actual device, analog step size varies due to conversion process, noises, quantization error and bits distortion caused by nonlinear circuit behavior and component mismatches (Yamaguchi and Soma, 1997). Since, Differential Nonlinearity (DNL) error can be expressed as the difference between the ideal and the measured code transition for successive code of the device under test ADC (Mark, 2003; Burns and Roberts, 2001; Akujuobi *et al*., 2007) as shown in Eq. 3 and Fig. 3.

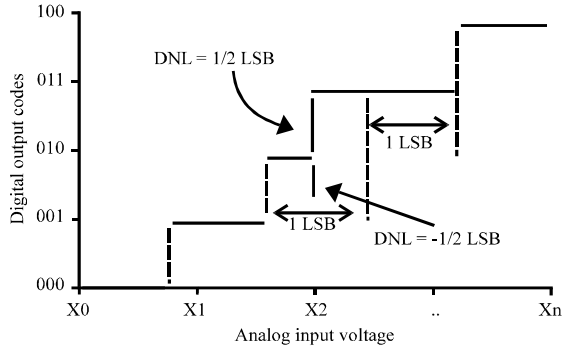

Fig. 3: ADC Differential Nonlinearity (DNL)

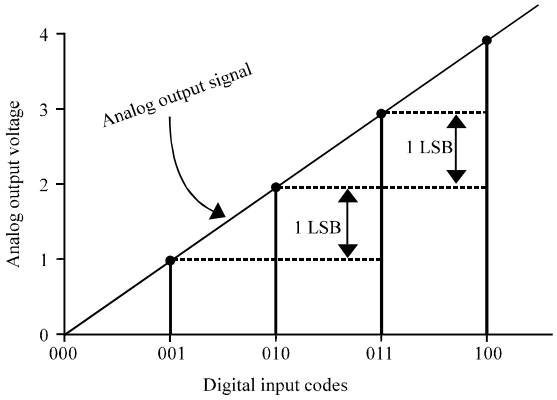

Fig. 4: Ideal DAC output codes

$$DNL(i) = \frac{\text{uppercode} - \text{lowercode}}{1LSB} - 1LSB \quad (3)$$

Ideal ADC has uniform distance between codes of exactly 1LSB and zero DNL error. However, this is not the case for actual performance.

DAC performance specified according to number of bits and output voltage range (FSR). While ADC is many to one mapping, DAC on the other hand is one to one mapping. Each digital input code corresponds to a specific output voltage with equal spacing as shown in Fig. 4.

Increment spacing based on the device LSB. However, in real time DAC operation, analog step size varies from ideal expected values as shown in Fig. 5.

DAC DNL error also can be defined as the difference between the ideal and measured output responses for successive output codes. An ideal DAC response would have analog output values exactly 1LSB apart and DNL 0LSB (Mark, 2003; Burns and Roberts, 2001; Vargha *et al*., 2002) as in Eq. 2. However, due to noise and voltage offset error (Mark, 2003; Xing *et al*., 2005), DAC output

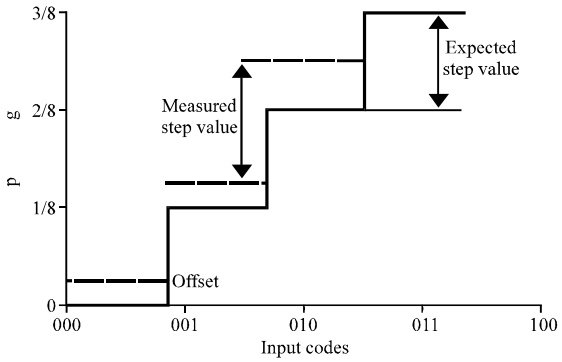

Fig. 5: DAC output deviation from ideal transition

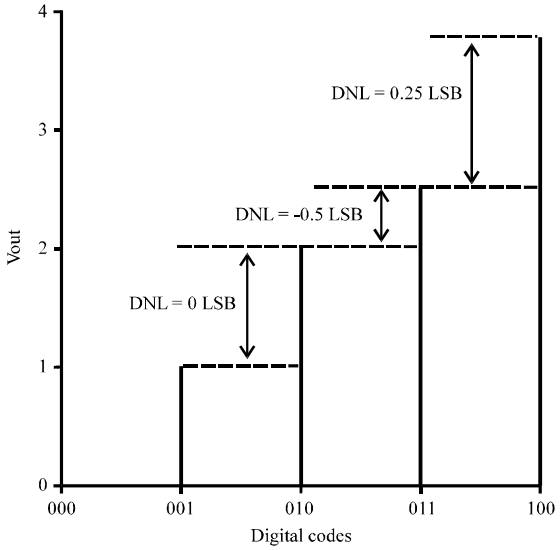

Fig. 6: DAC differential non-linearity

voltage will inherent non-linearity errors as in Fig. 6. Such errors distort the signal and degrade the performance of DAC (Mark, 2003; Burns and Roberts, 2001; Xing *et al*., 2005).

As seen in Eq. 3 an intensive complex calculation is involved to compute for DNL by including all codes, especially with higher resolutions DAC.

Wavelet transform: An ADC output waveform signal in time domain is shown in Fig. 7. In most cases for better characterization of signal components, signals are transformed and represented in a different domain instead of the time domain with no changes to signal information that help detecting fault frequencies hidden within waveform data (Bayram and Seker, 2016).

This kind of transformation allows for obtaining further information that is not readily available in raw signal. One of the most common transformation tools used is the fourier transform which is used particularly to represent a periodic signal in frequency domain through a summation series of sine and cosine. In fourier transform, a signal expressed in frequency domain (frequency vs. Amplitude) to determine all frequency components within a signal with no time representations (Keinert, 2003) as in Fig. 8.

Non-stationary signal viewed in frequency domain becomes distorted and added noise where it should not be due to the fourier assumption of the periodic nature of the signal which is not always the case. Distortion and lack of time representation obstruct the conceptual of when a particular signal accrues. Therefore, Short Time Fourier Transform (STFT) became very significant to break-up the signal into multiple windows of periodic signals in order to apply fourier transform (Stephane, 2001) as in Fig. 9.

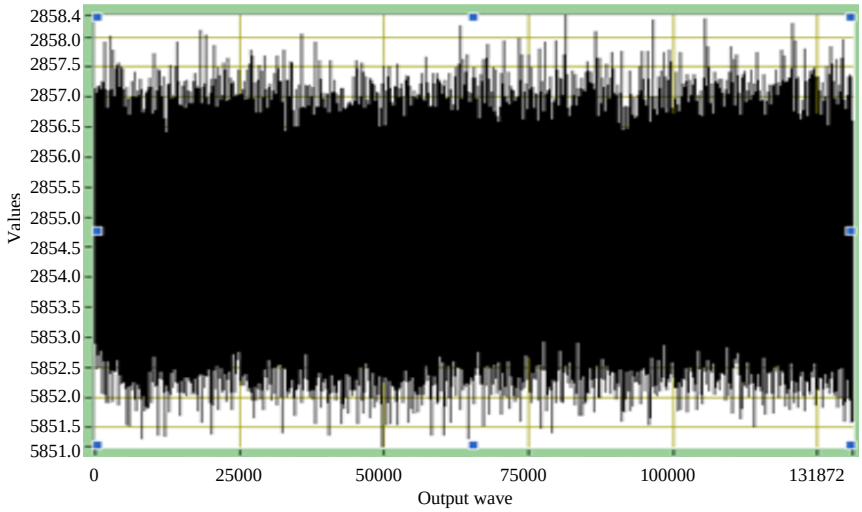

Fig. 7: ADC output waveform at 10 MHz in time domain

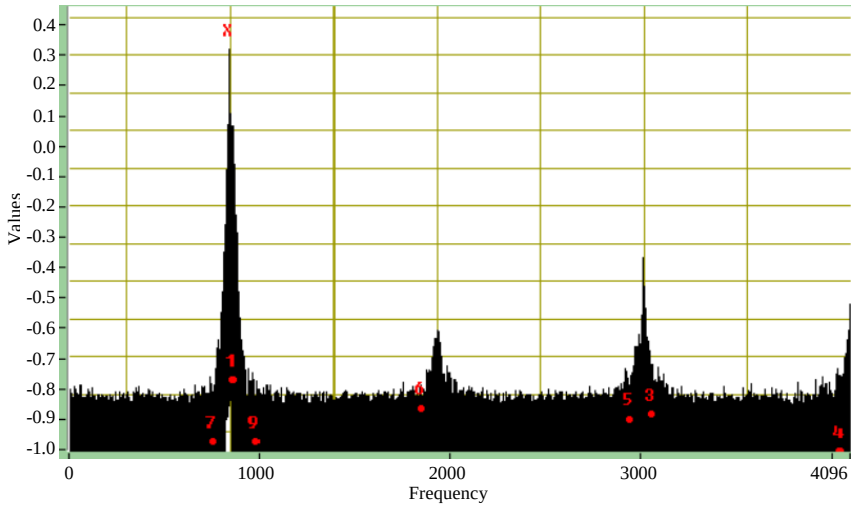

Fig. 8: Waveform at 10 MHz with harmonics in frequency domain

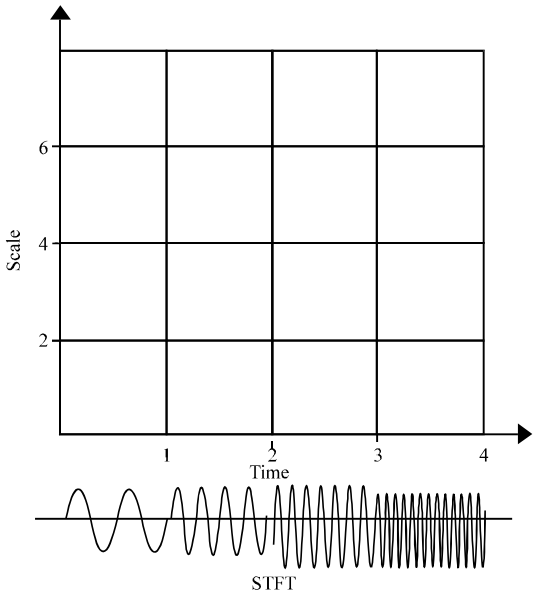

Fig. 9: STFT windowing signal analysis at different frequencies

However, the content of the signal need to be determined to make appropriate windowing for a signal to become stationary. As a result, transformation tools with adjusted window sizes are used to transform and analyze a signal. This capability of scaling, stretching and compressing called wavelet transform (Keinert, 2003; Stephane, 2001; Rioul and Vetterli, 1991; Kollar and Blair, 2005; Ruskai, 1992).

The objective of wavelet transform is to achieve a localized space frequency with the ability to determine

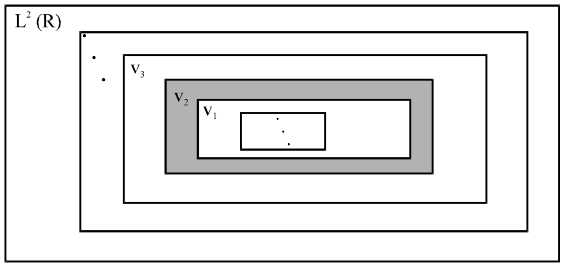

Fig. 10: Multiresulotions based on subspaces of the signal that allows zoom in and out of the signal components

the position of frequency components (Keinert, 2003; Rioul and Vetterli, 1991). Wavelet is based on scaling function (approximation v) and mother wavelet function Ø (details w). Scaling function as shown in Eq. 4:

$$\phi_{r,s}(x) = 2^{r/2}\phi(2^r x\text{-}s) \quad (4)$$

Where:

x = A continuous function
r = Scaling integers
s = Shifting integers

Used to increase sequences of closed subspaces $\{\bullet_j\}\bullet Z$ which approximates $L^2(R)$ (Ruskai, 1992). By using all possible values of r and s, the entire square integral real space $L^2(R)$ can be covered as in Eq. 5 and Fig. 10 to allow for multiresulotions and break down signal components (Raghuveer, 1998; Ruskai, 1992):

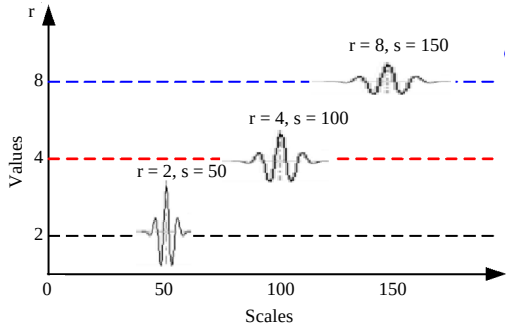

Fig. 11: Wavelet is shown in three different scales and translation

$$\{0\} \rightarrow, \ldots, \subset V_{-1} \subset V_0 \subset V_1 \subset, \ldots, \rightarrow L^2(R) \quad (5)$$

With the function of low pass flitter of looking at one subspace, scaling function is given by Eq. 6:

$$(x) \quad \sum_n h \ (n)\sqrt{2} \ (2x\text{-}n) \quad (6)$$

Where:
n = Shifting parameter
h = Shift coefficient

High pass filter function can cover the difference between subspaces V_2, V_1 for example as the shaded area in Fig. 10. This leads to $\{\bullet_{r,s}(x)\}$ wavelet function that can be defined as in Eq. 7:

$$\psi_{r,s}(x) = \frac{1}{\sqrt{s}}\psi\left(\frac{x\text{-}r}{s}\right) \quad (7)$$

Different type wavelet transforms have been used in various fields of signal processing (Oliver *et al*., 2005; Riouel and Vetterli, 1991; Kollar and Blair, 2005). Wavelet special properties of dilation and translation (Yamaguchi and Soma, 1997; Awada *et al*., 2010; Akujuobi *et al*., 2007; Keinert, 2003; Riouel and Volume, 1991) allow creating different scaled and shifted version of the signal to identify time duration and frequency bandwidth. Signal usually made of low frequency and high frequency components. Low frequency components are slow with time and require fine frequency resolution while high frequency components are fast in time and require fine time resolution. As illustrated in Fig. 11 and 12, wavelet with small scale has short time duration and wide frequency bandwidth while wavelet with large scale has long time duration and smaller frequency bandwidth.

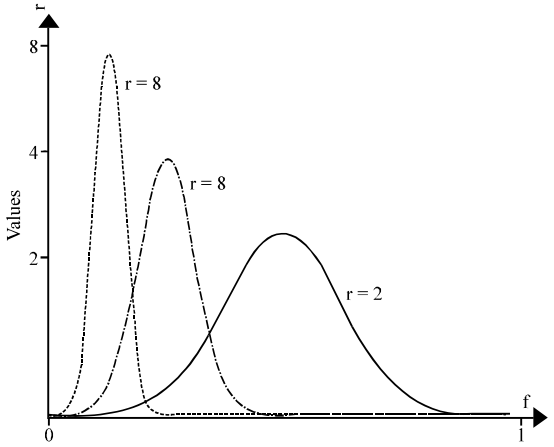

Fig. 12: With their power spectra representation

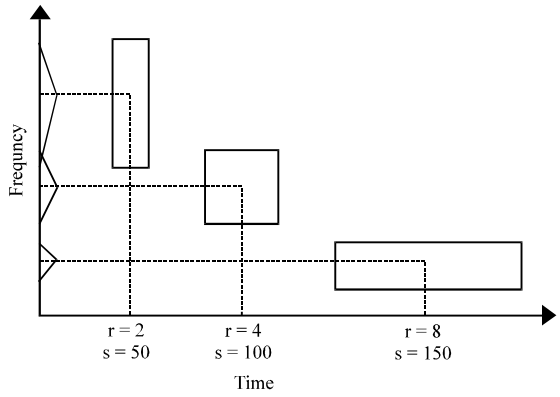

Fig. 13: Time-frequency resolution of different scales and translation wavelet

From Fig. 11 and 12, time duration and frequency bandwidth determine wavelet time and frequency resolution. For example in Fig. 13, wavelet with small scale has fine time resolution and coarse frequency resolution which enable the detection of fast frequency component in the signal. Mean while, wavelet with large scale has fine frequency resolution and coarse time resolution which enable the detection of slow frequency component in the signal.

As a result, wavelet function can be resized by using summation of shifted version of scaling function of the next higher space. For example in subspace $\{\bullet_j\}\bullet Z$. Let $\bullet_0 \bullet \bullet_1 \bullet \bullet_2$ where $\bullet_2$ is the complete signal and $\bullet_0, \bullet_1$ are higher spaces.

This special properties of scaling, dilation and translation of a signal allows for windowing resizing analysis (Fig. 14) by shifting the signal in time domain (X-axis) and the rescaling (expand or compress a signal on Y axis).

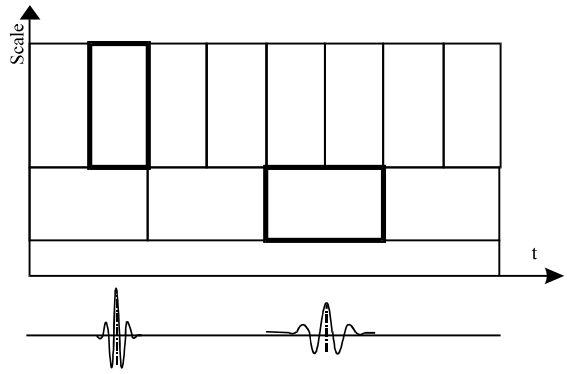

Fig. 14: Wavelet windowing signal analysis at different frequencies

Discrete wavelet transform and minimization of algorithms: Discrete Wavelet Transforms (DWT) computation is based on predetermined lowpass and highpass coefficient filters for each particular mother wavelet. In this research, DWT algorithm was used to decompose the DUT converter output signal by first utilizing filter banks of highpass and lowpass and down-sampled by factor of 2 (decimation) (Yamaguchi and Soma, 1997; Awada *et al*., 2010; Marshall and Akujuobi, 2002; Riouel and Vetterli, 1991; Ruskai, 1992).

By assuming an output discrete signal $S_n = \{S_{nk}\}$, decomposition of the signal can be shown in Eq. 8 and 9 for approximation and detail, respectively:

$$s_{n-1,j} = \sum_k \tilde{h}_{k-2j} s_{nk} \quad (8)$$

$$d_{n-1,j} = \sum_k \tilde{g}_{k-2j} s_{nk} \quad (9)$$

However, decomposition of a signal consists of two major functions. Signal convolution with wavelet coefficients as in Eq. 10 and 11:

$$(\tilde{h}(-)*s_n)_j = \sum_k \tilde{h}_{-(j-k)} s_{nk} \quad (10)$$

$$(\tilde{g}(-)*s_n)_j = \sum_k \tilde{g}_{-(j-k)} s_{nk} \quad (11)$$

This convolution is basically wavelet filtering. Followed the convolution, signal downsampled by 2 as in Eq. 12 and 13 for approximation and detail coefficients, respectively:

$$s_{n-1} = (\downarrow 2)(\tilde{h}(-)*s_n) \quad (12)$$

$$d_{n-1} = (\downarrow 2)(\tilde{g}(-)*s_n) \quad (13)$$

By applying filtering and decimation of 2 at each decomposition level, frequency characterizations are passed and number of samples rate reduced by half (half the frequency band). Starting with the largest scale (the original signal), bandwidth become a multiple of halves at the high and low pass filters for fast algorithms of computational and implementation process.

MATERIALS AND METHODS

Testing methodology: By Awada and Akujuobi (2007) 12 bits TI ADC (ADS5410) was tested for instantaneous DNL value using DWT. Testing set-up is as shown in Fig. 15.

Mean while in testing DAC as shown in Fig. 15, pattern generator was used to produce a digital form signal. DAC analog output signal was digitized through higher bit ADC (at least 4 bits higher than DUT DAC to achieve linearity measurement accuracy of 1/16 the DUT LSB) (Mark, 2003) with less error distortion. The digitized DAC output signal was captured and analyzed as shown in Fig. 16.

Computation technique: High-resolutions 14 bits TI DAC (DAC2904) was used for this research. This testing of DAC non-linearity performance, digital ramp pattern as shown in Fig. 9 was applied as DAC input. DUT DAC acquired response was compared to an ideal response. Multiple cycles of ramp signal was generated but only one complete signal was acquired for analysis by locating the minimum and maximum value in increasing ramp cycle using derivative analysis as shown in Fig. 17.

Ideally, DAC should have a negligible output deviation from strait line and 0 offset voltage (Mark, 2003; Burns and Roberts, 2001). However, in non-ideal environment, DAC analog output contains errors that distort the output signal as shown in Eq. 14:

$$\bar{x}(t) = x(t)+e \quad (14)$$

x(t) = Original ramp value
e = Error value

By capturing DAC output x(t) and digitize it by 20 bits digitizer (6 bits higher than the DUT DAC, 1/64 of original LSB), we can call the new DAC digitized signal as S_n.

DWT algorithm was applied to decompose S_n using multi-resolution technique as shown in study (V).

S_n is a combination of low and high frequency components. Low frequency components are stationary over a period of time while high frequency components

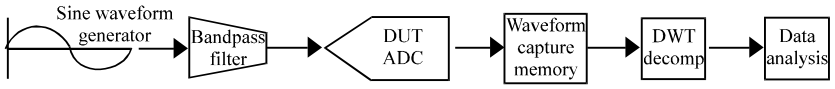

Fig. 15: Model setup for automated ADC wavelet testing

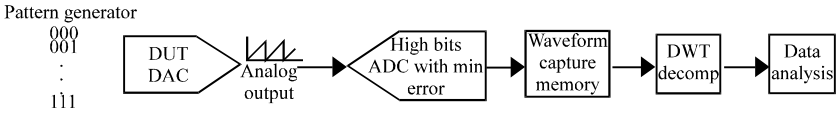

Fig. 16: Model setup for automated DAC wavelet testing

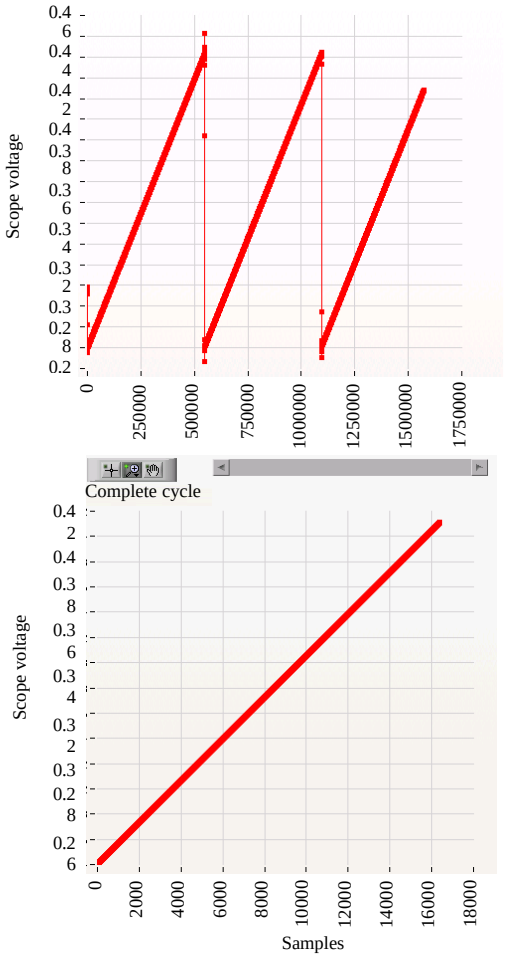

Fig. 17: DAC output at 100 kHz ramp signal

are noisy. In wavelet bank of filters, lowpass provide approximation coefficients and high pass provide detail coefficients. To obtain signal coefficients, a signal convolution (filtering) operation was performed to obtain lowpass and highpass as shown in Eq. 15 and 16, respectively.

$$\begin{bmatrix} \vdots \\ s_{n-1,-1} \\ s_{n-1,0} \\ s_{n-1,1} \\ \vdots \end{bmatrix} = \begin{bmatrix} \cdots & \cdots & \cdots & & & & \\ \cdots & \tilde{h}_{-1} & \tilde{h}_0 & \tilde{h}_1 & \tilde{h}_2 & \cdots & \\ & \cdots & \tilde{h}_{-1} & \tilde{h}_0 & \tilde{h}_1 & \tilde{h}_2 & \cdots \\ & & \cdots & \tilde{h}_{-1} & \tilde{h}_0 & \tilde{h}_1 & \tilde{h}_2 \\ & & & & \cdots & \cdots & \cdots \end{bmatrix} \begin{bmatrix} \vdots \\ s_{n,-1} \\ s_{n,0} \\ s_{n,1} \\ \vdots \end{bmatrix} \quad (15)$$

$$\begin{bmatrix} \vdots \\ s_{n-1,-1} \\ d_{n-1,-1} \\ s_{n-1,0} \\ d_{n-1,0} \\ s_{n-1,1} \\ d_{n-1,1} \\ \vdots \end{bmatrix} = \begin{bmatrix} \cdots & \cdots & \cdots & & & & \\ \cdots & \tilde{h}_{-1} & \tilde{h}_0 & \tilde{h}_1 & \tilde{h}_2 & \cdots & \\ \cdots & \tilde{g}_{-1} & \tilde{g}_0 & \tilde{g}_1 & \tilde{g}_2 & \cdots & \\ & \cdots & \tilde{h}_{-1} & \tilde{h}_0 & \tilde{h}_1 & \tilde{h}_2 & \cdots \\ & \cdots & \tilde{g}_{-1} & \tilde{g}_0 & \tilde{g}_1 & \tilde{g}_2 & \cdots \\ & & \cdots & \tilde{h}_{-1} & \tilde{h}_0 & \tilde{h}_1 & \tilde{h}_2 \\ & & \cdots & \tilde{g}_{-1} & \tilde{g}_0 & \tilde{g}_1 & \tilde{g}_2 \\ & & & & \cdots & \cdots & \cdots \\ & & & & \cdots & \cdots & \cdots \end{bmatrix} \begin{bmatrix} \vdots \\ \vdots \\ \vdots \\ s_{n,-1} \\ s_{n,0} \\ s_{n,1} \\ \vdots \\ \vdots \\ \vdots \end{bmatrix} \quad (16)$$

From the highpass filter, detail coefficients was obtained as in Eq. 17 and down sampled by 2 by taking the odd values as shown in Eq. 18 to end up with 2^n total number of samples, half of the original data):

$$(\ldots, d_{n-1,-1} d_{n-1,0}, d_{n-1,1}, \ldots,) \quad (17)$$

$$(\ldots, d_{n-1,-3}, d_{n-1,-1} d_{n-1,1}, d_{n-1,3}, \ldots,) \quad (18)$$

The collected detail coefficients in the first multiresulotion are used aging for 2nd multiresulotion by repeating (Figure 15-18).

In estimating for instantaneous DNL, using the concept of estimating DNL as in (Yamaguchi and Soma, 1997; Akujuobi *et al*., 2007), the difference between adjacent instantaneous magnitudes of the detail coefficients $d_{n-1,j}$ at the 2nd level of multiresulotion is used as applied in Eq. 19 to compute for instantaneous DNL:

$$DNL(n)=\frac{\max\left\{\left\|d_{n-1,j}\right|-\left|d_{n-1,j+1}\right\|\right\}}{\Delta_{Ideal}}-1 \quad (19)$$

where • $_{ideal}$ is ideal LSB

By Yamaguchi and Soma (1997), Awada *et al.* (2010) and Akujuobi *et al.* (2007) and since, the data used at the 2nd level of wavelet decomposition instantaneous DNL can be estimated by Eq. 20:

$$DNL(n)=\frac{2}{\Delta_{ideal}}\max\left\{\left|\frac{\Delta[n]}{2}\right|\right\}-1 \quad (20)$$

where• $[n] = |d_{n-1,j}|-|d_{n-1,j+1}|$

RESULTS AND DISCUSSION

The new computation algorithm was implemented into a system prototype of LabView application and the effectiveness of this proposed technique was tested by measuring the static characteristic DNL of ADC and DAC. Testing methodology as shown in Fig. 14 and 15 were used in order to collect and analyze DUT output signal. A picture of arranged bench prototype testing set-up is shown in Fig. 18.

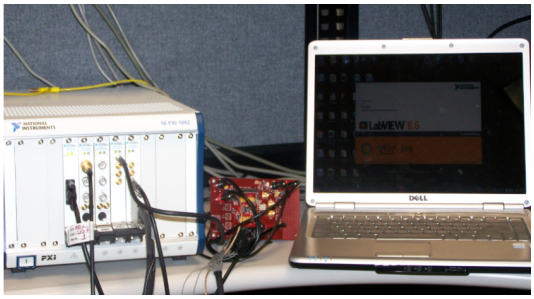

Fig. 18: Bench prototype testing set-up

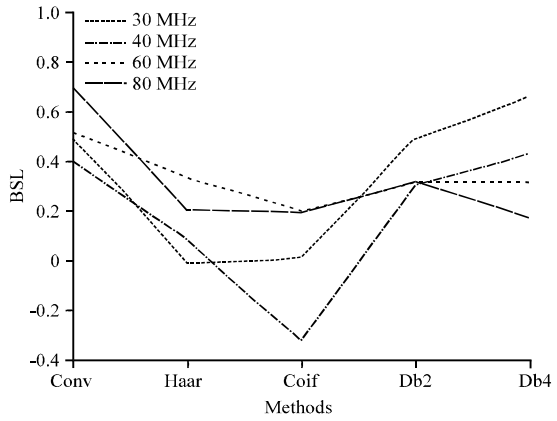

Fig. 19: The DNL values for Table 4

By Akujuobi *et al.* (2007), TI 12 bits ADC (ADS5410) was used as DUT to evaluate static characteristic DNL. DUT output waveform as shown in Fig. 7 was captured and analyzed using total of 131072 sample data point and employing conventional method. Meanwhile in wavelet decomposition process, ¼ of the total collected data was used to estimate for DNL. Testing results for ADC DNL using wavelet transform and conventional technique Vs. device specifications are shown in Table 1 and 2 and Fig. 19.

DAC DNL was also, evaluated using conventional technique as shown in Fig. 20 and new proposed wavelet transform (Fig. 21)

Results were compared and checked with the device specifications are shown in Table 3 and 4 and Fig. 22. Total of 16383 samples were used in conventional vs. 4099 samples in wavelet computation for DNL.

Wavelet transforms have shown improvements over the conventional testing techniques of testing ADC and DAC static parameters (DNL) by reducing the number of sampling data and multiplication complexity. As indicated from testing process, wavelet transforms algorithms reduced the number of compiled data by 75% of collected data samples which in return reduces the data storage space requirements by 3/4 the storage area and shorten test duration from 312 msec in conventional testing to 134 ms using wavelet algorithms.

Table 1: ADS5410 DNL specification

Parameter	Condition	MIN	TYP	MAX	Unit
Resolotion	-	-	12	-	BITS
Staric accuracy DNL	-	-0.9	±0.5	1	LSB

Table 2: ADC DNL values at various sampling frequencies and analysis

		Wavelet			
Sampling frequency	Conv.	Haar	Coiflet1	Db2	Db4
80 MHz	0.69	0.204	0.19	0.32	0.17
60 MHz	0.51	0.33	0.2	0.31	0.31
40 MHz	0.4	0.09	-0.32	0.3	0.43
30 MHz	0.49	-0.01	0.01	0.49	0.66

Table 3: DAC DNL values at various frequencies and analysis techniques

		Wavelet			
Testing frequency	Conv.	Haar	Coiflet1	Db2	Db4
200 kHz	3.211	0.543	0.46788	0.681	0.5903
150 kHz	2.481	0.7490	0.7127	0.759	0.2255
100 kHz	2.298	0.692	0.75529	2.013	0.1892
50 kHz	2.90	1.027	0.8865	2.482	0.9023

Table 4: DAC2904 DNL specification

Parameter	Condition	Min.	Types	Max.	Units
Resolotion	-	-	14	-	BITS
Staric accuracy DNL	-	-	±4.0	-	LSB

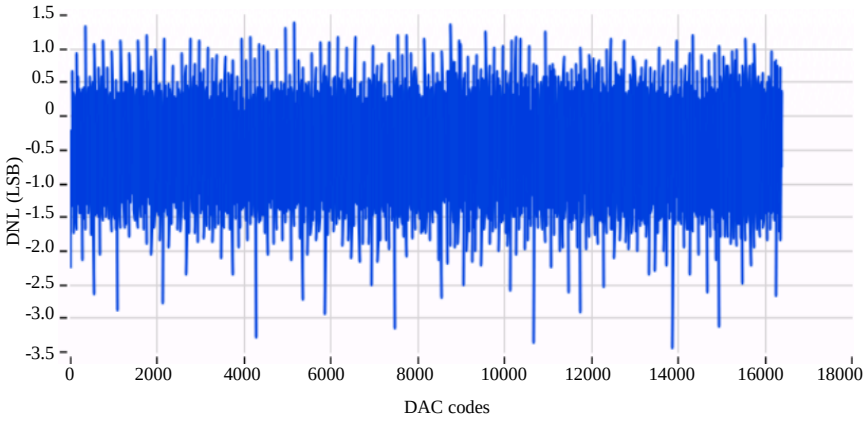

Fig. 20: DAC DNL computation

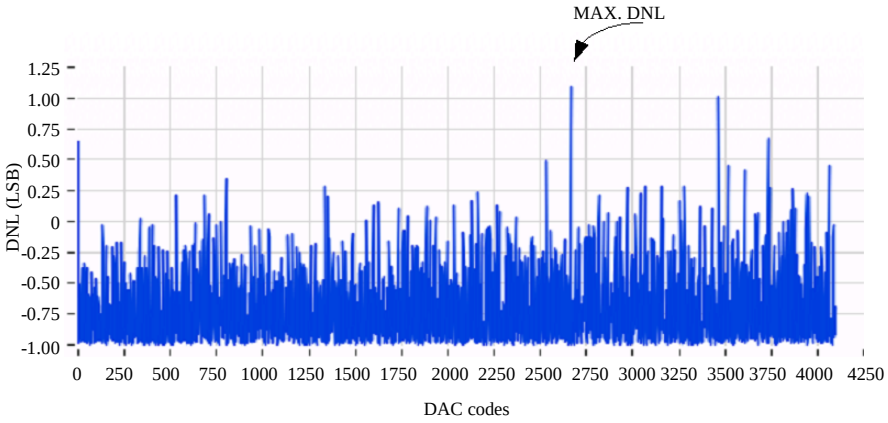

Fig. 21: DNL wavelet based computation

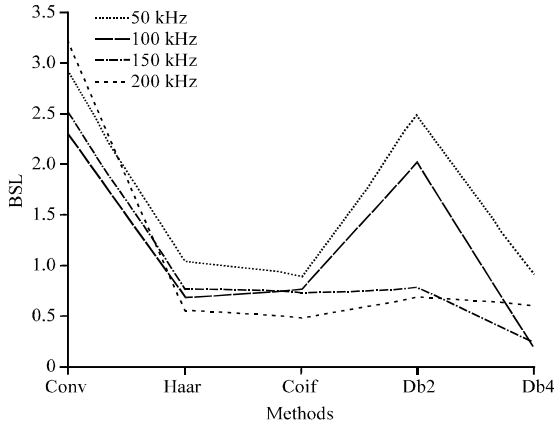

Fig. 22: The DNL values for Table 2

CONCLUSION

New method of testing mixed signal converters was presented to show the ability of wavelet to analyze converters output signal to identify bit errors due to signal distortions, noise, etc. which degrade the performance converters in wide range of application. This research, present the benefit of wavelet features and efficient algorithms to decrease sample data in conjunction with oversampling for faster testing process, less cost and accurate reading, especially with the incredible growing demands for higher speed and resolution converters with the ability for built-in self test impeded algorithms.

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