Journal of Engineering and Applied Sciences 13 (16): 6866-6872, 2018
ISSN: 1816-949X

Design and Simulation of a New Seven Levels Inverter for Renewable Energy Sources

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Abstract: In multi-level inverters design, the number of DC sources and switching devices are the key factors for designing of this kind of inverters. This study presents a new design of a seven levels inverter by using of single DC source with three series connected capacitors that are in parallel with the DC source. Only 8 IGBT switching devices are required for the design. A new method of modulation is presented to get the logic expression that makes the required pulses to drive the IGBT switches of the proposed inverter with a prior assumption that the frequency of each carrier is the same as the frequency of the reference or modulating signal to get the logic expression for each switching device. Later, the frequency of the carriers can be increased to a desired level for a proper performance of the inverter. In the proposed resarch, the fundamental frequency is 50 Hz and the carriers frequency is 3 kHz. The proposed inverter is simulated successfully by using MATLAB Simulink where low total harmonic distortion was achieved for its output voltage and current.

Key words: Inverter, multi-levels, seven levels, POD, APOD, THD

INTRODUCTION

With the increasing of utilization of the renewable energy sources, the demand on the multi-level inverters is also increased. Since, it gives better performance with high efficiency and low total harmonic distortion. Many researches have published many papers about different constructions, designs and or modulation techniques for the multi-level inverters. Some of these designs may require several DC sources and the other may need only single DC source. The main designs of the multi-level inverter are the diode clamed, flying capacitor and cascade H-bridge. Some of these designs which can be classified as a compromise between the flying capacitor and the cascaded H-bridges topologies. It makes seven levels inverter by using a single dc source with an auxiliary capacitor. The modulation is made by using of 6 carriers (Ounejjar *et al*., 2011). Other researchers used a trapezoid signal as a modulating (reference) signal with four carriers to make different modulation techniques such as Phase Disposition PD, Phase Opposition Disposition POD and Alternative Phase Opposition Disposition APOD (Bensraj and Natarajan, 2010). All of these modulations are made for cascade 5 levels inverter which uses a couple of DC sources. The multi carriers and different shapes of reference signals are ways to reduce the total harmonic distortion. Another method which is Selected Harmonic Elimination (SHE) is used by Gobinath *et al*. (2013) for cascade seven levels inverter. The SHE method uses a calculation by Newton-Raphson numerical analysis to detect the angles that are used to make the change in voltage levels to eliminate the first three harmonics. But for more harmonics elimination, SHE method needs long and complex computer program with many iterations for making the calculations. The research that was presented by Choi and Kang (2015) a new design was made to make seven levels inverter by using of single DC source with a group of three series connected capacitors that are parallel to the DC source. In this design, the modulation is made by using of three carriers but with some of predetermined Periods (P_n) for the changing in voltage levels. For seven levels inverter the number of these periods is 10. Another design of the seven levels inverter is made by using eight switching devices (Hsieh *et al*., 2016). The modulation is made by using 6 carriers which are compared with a sinusoidal modulating signal. The logic expression is made with combination of predetermined periods and the modulated signals. In another research, the effect of over modulation is studied for three phases boost inverter to increase the inverter's output voltage with lower THD results (Elserougi *et al*., 2013). The over modulation means, the peak amplitude of modulating signal should be higher than the carrier signal for some period of time. In this study, a new design of seven levels inverter based on the construction of full bridge inverter and modified diode

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clamped multi-level inverter (Luo and Ye, 2010;Mekhilef and Masaoud, 2006; Rashid, 2007). In the new design, the number of used carriers is 3 only. Also, there will be no dependency on the predetermined periods (P_n) in making of pulse width modulation techniques for each switching device. The effect of the over modulation technique is also, studied and compared at different amplitudes of the modulating signal with THD values to show its impact to reduce the THD. The paper is arranged as follows: an Introduction, description of the proposed inverter circuit inverter's modes of operation, the used pulse width modulation technique, new method of making the logic expression for each IGBT switch, simulation results, impact of over modulation technique for reduction of the THD and conclusion.

THE PROPOSED SEVEN LEVELS INVERTER

The proposed multi-level inverter is 7 levels inverter. It contains a single DC source (V_{dc}) with three capacitors that are connected in series with each other and in parallel with the DC source to make a voltage divider across the dc source. The inverter circuit is mainly composed of a set of IGBT switches to make the desired switching at different levels of the output voltage. The number of the IGBT switches is eight and each one with anti-parallel diode. Four of these switches are forming full bridge inverter circuit which numbered as S1-S4 to make the output voltage levels of $\pm V_{dc}$ and 0 V. The rest of the switches are combined with diodes in series with them and also with some of the switches of the portion of the full bridge circuit to make the output voltage at levels of $\pm 1/3$ and $\pm 2/3$ of V_{dc} as shown in Fig. 1.

Modes of operation of the proposed seven levels inverter: There are eight modes of operation of the proposed 7 levels inverter. In Fig. 2, the red path represents the power flow at each mode ofoperation which can be explained in the following lines. It can be noted that the switch S4 is on for the first half cycle of the fundamental frequency and S2 is on at the other half of it. The first mode is mode 1, this mode is happening when both S1 and S4 switches are on where the output voltage is at level of $+V_{dc}$, check Fig. 2a. Mode 2 is when each of S6, D6 and S4 are ON where the output voltage is at level of $+2/3\ V_{dc}$. In this mode, both C2 and C3 are sharing their voltages to generate the voltage level of the output voltage, Fig. 2b. Mode 3 is when the output voltage at level of $+2/3\ V_{dc}$ as in Fig. 2c where each of the S8, D8 and S4 are on. In this mode, the voltage is fed from capacitor C3 only. The other mode is mode 4 where the output voltage is at level of 0 V when both switches S3 and S4 are on to form a short circuit path across the load. The following mode is mode 5. The second half cycle is established of the output voltage when each of S5, D5 and S2 are on to make the output voltage at level of $-1/3\ V_{dc}$. In this mode, the voltage is fed from capacitor C1 only. The other mode is mode 6 where the output voltage is at level of $-2/3\ V_{dc}$ when each of S7, D7 and S2 are on. In this mode, both C1 and C2 are sharing their voltages to generate the required voltage level of the output voltage as shown in Fig. 2f. Then mode 7 will come as shown in Fig. 2g when both switches S2 and S3 are on to make the output voltage at level of $-V_{dc}$. The last mode is mode 8 where the output voltage is at level of 0 V_{dc} again when both switches S2 and S1 are on as shown in Fig. 2h. Table 1 shows the switching scheme of the proposed inverter at different voltage levels.

Pulse width modulation of the proposed seven levels inverter: In this inverter an absolute sine wave at the fundamental frequency is generated by taking an absolute function to sine wave to make the Modulating Signal (MS). There are three carries are generated at higher frequencies than the fundamental frequency to make the required pulse width modulation for each switch. The first two carriers from above are shifted by Phase Opposition

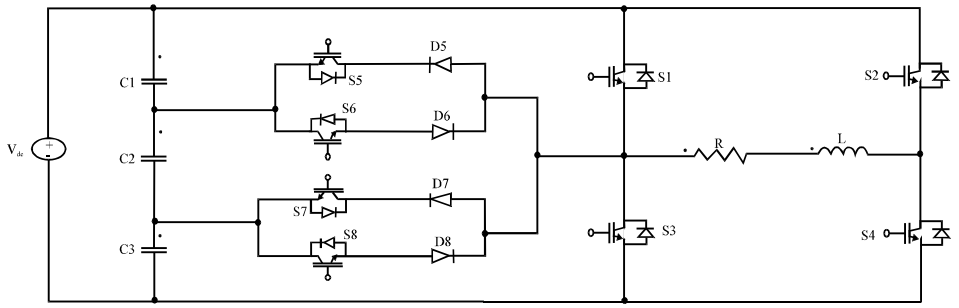

Fig. 1: The proposed seven levels inverter circuit

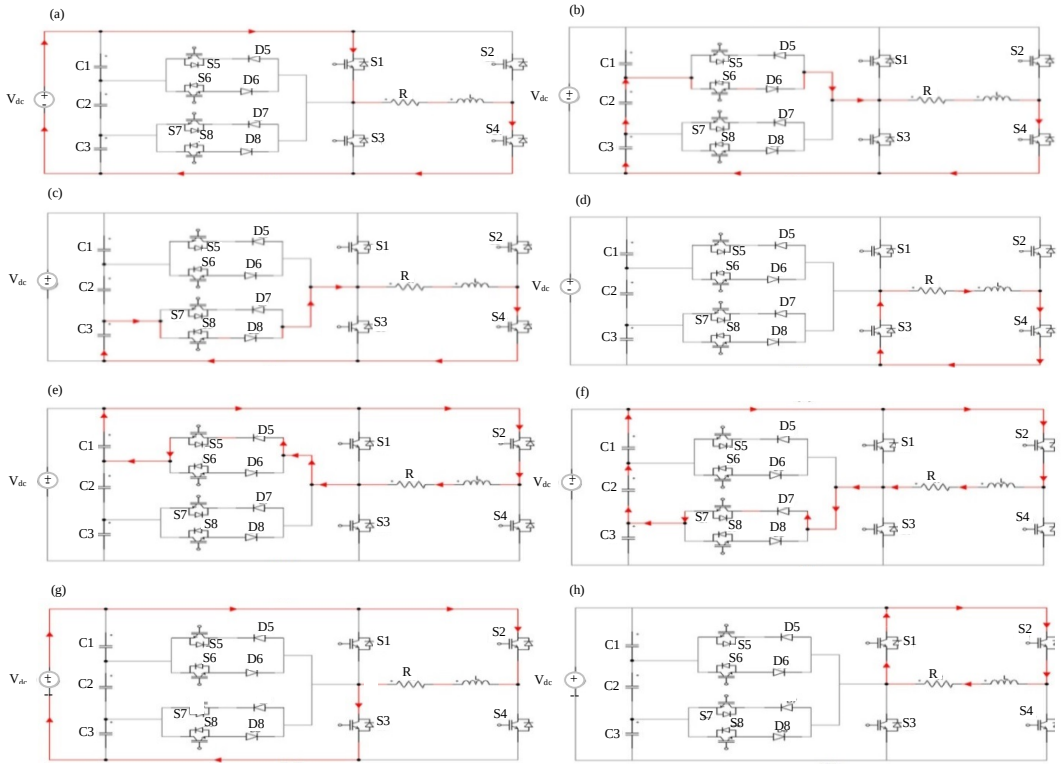

Fig. 2: Modes of operation of the proposed inverter

Table 1: The proposed inverter switching states at different voltage levels

SW.s/Vo (Levels)	$+V_{dc}$	+(2/3) V_{dc}	+(1/3) V_{dc}	0	0*	-(1/3) V_{DC}	-(2/3) V_{DC}	$-V_{DC}$
S8	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF
S7	OFF	OFF	OFF	OFF	OFF	OFF	ON	OFF
S6	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF
S5	OFF	OFF	OFF	OFF	OFF	OFF	ON	OFF
S1	ON	OFF	OFF	OFF	ON	OFF	OFF	OFF
S2	OFF	OFF	OFF	OFF	ON	ON	ON	ON
S3	OFF	OFF	OFF	ON	OFF	OFF	OFF	ON
S4	ON	ON	ON	ON	OFF	OFF	OFF	OFF

Disposition (POD) method. The last two carries from below are shifted by Alternative Phase Opposition Disposition (APOD) Method. Three comparisons can be made between each carrier with the modulating signal. In Fig. 3, there will be ten regions which are noted by angle where these angles are responsible about the changing among different voltage levels (Choi and Kang, 2015). The Modulation index (Ma) can be determined by the following Eq. 1:

$$Ma = \frac{Am}{Ac_1 + Ac_2 + Ac_3} \quad (1)$$

The instantaneous output voltage can be calculated by Choi and Kang (2015):

$$V_o = M_a \times V_{dc} \times \sin(\omega t) \quad (2)$$

where, Ac_1, Ac_2, Ac_3 and Am are the peak amplitude of carrier_1, 2, carrier_3 and the modulating signal respectively as shown in Fig. 3. When Ma is lower than or equal to Ac_2 a 5 levels inverter can be achieved from the proposed inverter and when Ma is lower than or equal to Ac_3 a three levels inverter can be gotten.

New method of making the logic expression to the switches of the proposed inverter: There are some ways to make the logic expressions of the switching signals for the multi-level inverter design. Some of the researches are making and with a Predetermined periods (Pn) and also with the switches signals S2 and S4 or with the signals that are generated by the comparisons among the carriers and the modulation signal. In this study, these periods are the angles which calculate the required regions among them. This method is simple but to make the required periods, the angles that make the change in between the levels of the output voltage should be known first. The new method is more efficient, since, it does not require a prior knowledge of these angles. This method is made by an assumption that the frequency of the carrier signals is same as the fundamental frequency as shown in Fig. 4.

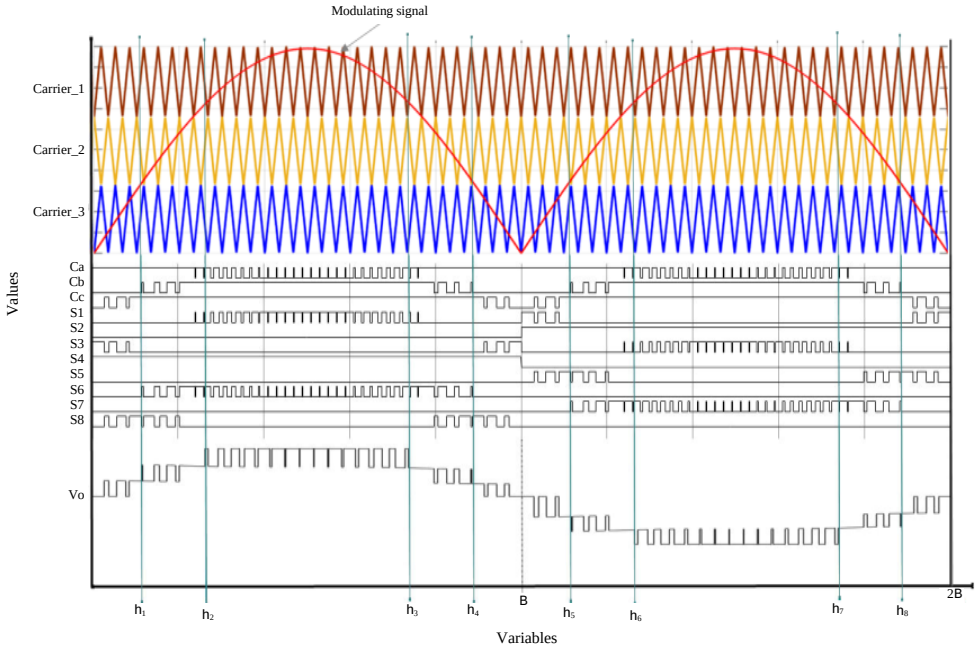

Fig. 3: Switching pattern of the proposed inverter

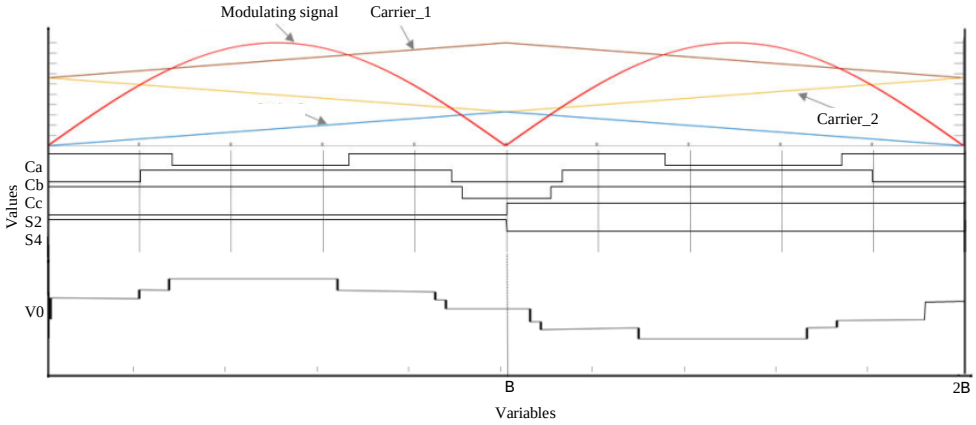

Fig. 4: The modulating and carriers signals at the fundamental frequency

In this new method, there are three comparisons are made among each carrier signal with the modulating signal as shown in the Fig. 4 where these comparisons are Ca, Cb and Cc and also, the switching signal of S2 and S4 switches are known, so, the logic expression of the proposed inverter can be as follows: MS = absolute (Sine function at fundamental frequency):

$$Ca = MS \leq carriar\_1$$
$$Cb = MS \leq carriar\_2$$
$$Cc = MS \leq carriar\_3$$

S4 = Square wave at fundamental frequency with 50% duty cycle:

$$S1 = (\overline{Ca} \cdot S4) + (\overline{Cc} \cdot S2)$$
$$S3 = (\overline{Ca} \cdot \overline{S2}) + (\overline{Cc} \cdot S4)$$
$$S8 = (Cc \oplus Cb).S4$$
$$S5 = (Cc \oplus Cb).S2$$
$$S6 = Ca.\ Cb.\ S4$$
$$S7 = Ca\ .Cb\ .\ S2$$

where the symbols $(\bar{s})(.), (+), (\bullet)$ represents NOT and OR and XOR logic expression, respectively. After making the

required logic expression, now it is possible to increase the frequency of the carriers in a manner that serves the inverter to be at high efficiency with low harmonic distortion. The signals of all switches from S1-S8 will be then as shown in Fig. 3.

SIMULATION RESULTS

The proposed seven levels inverter is simulated at various Am conditions. The output voltage waveform is as shown in Fig. 5 where the input voltage V_{dc} is 312 V. The fundamental frequency is selected to be 50 Hz and each carrier frequency is kept at 3000 Hz. The circuit is simulated by using MATLAB Simulink R2017a Version. The Total Harmonic Distortion (THD %) is determined for the proposed inverter.

The THD can be calculated up to the 40th harmonic as stated in (Anonymous, 1965). Figure 6, shows the THD of the proposed inverter's output voltage which is 4.4%.

The proposed circuit is tested at different load conditions and at different amplitude of the modulating signal (Am). When (Am) is less or equals to the amplitude of the carrier Ac_2, the output voltage of the inverter will be at five levels as shown in Fig. 7. When the Am is less or equals to the amplitude of the carrier, the output voltage of the inverter will be at 3 levels only as shown in Fig. 8.

The changing of Am values is a good way to control the inverter's output voltage value not only changing the voltage levels of it. By using a filter of LC circuit at the output side of the inverter, a good smoothing to the output voltage and current can be achieved where the inductor of the filter is 500 uH and the capacitor is 130 uF. Figure 9 shows the output voltage and current with using the LC filter where the RMS values of the output voltage and current are 222 V and 10.43 A respectively. Figure 10 shows the THD of the current after using of the filter.

Effect of over-modulation technique on total harmonic distortion and the RMS output voltage: As stated by Elserougi *et al*. (2013) and Rashid (2007) the over modulation technique can be used when it is desired to increase the RMS of the output voltage. Since, this type of inverter is designed to work with renewable energy sources. The over modulation means that the amplitude of the modulating signal is higher than the first or higher carrier amplitude value as in this inverter which Ac_1 is of carrier_1. The over modulation may make the peak of the output voltage at dc level for some period of time. This

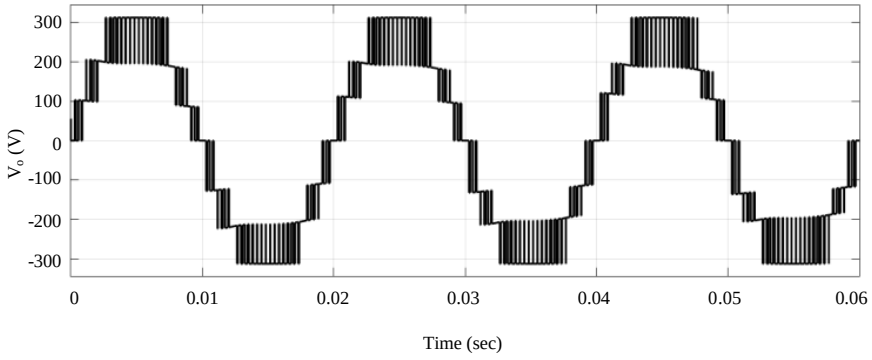

Fig. 5: The simulated output voltage of the proposed seven levels inverter

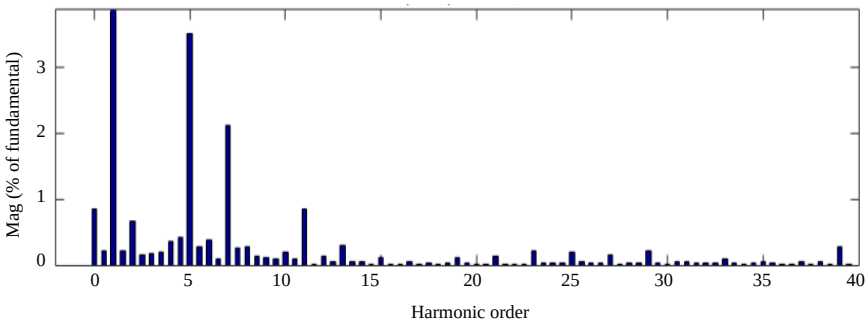

Fig. 6: THD of the proposed inverter's output voltage

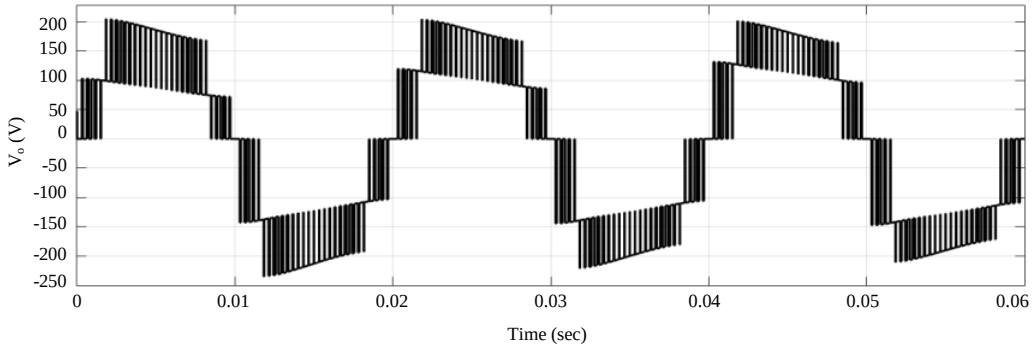

Fig. 7: The output voltage of the inverter

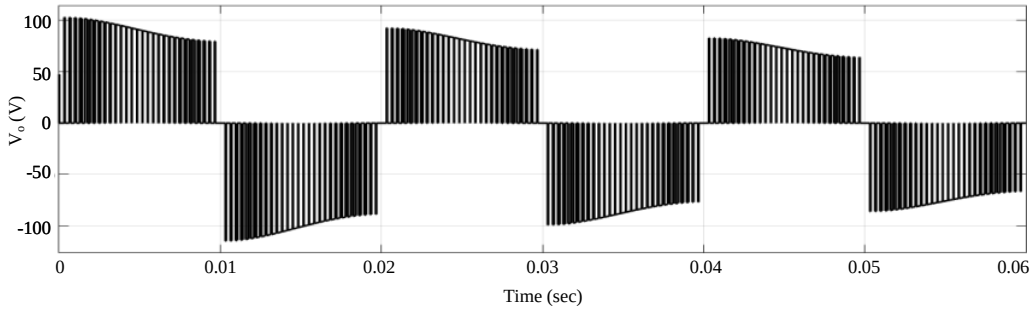

Fig. 8: The output voltage of the inverter

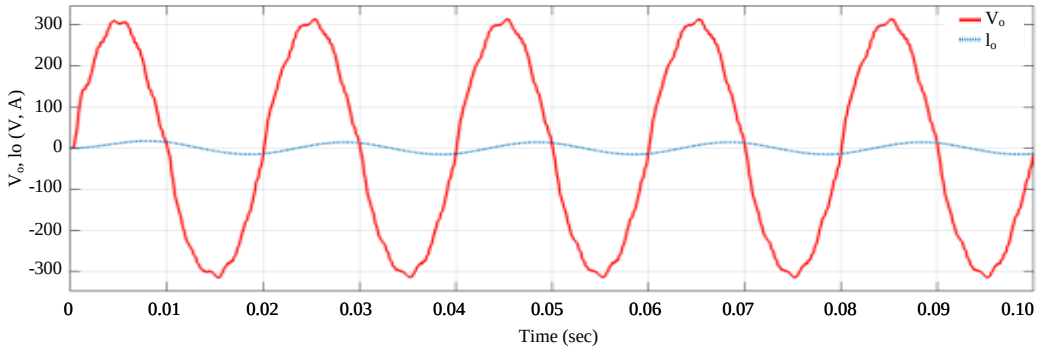

Fig. 9: Output voltage and current after using of the filer

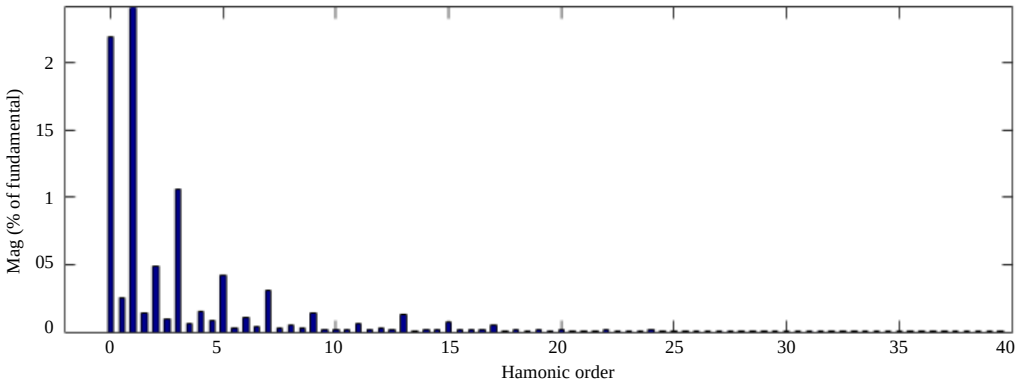

Fig. 10: THD of the output current after using of the filter

Table 2: Comparison of RMS and THD of the output voltage at different values of in case of over modulation

Amplitude of the modulating signal Am (PU)	Output voltage (RMS)	THD (%)
1.00	214.4	4.4
1.02	221.1	3.63
1.04	224.9	3.52
1.06	227.9	3.55
1.08	230.6	3.88
1.10	232.9	4.32

method has merits and demerits. The merits are when it increases the RMS value of the output voltage and decreasing the THD at some level. The demerit is when the Am is increased more, the THD may be increased with increasing of the first order harmonics. Table 2 shows a comparison of using the over modulation technique at different amplitudes of Am and THD values. The better result is when Am is at 1.05 PU where lower THD can be gotten which is 3.41%.

CONCLUSION

In this study, the proposed seven levels inverter is designed and simulated successfully. The new method of making the carries frequency is same as the fundamental frequency is good solution to get the logic expression of each switching device without depending on the predetermined periods then increasing the carrier frequency to get better performance of the inverter to get low THD. By decreasing the value of the amplitude of the modulating signal at some level less than or equal to amplitude of some carriers, a reduction in number of levels of the output voltage can be achieved. The over modulation technique can be used to relatively increase the RMS value of output voltage and decrease the THD. This inverter is recommended to be used at off grid applications with the renewable energy sources directly such as solar cells and/or with using of batteries or via. some of DC/DC step-up voltage converters circuits at the DC link side.

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