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A New Design of a Voltage Source MLI and Analysis of its Applicability for Medium Power Requirements

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Abstract: Multilevel inverters are being utilized widely and has generated immense interest in industry and research. While the conventional topologies have proved to be viable options for high power and medium voltage applications, a lot of research in this field is leading to continuous emergence of newer topologies aimed at reducing power losses while increasing the efficiency of the inverter. In this study, a distinct topology of MLI has been proposed that is recognizably different from the conventional topology. This new design uses fewer number of DC sources to generate maximum voltage levels, accordingly the count of power switches also lessens, leading to better spectrum and minimum distortion. Asymmetrical topology is used to generate 15 level stepped voltage output and addition of voltage Level Incremental Cell (LIC) in the same topology, further improves the voltage level up to 29 levels for single phase inverter resulting in lowering of Total Harmonic Distortion (THD). The capability of the experimental prototype for proposed MLI topology to produce intended voltage levels are further corroborated by the simulation results generated using MATLAB/Simulink.

Key words: Multi Level Inverter (MLI) asymmetrical topology, voltage Level Incremental Cell (LIC), Total Harmonic Distortion (THD), efficiency, experimental prototype, India

INTRODUCTION

Over the years, Multilevel inverters have attained wide acceptance in industrial applications, owing to numerous advantages such as reduced voltage stress on the power switches, low harmonic and EMI output, flexibility to operate on low as well as high switching frequencies and possibility of fault-tolerant operations (Malinowski *et al*., 2010). With the help of suitably connected power semiconductor switches, multiple input DC voltage sources and by controlled switching of power switches a multistep waveform with controllable amplitude, frequency and phase can be achieved. Among the available topologies CHB structure is capable of reaching medium output voltage levels using only standard low-voltage components (Corzine and Familiant, 2002; Rub *et al*., 2010). The grouping of MLI is usually done according to the values of the voltage sources used, the first group that uses voltage sources of equal values at all inputs it is termed as symmetric topology, however in usage the asymmetrical topology that makes use of values of DC sources in binary or trinary progression proves better in performance in terms of number of levels using the same number of switches (Astudillo *et al*., 2008; Alishah *et al*., 2014). Most of the current research activities of the researcher working on designing and testing of topologies for MLI are aimed at designing topologies that effectively reduce the number of components such as switches and DC sources leading to reduction in size and weight of the MLI while simultaneously aiming to achieve, increased power density, simplify gate drive and control and low power consumption by the switches, resulting in increase in the total reliability of the inverter (Gupta and Jain, 2013; Ajami *et al*., 2013; Mokhberdoran and Ajami *et al*., 2014; Babaei *et al*., 2015; Sappati *et al*., 2014). This study focuses on the design aspects of multi level inverter using SPWM modulation technique in which the numbers of switches as compare to the conventional MLI design are reduced by a considerable number, resulting in lessening of switching losses, cost saving and improved efficiency. Modulation techniques are used to control the power switches. The choice of modulation methods depends upon the applications where the inverters are used. Among frequently used modulation techniques SPWM, SHE and Space Vector Modulation (SVM) the study opts to use SPWM in the design of proposed MLI as this technique applies simple control strategy by comparing the modulated signal with triangular carrier signals. The research in this study makes use of asymmetrical

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topology by using with SPWM modulation to design a 15 level inverter and by adding an extended cell (LIC) the same topology resulted in nearly double number of stepped output voltage at 29 levels. In this study, the aim is to use fewer number of power switches and yet increase the number of generated output levels. This is achieved by using a basic cell unit consisting of unidirectional switches (one IGBT with anti parallel diode) and power diodes. As the basic unit generates only positive levels hence adding an H bridge to this inverter will generate all positive and negative level at the output. Three different algorithms are proposed for generating the voltage levels at the output and comparative study has been done to evaluate the performance of the proposed topology with the conventional topologies. Based on the comparison it can be seen that the developed MLI uses lesser number of switches for better performance. A laboratory prototype is also design to check the performance of the inverter.

MATERIALS AND METHODS

Proposed topology:

Asymmetrical 15 Level Inverter Configuration with level incremental (LIC): In the proposed topology the arrangement of switches vary from the conventional arrangement for both topologies, symmetrical and asymmetrical. Topologies can be classified or differentiated as symmetrical or asymmetrical based on the values of DC voltage sources. The asymmetrical topology is preferred over symmetrical one as it gives higher number of levels of output waveform with same number of switches as stated earlier also.

The use of asymmetrical topology is necessary as it decreases the number of switch count and number of DC sources while it improves the stepped output voltage waveform leading to an improvement in the efficiency of inverter. At this stage a new topology called sub multilevel converter is introduced. A sub multilevel inverter is basically a hybrid multilevel inverter which is the combination of basic H and minor variation in the arrangement of switches and DC sources in H-bridge.

Basic proposed topology: The basic proposed topology is shown below in Fig. 1a, b is to enumerate types of switches. It consists of 5 unidirectional switches and 3 diodes. Here, 3 positive levels can produce from this cell.

To produce bidirectional waveform an H bridge is needed. In symmetrical topology, basic cell uses only 5 switches with equal values of dc sources to achieve 7 levels at the output of inverter. To increase the number of levels using the same number of switches, asymmetrical

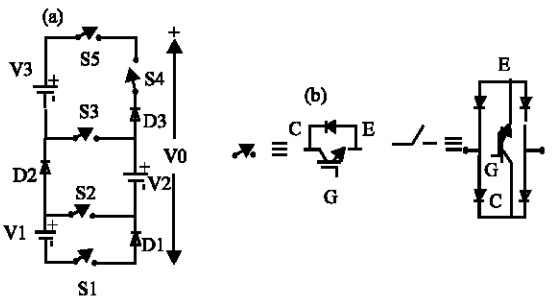


Fig. 1: a) Basic proposed topology and b) Unidirectional and bidirectional switch

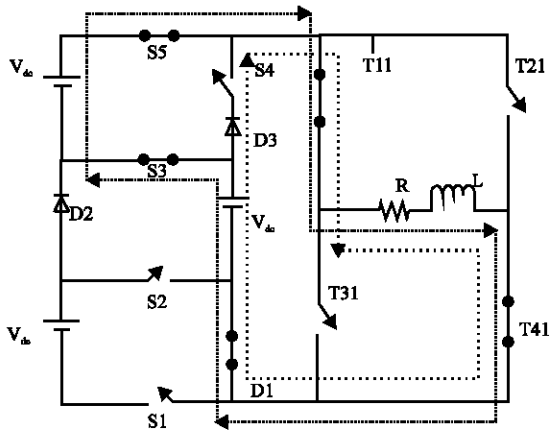


Fig. 2: Asymmetrical topology for 15 level to obtain step 1: $+V_{dc}$ step 2: for $+2\ V_{dc}$

topology is used with the same configuration and varying values of DC source in terms of even multiples. For proposed topology two extensions are possible cascading connection of proposed cell connections configuration cascading of each proposed cell with H-bridge configuration.

Here, idea is adopted for analysis as requirement of switches are less as compare to former one. Figure 2 a, b is the circuit diagram to attain 15 levels with the direction of current for achieving different steps of at the output of inverter. Table 1 will illustrate to achieve 15 levels and the value of DC input is 10 V = 1 p.u. is assume.

Asymmetrical inverter configuration with Level Incremental (LIC): Voltage Level Incremental Cell (LIC) is incorporated to increase the levels of multilevel inverter at the output as proposed in (Sappati *et al*., 2014). Figure 3 shows the operation of LIC as: with ON state of the switch current flows through the switch from point A-B whereas in the OFF state of the switch the current will flow through the diode from point A-B.

Table 1: Switching sequence for 15 level inverter (1 pu = 10 V)

V_{pu}	S1	S2	S3	S4	S5	D1	D2	T11	T21	T31	T41
7	1	1	1	0	1	0	0				
6	1	1	0	1	0	0	0				
.	.	.	.	.	.	.	.				
.	.	.	.	.	.	.	.	1	0	0	1
.	.	.	.	.	.	.	.				
2	0	0	0	1	0	1	0				
1	0	1	0	0	1	1	1				
0	0	0	0	0	0	0	0	1	1	0	0
-1	0	1	0	0	1	1	1	0	1	1	0

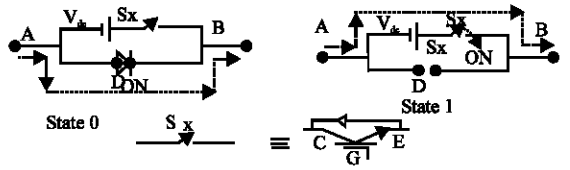


Fig. 3: Level Incremental Cell (LIC)

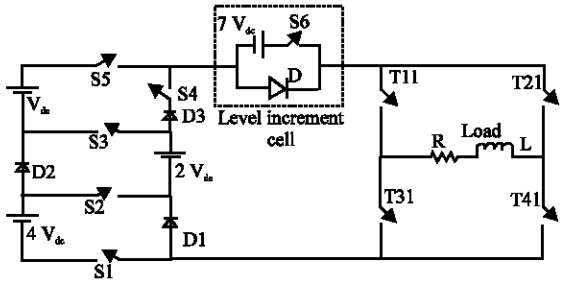


Fig. 4: The 15 levels+cell topology

Normally two rules are needed to select the proper value of LIC in symmetrical and asymmetrical topologies. For some topologies the cell value is equal to sum of voltage source values in the existing topology with H-bridge:

$$V_{ex} = [V1+V2+V3+, \ldots, Vn] \quad (1)$$

Using this concept number of levels increases up to doubling of the levels of inverter but not double. For some topologies the cell value is as follows:

$$V_{ex} = [V1+V2+V3+, \ldots, Vn]+1 \quad (2)$$

Using this concept number of levels of inverter will reach to double of the existing inverter levels. Here, in the proposed topology former concept has been used.

Figure 4 represents the diagram of addition of Level Increment block (LIC) in 15 levels asymmetrical cell. Using this concept the number of levels of inverter reaches up to 29 level. The proposed topology by using 5 switches and 3 power diodes in unit cell and 3 dc sources gives 15 levels and for achieving 29 levels (the 15 level+cell) it uses only 6 switch 4 power diodes and 4 dc source. Whereas for achieving 15 levels by Babaei *et al.* (2015), 2 cells are needed with developed cell in which the number of switches are 12 with 7 dc sources and its limitation is that it is used only for symmetrical topology. However, the proposed topology in symmetrical configuration can produce 9 and 13 level using LIC with voltage values V_{dc} and 3 V_{dc}, respectively.

Generalization of proposed topology: The proposed topology can be extended to "n" numbers of cells which are connected in cascade. If "n" is number of cells are connected in cascade and each cell consists of three numbers of sources namely 1-V3n. The three algorithms are used to determine the voltage values for production of voltage levels in MLI for asymmetrical configuration.

Proposed algorithm

First algorithm (M1): The proposed algorithms increases the steps in the output voltage. Here, a cell with variety of "three" different voltage sources such as V_{dc}, 2 V_{dc}, 4 V_{dc} are used known as binary progression. The expression for the number of dc voltage sources, max voltage in the output voltage waveform, used in algorithm is depicted in Table 2.

Second algorithm (M2): Here, the voltage source values are based on binary value progression of each cell. General expression for Eq. 3 and 4 as follows:

$$\text{1st cell voltages} \quad V11 = 4V_{dc};\ V21 = 2V_{dc};\ V31 = V_{dc} \quad (3)$$

2nd cell onwards voltage values:

$$V1n = 28\times8^{n-2};\ V2n = 14\times8^{n-2};\ V3n = 7\times8^{n-2} \quad (4)$$

where, n = 2, 3, 4, ..., n cells

Third algorithm (M3): In the third algorithm Level Increment Block (LIC) is connected to asymmetrical topology so that output voltage levels can be increased. Here, the block voltage source value for every cell addition is changing according to level increment. The general expression for the algorithm are given in Table 3 and expression for block voltage is given in Eq. 5:

$$V_{ex} = 7\times8^{k-2} \quad (5)$$

Block voltage source value: The proposed topology uses unidirectional switches in thecircuit; these unidirectional switches are made by a combination of IGBT with

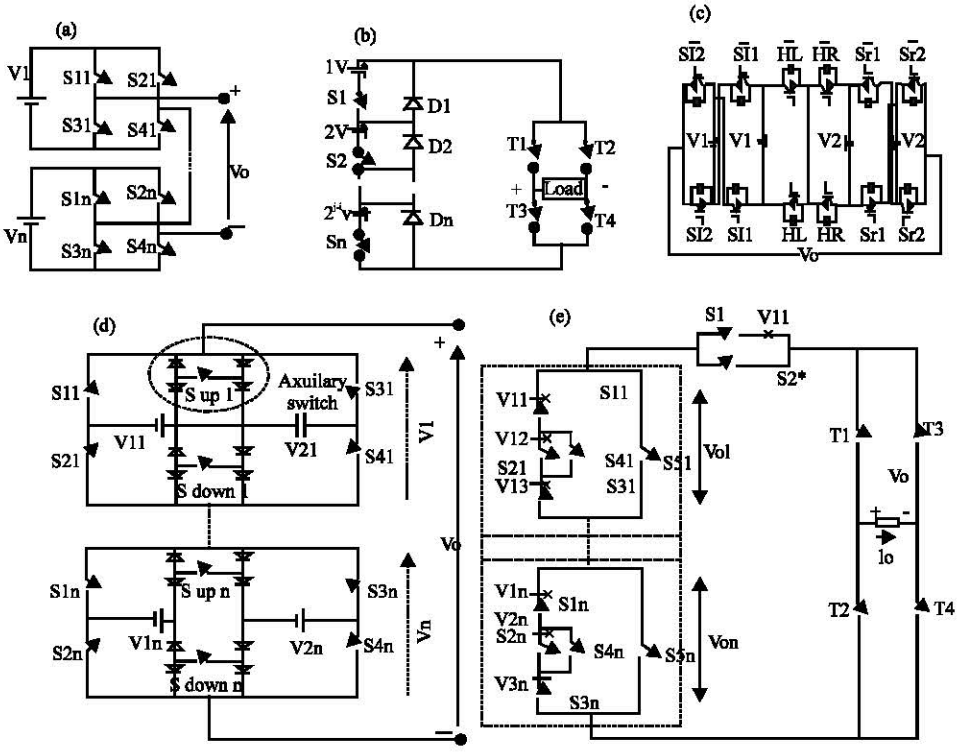


Fig. 5: a) T1 Cascaded H-bridge topology (Corzine and Familiant, 2002); b) T2 (Alishah *et al*., 2014); c) T3 (Ajami *et al*., 2013); d) T4 (Mokhberdoran and Ajami, 2014) and e) T5 (Babaei *et al*., 2015)

Table 2: General equation for the parameters used in proposed 3 algorithms

Proposed algorithms	Voltage source amplitude	N_{level}	V_{max}	$N_{variety}$	N_{diode}	N_{IGBT}
First algorithm (M1)	V11 = V12 = V13 =, ..., = V1k = 4 V_{dc} V21 = V22 = V23 = , ..., =V2k = 2 V_{dc} V31 = V32 = V33 = , ..., = V3k = V_{dc} for K = 1, 2, 3 ,..., n	14N+1	7n*Vdc	3	3n	5n+4
Second algorithm (M2)	V11 = 4 V_{dc}; V21 = 2 V_{dc} V31 = V_{dc}, V1k = 28×8^{k-2}, V2k = 14×8 k-2, V3k = 7×8^{k-2} For k = 2,3, ..., n	243+42×(20^{n-1})/19	(7×8^{n-1}) V_{dc}	3n	3n	5n+4
Third algorithm (M3)	V11 = 4 V_{dc}; V21 = 2 V_{dc} V31= V_{dc}; V1k = 28×8^{K-2}, V2k = 14×8^{K-2}, V3k = 7×8 K^{-2}; Vex = 7×8^{k-1} for K = 1, 2, 3, ..., n	1+7×4 n	(7×4^{n}) V_{dc}	3n+1	3n+1	5n+5

anti-parallel diode. Here, the driver circuit needed for firing the switches will be same as no. of switches or IGBTs and no driver circuit is required for power diodes. Table 2 show the general equation used in the proposed algorithm.

Comparison of proposed algorithms with existing topologies: From Table 2, it is found that topology M3 gives more number of levels for same number of switches and DC sources used in M1 and M2 topologies. Again variety of dc sources are more in M3 but it also gives more number of levels as contrast to other algorithms.

Proposed topologies M1 and M3 are compared with recently published existing topologies for different parameters viz. number of levels, number of switches and number of dc sources used among proposed algorithms are given in Table 3 and shown in Fig. 5.

From Table 3, comparison graphs are plotted to show the variation of no of dc sources, no of diodes and no of switches w.r.t. no of levels achieved by different existing topologies and proposed one. From a comparison of the graphs in Fig. 6a-c it can be observed that the source requirement in proposed topology (M3) equals to that in the topology T5 but when the comparison is done with respect to number of steps produced (M3) produces 29 levels using one cell whereas topology T5 produces 9 levels using one cell. Similarly when comparison is done for number of sources used to produce no of levels, the proposed topology (M1) outputs 15 levels by using one

Table 3: Comparison between topologies

Topology	Levels	Switches	dC sources	Diodes
Proposed M1	14n+1	5n+4	3n	3n
Proposed M	1+7×4^n	5n+5	3n+1	3n+1
Topology-T1 (Astudillo *et al*., 2008)	2n+1	4n	n	--
Topology-T2 (Ajami *et al*., 2013)	2^(n+1)-1	n+4	n	n
Topology-T3 (Babaei *et al*., 2015)	n×(p+1)+1 (here, p = 2)	2n+4	n(>4, even)	--
Topology-T4 (Sappati *et al*., 2014)	2^(2n+1)-1	6n	2n	8n
Topology- T5 (Kangarlu and Babaei, 2013)	12n-3	5n+6	3n+1	--

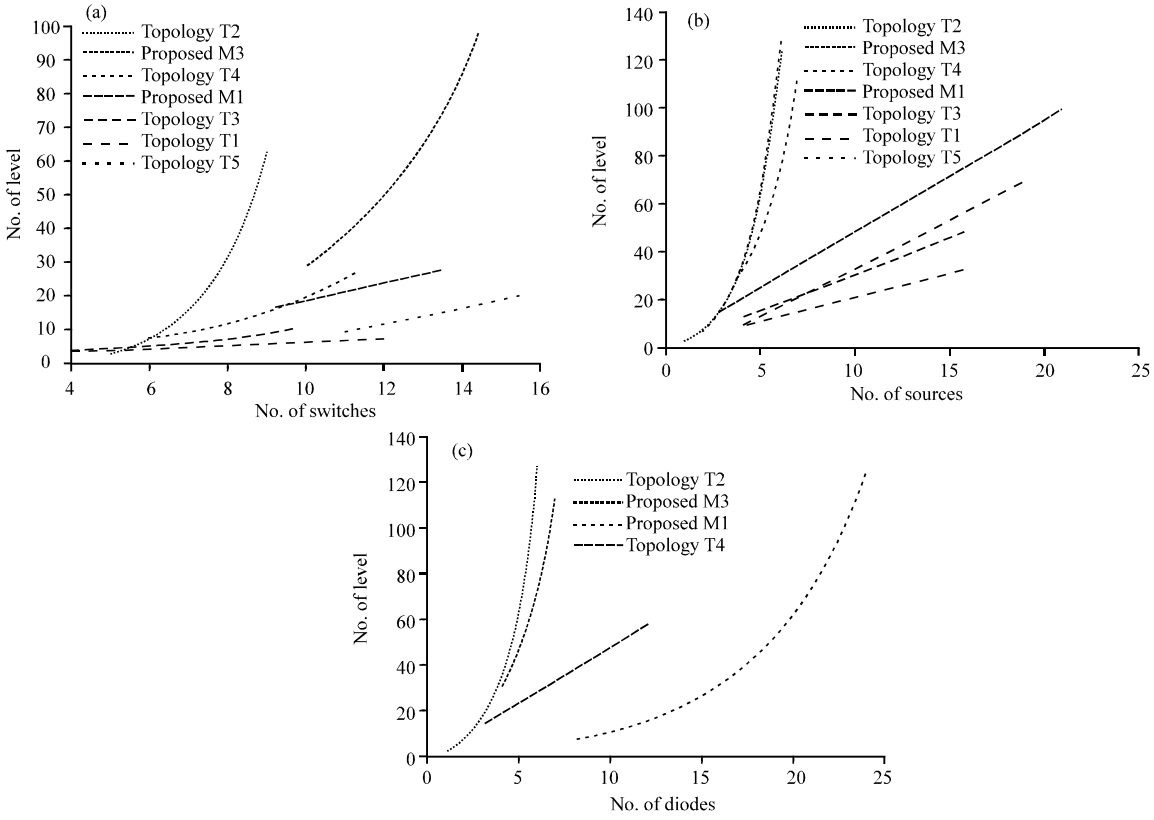


Fig. 6: a) Variation of nlevel with nswitch; b) Variation of nlevel with N sources and c) Variation of N level with diodes

cell with one less source where as topology T5 produces 15 levels using two cells in cascade. When the proposed topologies (M1) and (M3) are compared with topology T4 (Fig. 6c) for number of diodes, topology (M1) uses only 3 power diodes in one cell to produce 15 levels and topology (M3) uses only 4 power diodes to produce 29 levels, topology T4 uses 8 power diodes to produced 7 level in unit cell and topology T2 uses 3 diodes to produce 15 level, however, topology T5 does not need any diodes. In terms of utilization of switches topology (M1) and (M3) uses 9 and 10 number of switches, respectively where as topology T5 uses 11 No. of switches and topologies T3 and T4 uses 6 switches in one cell. Thus, from the comparative study of the two proposed topologies with the existing topologies it can be concluded that the utilization of switches and sources are more economical in the proposed topologies.

RESULTS AND DISCUSSION

This study deals with the performance of the proposed inverter in terms of Total Harmonic Distortion (%THD) and efficiency at different load conditions (R and RL loads). The proposed inverter configurations are verified by MATLAB/Simulink Software to investigate voltage across the loads. The simulation results are for 15 levels (using M1) and for 29 level (using M3) using APOD modulation method which is one of the popular carrier based modulation (SVPWM) method. The values taken

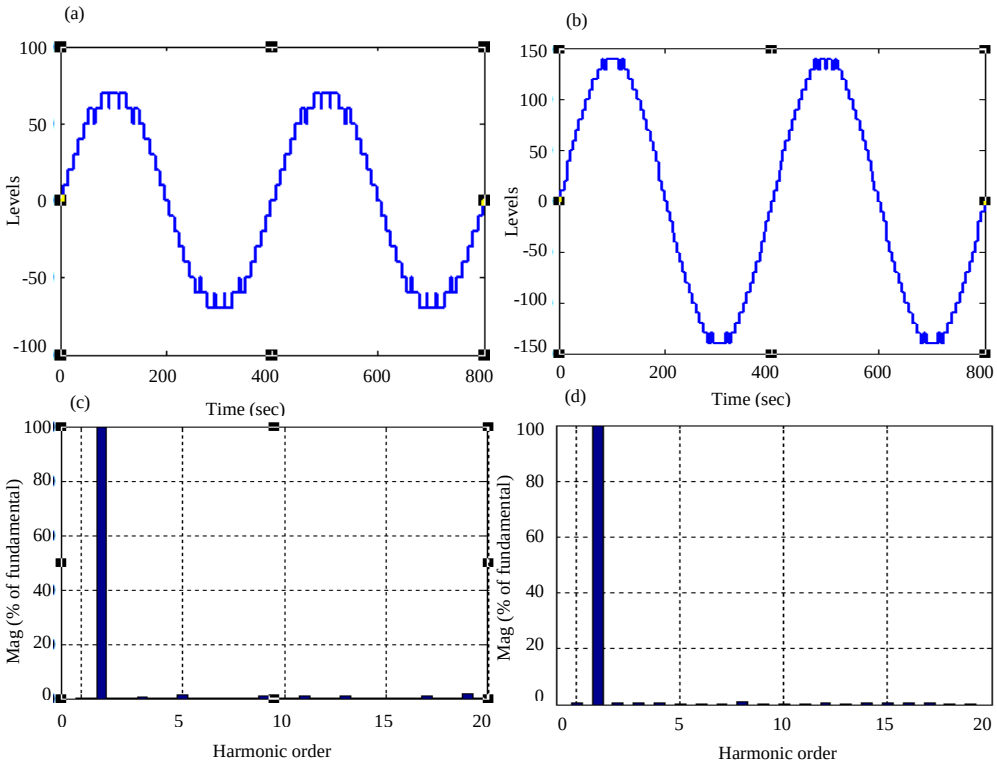


Fig. 7: Output voltage waveform and FFT spectrum for R-L load: a) 15 level inverter; b) 29 level inverter; c) Fundamental (50 Hz) = 1.169, THD = 6.97% and d) Fundamental (50 Hz) = 140.1, THD = 3.92%

Table 4: Topology Comparison with optimal frequency and corresponding THD value

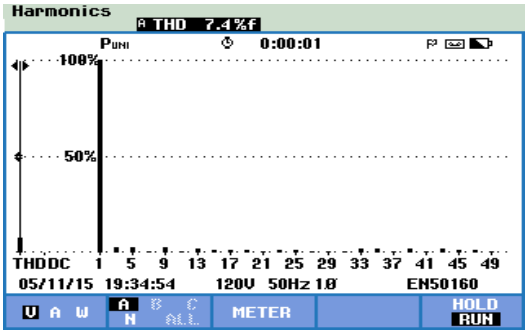
	R-load (90 Ω)			
No. of levels	Simulation/Frequency (Hz)	Hardware/THD (%)		WTHD
15	1.1 K	7.04	7.5	0.2861
	1.2 K	7.49		0.6590
29	1 k	4.67		0.4143
	1.6 K	4.16	4.4	0.2569
RL-Load(90+j4.39mH)				
	1.1 K	6.97	7.2	0.2861
	1.2 K	7.54		0.6590
	1 K	4.2		0.3697
	1.6	3.92	4.0	0.2547

for 15 level are V 11 = 4 V_{dc}, V 21 = 2 V_{dc}, V 31 = V_{dc} at frequency 1.1 and 1.2 kHz, since, THD obtained is minimum at these values. Similarly for 29 level V 11 = 4 V_{dc}, V 21 = 2 V_{dc}, V 31 = V_{dc} and V_{ex} = 7 V_{dc} at frequency 1 and 1.6 kHz, respectively. The THD and efficiency of the proposed inverter at different load conditions are evaluated. Performance of any inverter can be checked with R-L load. Figure 7a, b show the output voltage waveforms and respective %THDvalues for R-L load of 15 and 29 levels inverters. Table 4 gives the comparison of values of THD at different frequencies for 15 and 29 levels inverter at diverse load conditions. The THD is the measure of quality of output waveform of MLI and calculated with the help of the following Eq. 6:

$$THD\% = \sqrt{\frac{V_{rms}^2 - V_1^2}{V_1^2}} \times 100 \quad (6)$$

Figure 7a, b depicts the output waveform and corresponding harmonic spectrum for 15 and 29 levels inverters, respectively for R-L (90+j4.39 mH) load and minimum value of %THD is obtained for 15 and 29 levels are 6.97% at 1.1 kHz and 3.92% at 1.6 kHz frequency, respectively which is within accepted limit.

(a)



(b)

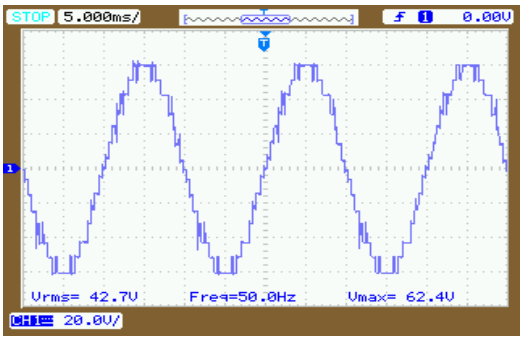
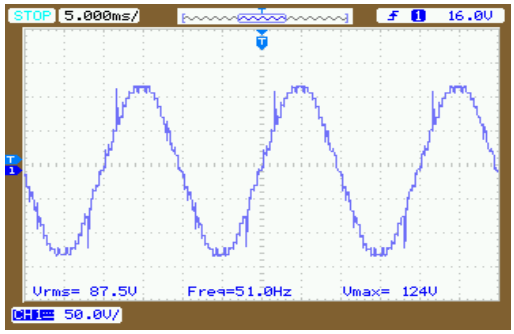


Fig. 8: a)and b) Output voltage and corresponding THD% values for 15 level inverter with R-L load

Hardware setup and results: To justify the results obtained from simulation is further tested in laboratory. The hardware used are digital controller d space-1104 and Power Inverter Module (MECHA MECHATRONIX/2014 R01) consisting of 8 IGBTs per module. To calculate the harmonic distortion power quality analyzer (Fluke Model 434-II) has been used.

The output waveform and harmonic spectrum for 15 level inverter are shown in Fig. 8a, b and 9a, b show the output waveform and harmonic spectrum for 29 levels inverters for R-L load. It can be from Fig. 9b that the value for the THD % for 29 level inverter is 4.0% at 1 kHz. This result is within the scope of IEEE standard. The results obtained by proposed topologies illustrate that the quality of output waveform reduces the size of filter considerably resulting in lowering of the overall cost of the inverter. The output voltage waveform across switch T11 and S2, respectively for 15 level inverter can be in Fig. 10a, b, respectively. To verify the circuit of proposed topology it is necessary to check the efficiency (Kangarlu and Babaei, 2013). The efficiency of the proposed MLI has been calculated by using expression given in Eq. 7:

(a)



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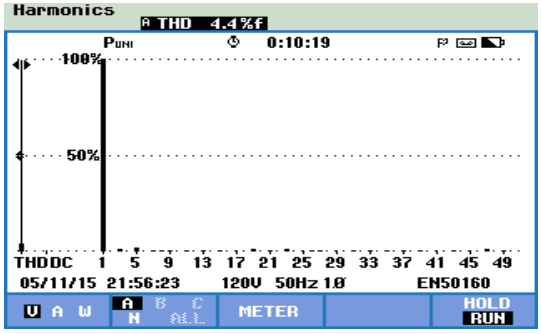
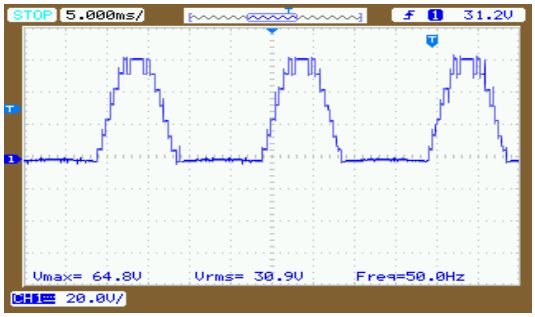


Fig. 9: a) and (b) output voltage and corresponding THD % values for 29 level inverter with R-L load

(a)



(b)

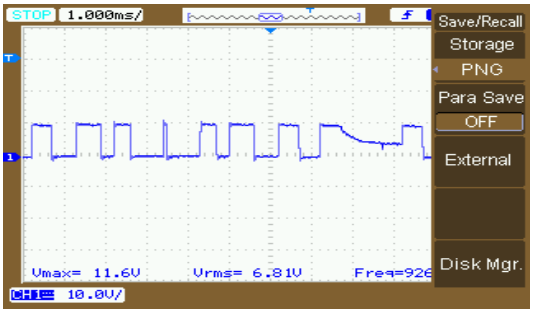


Fig. 10: a) and b) output voltage wave from across switches T11 and S2

Table 5: Efficiency calculation at R and RL load

	Source 1		Source 2		Source 3		Outputvoltage	
Load	Voltage (V)	Current (mA)	Voltage	Current (mA)	Voltage	Current (mA)	Voltage	Efficiency (%)
R = 90	10	364	20	444	40	580	46.6	94.845
RL = 90+j4.39 mH	10	391	20	411	40	614	45.0	95.135

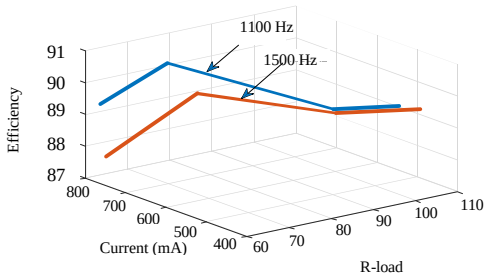


Fig. 11: Efficiency graph for 15 level at different loads

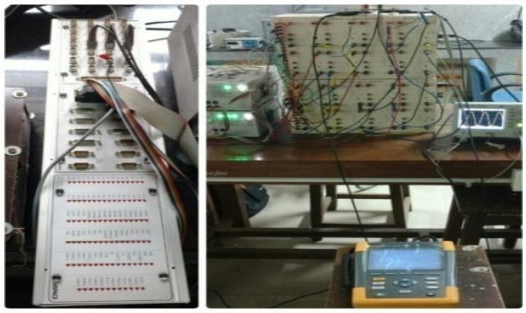


Fig. 12: Test rig

Calculation of efficiency:

$$\text{Efficiency}\% = \left[\frac{P_{out}}{P_{IN}}\right]\times 100 \qquad (7)$$

where, P_{OUT} denotes output power of inverter. Table 5 shows the hardware results of input and output voltages and currents of 15 level inverter at different loads. A graph has been plotted for efficiency of 15 level inverter at different values of R-L loads at 1.1 and 1.5 kHz frequencies as shown in Fig. 11 and the maximum efficiency of 95.135% is obtained at R-L load at 1.1 kHz (Fig. 12).

CONCLUSION

In the present study, the main object was to design MLI with reduced amount of switches to reduced switching losses of inverter and compared with recently proposed topologies and it is found that the proposed topology give better performance as compare to the topologies taken into consideration in point of view that IGBT switches, driver circuits and losses required for a particular number of levels even though same number of voltage sources are used. The THD obtained for 29 level inverter is 4.0% which is within IEEE standard. According to the obtained results of efficiency for 15 level inverter, the proposed topology can be used for controlling single phase or three phase AC drives.

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