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Novel Eleven-Transistor (11T) SRAM for Low Power Consumption

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Abstract: Low power SRAM array is fundamental to organize substantial reliability and prolonged battery life for portable application. Since, charging/discharging enormous bit lines capacitance consume large portion of power, new SRAM design is proposed to lessen the power consumption and access delay for read/write operation. The proposed 11T cell contains two transistors in the feedback path of the respective inverter to minimize the write power consumption. Cell is simulated in terms of speed, power and stability. The simulated results show that the read and write power of the 11T SRAM cell is reduced up to 49 and 80% at 0.7 V, respectively and cell achieves 2.5× higher Static Noise Margin (SNM) compared to the conventional 6T SRAM cell. The designed cell can be utilized in mobile appliances even in worse temperature state with lower power consumption.

Key words: SRAM, power consumption, access time, read/write, SNM, worse

INTRODUCTION

In every aspect of our daily lifestyle the portable gadgets such as personal digital assistants and mobile appliances are obtaining more popularity while making improvements day by day (Liu *et al*., 2007). Greater request in fixed memory access in video or image employment influences its power utilization, making the endurance of the battery reach its maximum capacity. Power dissipation has become a vital consideration due to the rapid development of battery operated tools and appliances (Gopal *et al*., 2013). Current leakage is expanding with the decline of the gadget sizing. Therefore, low power SRAM cell design is crucial in order to accomplish battery operated device functions (Seevinck *et al*., 1987, Alioto, 2012). Approximately 90% of VLSI circuits make up SRAMs. Important factors of SRAMs which are the speed, stability and power consumption have led to various designs with the objective of reducing the power utilization to the minimum level during read/write operations (Grossar *et al*., 2006). The fundamental aspect in SRAM cell architecture is stability. It determines the cell's capacity to work the resilience and processing constrictions. In the existence of noisy signals, appropriate operations have to be uninterrupted. Hence, different considerations and experimentation have been done with a specific end goal to limit the power utilization of SRAM modules. A standout amongst the most practical steps to meet this objective is to construct extraordinary low power SRAM architecture. Latest research works have proved that access disturbance at low-power mode in Conventional 6T SRAM caused it to suffers extreme stability degradation (Aly and Bayoumi, 2007; Prabhu and Singh, 2009). The aim of this study is to design an improved Novel 11T SRAM cell in 65 nm CMOS technology which can perform the read/write operation in low power state by improving the static noise margin. The suggested SRAM design functions by disengaging the feedback path of the inverter with the goal that the coveted writing state can be accomplished. The write operation is accomplished easily by passing the information from the bit-line to storage node and this will cause decrease in power utilization and access time. This study assesses the following highlights for SRAM cell utilizing the recommended Novel 11T SRAM configuration architecture: power utilization, access time of write/read, stability and static noise margin. The outcomes, simulations and outputs are contrasted with conventional 6T and 7T SRAM cell to differentiate the performance of the proposed cell.

MATERIALS AND METHODS

Proposed circuit description: The schematic design architecture of the proposed 11T SRAM cell is depicted in Fig. 1. The cell consists of 11 transistors which includes two bridging transistors which is transistor NMOS N5 and PMOS P3 which are associated at the feedback path of the inverter and a read access transistor, NMOS N8 which will only be initiated during read operation. The write execution of the novel 11T cell contrasts from 6T SRAM by removing the feedback path of the two inverters.

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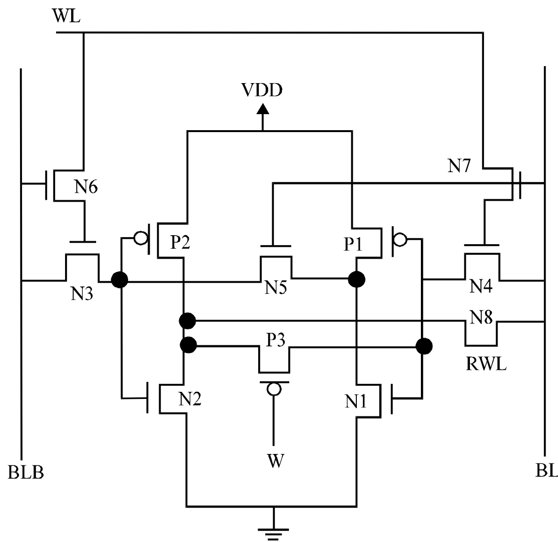

Fig. 1: Proposed SRAM cell

Therefore, the transistor's working burden is wiped out by lessening its power consumption and access delay. Other than that, the two bridging transistors are handled by one of the Bit-Line (BL) to additionally diminish the power consumption of the cell. In this way, the access time is reducing, since, the switching operation at the feedback path way is executed at the same time when N5 is turned ON while P3 is turned OFF and the other way around. These bridging transistors functions as feedback path transistor to execute quick state change (0->1 or 1->0) at storage node Q and nQ without totally discharging. Word Line signal (WL) dominates the write access transistor to permit write "0" or write "1" operation. For read operation, a read access transistor, N8 is activated by read word line which shortens the read path. The write operation is executed by moving the information from Bit-Lines (BL and nBL) to storage nodes (Q and nQ). The path of the cross-coupled inverter is disconnected by the bridging transistor before accomplishing any write operation. Both the bit-lines are set to the desired logic before starting the write operation by activating the access transistors. The complement of the input data of BL is supported by nBL with the goal that when BL is equivalent to 1 then nBL is equivalent to 0 and vice versa. Amid every operation the bridging transistor will alternatively turn ON/OFF by the input from BLB and W. The transistors that are activated during both write operation is depicted in Fig. 2a, b.

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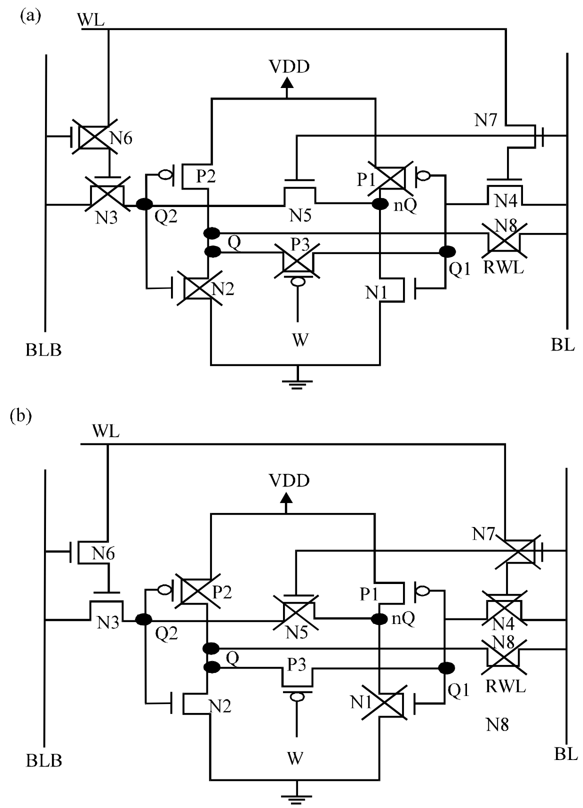

Fig. 2: a) Write "1" mode and b) Write "0" mode

accomplishing any write operation. Both the bit-lines are set to the desired logic before starting the write operation by activating the access transistors. The complement of the input data of BL is supported by nBL with the goal that when BL is equivalent to 1 then nBL is equivalent to 0 and vice versa. Amid every operation the bridging transistor will alternatively turn ON/OFF by the input from BLB and W. The transistors that are activated during both write operation is depicted in Fig. 2a, b.

Concerning the write "1" operation at storage node Q, Bit-Line BL must be set to high state (BL = 1). The complement of the input data is conveyed by nBL (nBL = 0). By setting BL = 1, transistors N7 and N4 are now kept in ON state and when transistor N4 is turned ON, the information from BL is transferred to storage node Q through inverter 1 (P1 and N1) to change nQ which is equivalent to Q2 transistor N5 will be kept ON through transistor N7 and transistor P3 will be initially kept OFF, since, W is set to 1. By setting WL to "0", the transistor N3 is turned OFF which detaches nBL from node q2 (P2 and N2) Q2. Concerning the write "0" operation at the storage node Q, bit-line nBL must be set at high state, (nBL = 1). The complement of the input data is conveyed by BL (BL = 0). By setting BL = 0, transistors N7 and N4

are kept in OFF state and transistor N4 detaches BL from inverter 1 (P1 and N1). Transistor N5 will be kept OFF through transistor N7 and transistor P3 will be initially kept ON by setting W to "0". By setting WL to "1", the transistor N3 is turned ON. When N3 is ON, the data that is contained in nBL is shifted to storage node Q2 through inverter 2 (P2 and N2) to change Q which is equal to Q1. To perform read operation, set RWL = high, WL = 0. Transistors N7 is utilized to carry out the read operation.

RESULTS AND DISCUSSION

The Novel 11T cell design is actualized and simulated utilizing 65 nm CMOS innovation utilizing BSIM4 Model parameter. The supply voltage, VDD is 0.7 V. Two separate circuit makes up the proposed cell which is the read operation circuit and write operation circuit with a specific end goal to enhance the speed, power utilization, stability and access time. Other than that, the write circuit comprises of two extra transistors which is in charge of cutting off the feedback path of the inverters. Consequently, without having to discharge the bit-line completely, the storage nodes states can be flipped amid the write operation.

Table 1 demonstrates the results that have been simulated for various inputs. From the yield, we can state that the general power consumption of the designed 11T SRAM is much lower compared in relation to customary 6T and 7T SRAM cell. By cutting off the feedback loop during the write '1' and write '0' operation brings about decrease in power consumption. During the transition 0->1, the power consumption is reduced up to 81.79% and during transition 1->0 is 81.73% as compared with 6T SRAM. During the transition 1->1 and 0->0, the power utilization is practically to 76%. The write access time or commonly known as write delay which is characterized as the time between the activation 50% of WL to Q bar is 90% of its swing. It can be noticed that the access time of the proposed 11T cell is decreased half compared to 6T SRAM cell where the percentage for change 0->1 and 1->0 are 53.13 and 51.56%, individually. The results that have been simulated are delineated in Fig. 3 where the yield value for both the transitions is decreased to half as compared to 6T SRAM.

Simulation at various temperatures was performed on the proposed 11T ranging from 27-140°C to watch its standby power. The sub-threshold current is dominated by carrier diffusion, consequently the leakage current increments exponentially with temperature. Contrasted with 6T SRAM, the standby power at every temperature of the 11T cell architecture is less than half as represented in the graph. Not at all like in 6T cell, the standby power of the 11T cell is much lower which empowers the cell to be worked under harsh condition with low power consumption which is demonstrated from the simulation result in Fig. 4. Presenting a separate transistor (N7) at BL and a signal RWL empower the proposed circuit to execute read operation in a different way as compared to the write operation. During read '0' operation at node Q, BL is discharged through transistor N2 and during read '1' operation, BL does not discharge, since, it is in the similar voltage level at node Q. Table 2 clarifies that just a single path of the execution consumes power which is for the read '1' operation while for read '0' the power utilization is 0. Because of the reason, the access time for read '0' operation is additionally dropped

Table 1: Write power for different input

Transition	Write power consumption (μW) 6T	7T	11T
0->1	4.938	5.073	0.899
1->1	0.017	0.018	0.004
1->0	4.944	0.987	0.903
0->0	0.016	0.004	0.004

Table 2: Read access time

	Read access time (psec) Read '1'	Read '0'
6T	80	80
7T	80	91
11T	16	82

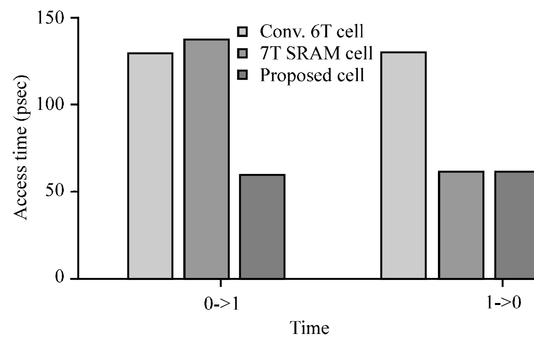

Fig. 3: Write access time

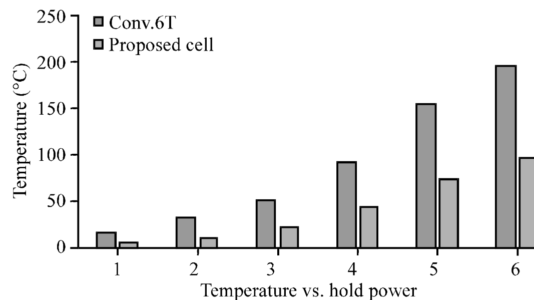

Fig. 4: Temperature vs. hold power

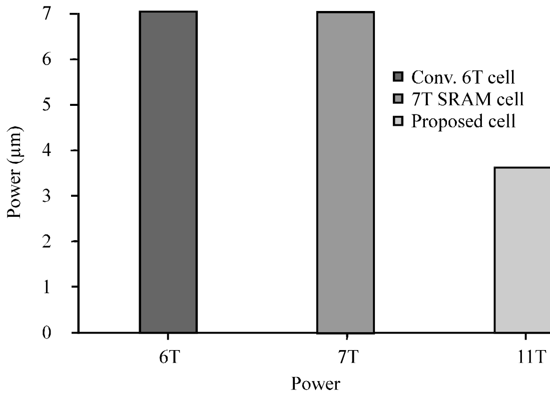

Fig. 5: Read power

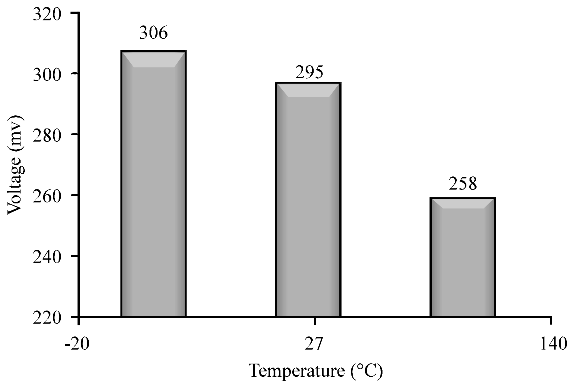

Fig. 6: Static noise margin

Table 3: SNM for different V_{TH}

	SNM (mV)	
V_{TH}	Conv.6T	11T cell
0.3	-	287
0.4	85	295
0.7	-	309

radically as compared with 6 and 7T cell. In light of lower voltage drop on the read bit-line, the average percentage of read power decrease is 49.1% in contrast to other cells. The bar graph in Fig. 5 shows the read power consumption at temperature ranging from 27-140°C is about 50% (half) of the other two cells. Due to individual read and write circuit path, the SNM of the 11T cell is higher compared to 6T cell as illustrated in Fig. 6. The decrease in SNM value for the tested temperature range (-20-140°C) is only 17.6% because of carrier diffusion which increase the change in current when temperature increases. Table 3 shows the read SNM at different Threshold Voltage (V_{TH}). At VT_H = 0.4, the SNM value of the proposed design is 295 mV compared to 85 mV of the 6T cell. The changes in SNM from low to high V_{TH} is about 7.1%. Slight variation occurs due to leakage current in the circuit. Overall, there and are no drastic changes in SNM value for different temperature and V_{TH} value.

CONCLUSION

The Novel 11T cell saves up to 49% power during read operation and 80% during write operation compared to the conventional SRAM cell. Based on the simulation results, the Novel 11T SRAM cell allows minimal stability loss and able to operate at worse condition (T = 140°C). The objective of the study is achieved by presenting a new technique where the original circuit is introduced with two bridging transistors. Separate path for read operation enhance the read stability, access delay and power consumption. Therefore, the proposed 11T SRAM cell can be power efficient and provides high speed during read and write operation compared.

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