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Low Power Single-Rail Domino Logic Full Adder Design

[1]Shashikanth Reddy, [1]U. Somanaidu, [1]D. Khalandar Basha and [2]D.M.K. Chaitanya
[1]Institute of Aeronautical Engineering College,
Department of Electronics and Communication Engineering, Dundigal, Hyderabad, India
[2]Vardhaman College of Engineering, Shamshabad, Hyderabad, India

Abstract: The purpose of this research is to analysis and design of single rail domino logic full adder with static and dynamic logic styles. In the research we are going to explain the five different logic styles with XOR/XNOR gates is the gate is the most fundamental gate in the adder circuit namely full static CMOS logic, Complementary Pass-Transistor Logic (CPL) and dual-rail Domino dynamic logic in compare with single-rail Domino dynamic logic are implemented. Proposed adder is implemented with 12 transistor knows as single rail Domino logic circuit. Proposed system is designed in cadence virtuoso tool simulations and calculation of power and delay calculated in 45 nm technology with power supply and voltage across 1.0 V) at different temperatures.

Key words: Full static, pass-transistor, single-rail logic and dual-rail logic, Domino dynamic, power supply, transistor knows

INTRODUCTION

Most of the process technology studies for the low-voltage and low power applications are designed with different technologies like BiCMOS/CMOS but it will remain the dominant solution in the future. According the trends of VLSI by the year 2001 the technology was at 95 nm and by 2003 it is reduced again to 65 nm which says that the problem in manufacturing yield in overcome. The gate length will be reduced to 13 nm by 2016. Comming to power supply voltage in 2001 at 1.2 V and is expected to reduction to 0.9 V by 2007 it may even reduce to 0.6 V by 2016. The increasing the demand for low-power VLSI can be addressed at different design levels (Navi *et al*., 2008; Zimmermann and Fichtner, 1997) such as the architectural, circuit, layout and the process technology level. By taking all the important parameters consideration the governing the power dissipation, i.e., switching capacitance, transition activity and short-circuit currents which are strongly influenced by the chosen the logic style. In this section, these investigations are extended to a much wider set of logic gates and with that to arbitrary combinational circuits.

Implementations of Full adder circuit: The static CMOS full adder cell (26T) (Gao, 2011) is shown in Fig. 1. Consists of pull-up and pull-down networks. The PMOS transistors in pull-up network is the dual network of the NMOS transistors in pull-down network are connected. The advantage of CMOS logic is that it dissipates less dynamic power. The draw backs of static CMOS logic is the higher propagation delays and it required more number of transistors up to 2 n where n is the number of inputs. Some logic manipulations can help to reduce the tranisistor count. It also suffers from low fan-out capability (Kumar *et al*., 2012). This ciruit is designed by boolean expression as shown below equation sum expression and carry expression as:

$$SUM = (A\,XOR\,B)\,XOR\,Cin = (A \oplus B) \oplus Cin$$

$$COUT = A\,and\,B\,or\,Cin\,(A\,XOR\,B)$$

$$A.B+Cin\ \ A \oplus B$$

A	B	Cin	Sum	Cout
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Corresponding Author: Shashikanth Reddy, Institute of Aeronautical Engineering College,
Department of Electronics and Communication Engineering, Dundigal, Hyderabad, India

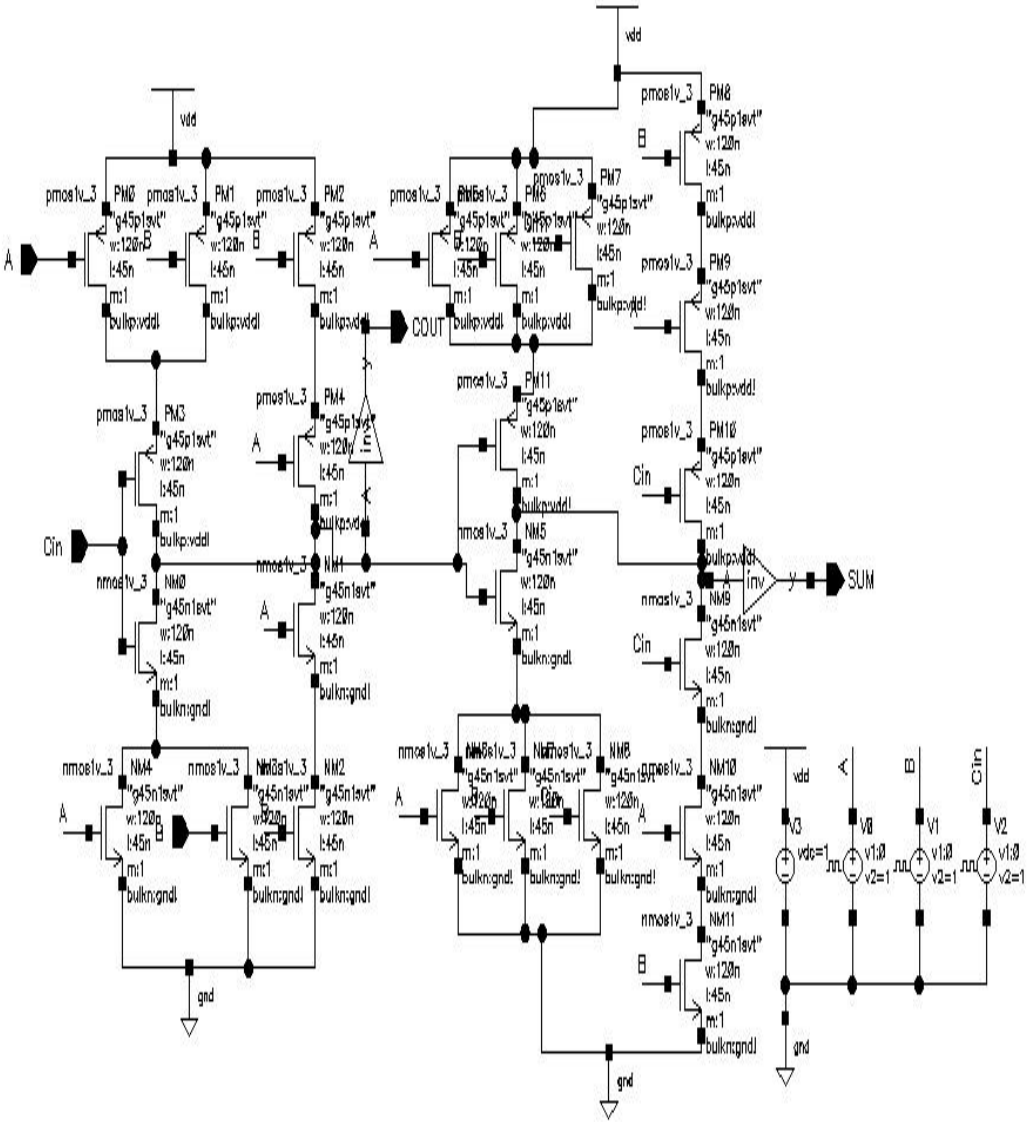

Fig. 1: Full static CMOS full adder circuit

Complementary Pass-transistor Logic (CPL) full adder has 15 transistors and is based on the CPL logic. A CPL logic full adder circuit is shown in Fig. 2. In the circuit, there are two small pull-up PMOS transistors for swing level restoration in the high-speed, full-swing level restoration factor of operation and good driving node capabilities due to the output static inverters and fast differential stage of cross coupled PMOS transistors when signal A is high, -A is low. Tranisistor pair P1 and N1 thus acts an inverter with -B appearing at the output. The tranmission gate formed by transistor pair P2 and N2 is open. When signal A is low, -A is high the transmission gate (P2, N2) is now closed, passing B to the output. The inverter (P1, N1) is partically disabled.

Dual-rail Domino logic gates: in this they are not many several limitation of not being able to implement inverting logic functions like NOR gate, NAND gate, XOR gate and high power required to generate the circuit due to clock signal. This circuit shows the pre-charged circuit technique by Neil and Harris (2011), Kang and Kim (2004) Dual-rail Domino system logic and its acts as pre charged circuit technique which is used to improve the speed of CMOS circuits. The main major drawback of the dual rail domino pre charged design styles over the static styles is that they eliminate the false transitions and the corresponding power dissipation. However, in dynamic circuits, additional power is dissipated by the distribution network and the drivers of the (Goel *et al*., 2006;

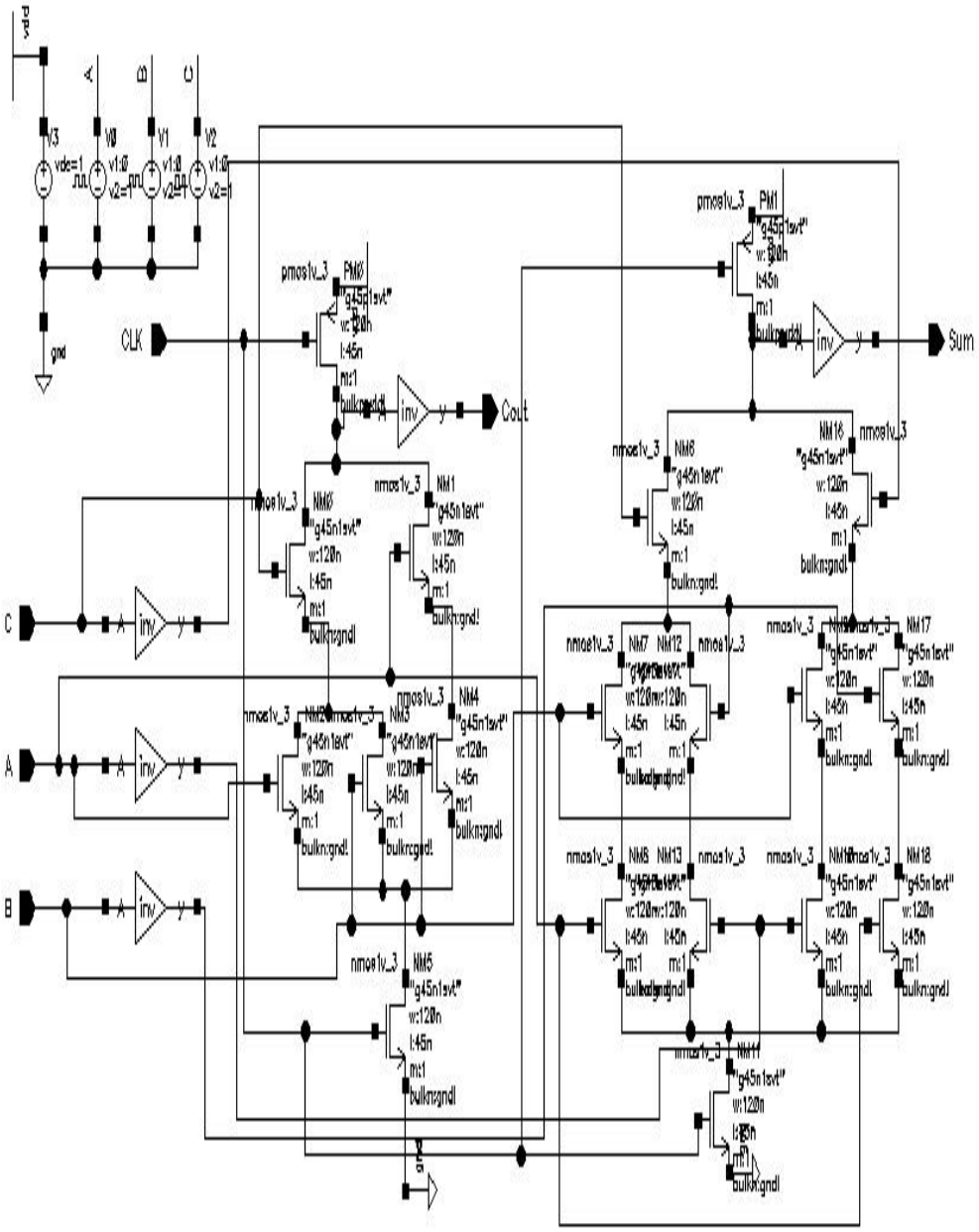

Fig. 2: CPL based full adder

Roy and Prasad, 2009; Yeo and Roy, 2004; Jia *et al*., 2013; Sun and Tsui, 1995) clock gating signal. This less power consumption and area than the previous circuits but the drawback is it requires more no. of transistors. Figure 3 shows about the dynamic dual adder.

The circuit of the high speed Domino logic full adder is shown in figure in high speed domino the keeper transistor is driven by a combination of the output node and a delayed clock. The circuit works sum output signal and the inverted sum output signal (Chandrakasan and Brodersen, 1995) and another two small pull-up PMOS transistors for swing restoration in the carry output as follows at the start of the evaluation phase delay thus keeper transistors will turn on to keep the dynamic node high, fighting the effects of leakage (Roy and Prasad, 2009; Yeo and Roy, 2004; Jia *et al*., 2013; Sun and Tsui, 1995; Wairya *et al*., 2012; Verma *et al*., 2012). It requires more no. of transistors compare to dual rail Domino logic adders circuit but it provides less power consumption and better area on the chip. Design is shown in Fig. 4-6.

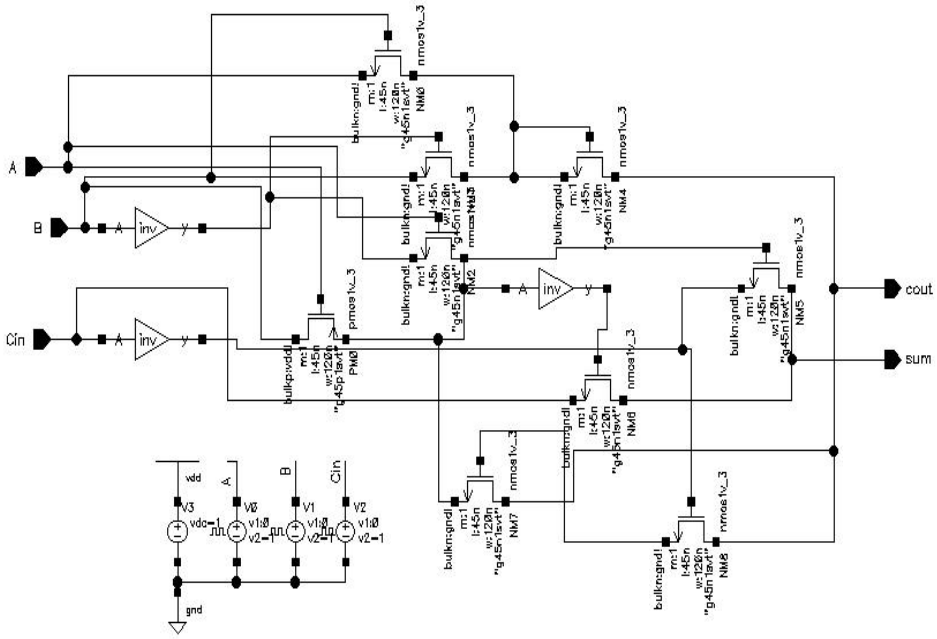

Fig. 3: Dynamic dual Domino based full adder

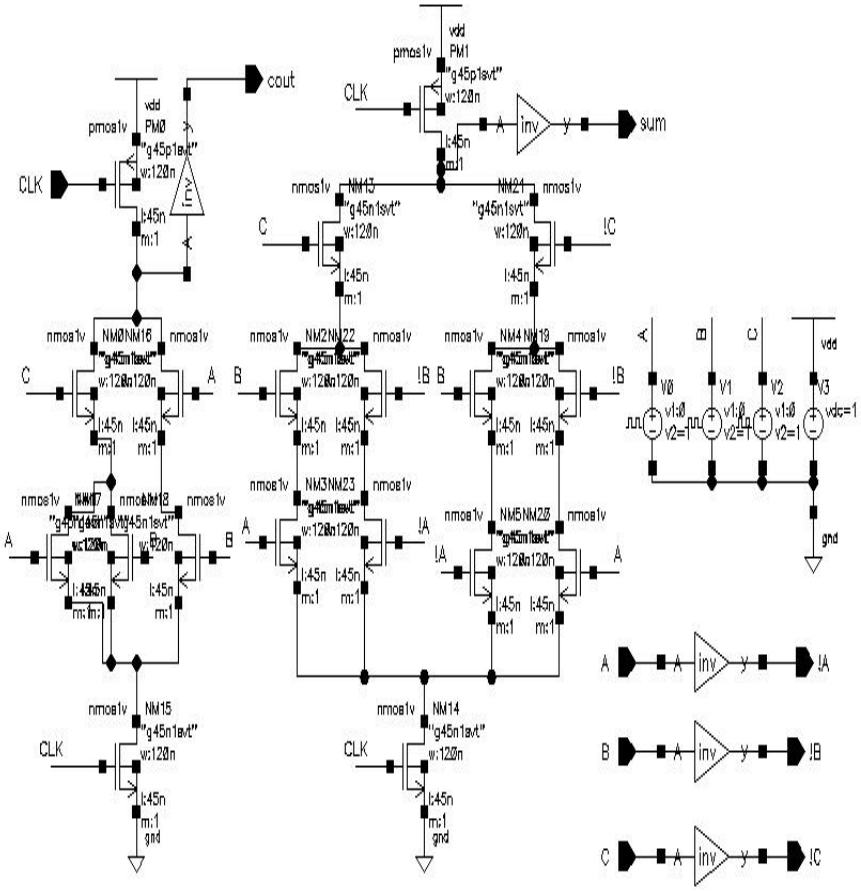

Fig. 4: Fast dynamic dual Domino based full adder

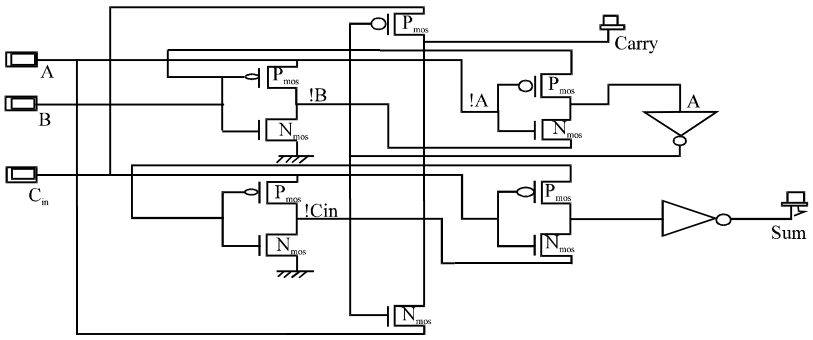

Fig. 5: Single-rail Domino of full adder using XOR gates

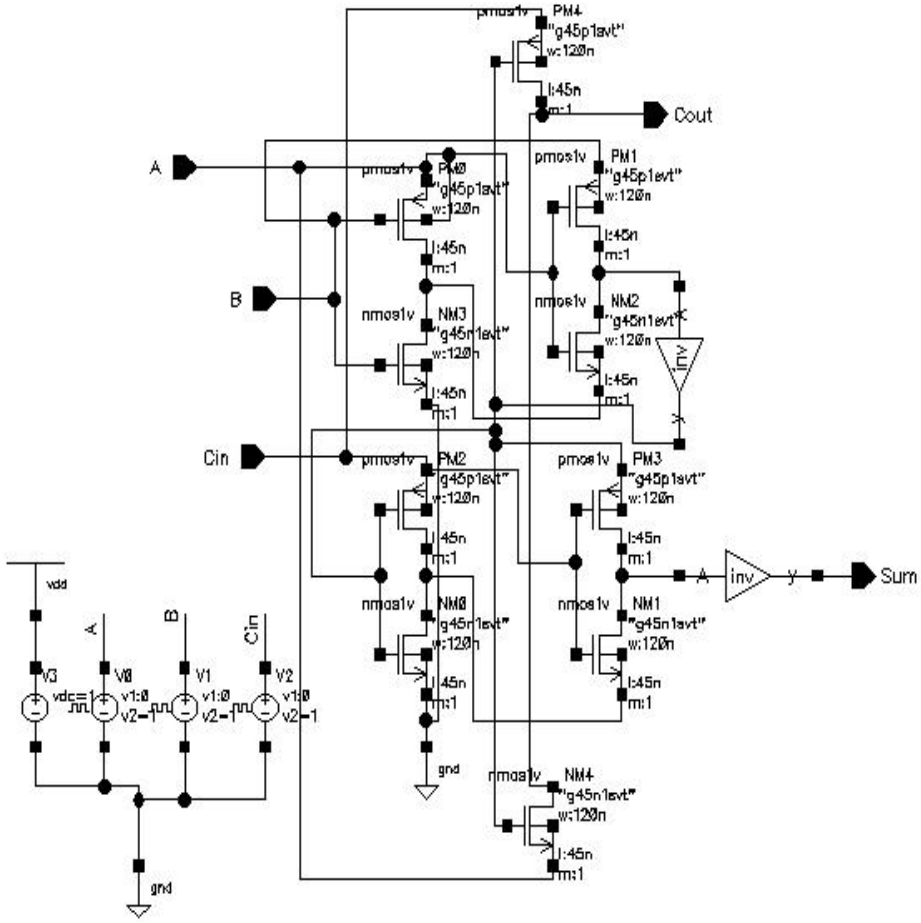

Fig. 6: Single rail Domino logic circuit based full adder in cadence

MATERIALS AND METHODS

Single rail domino logic full adder: In the Dual-rail inputs we discussed so far are useful for only XOR/XNOR gate implementation. But for other logic gates function such as NAND and NOR (Yeo and Roy, 2004; Jia *et al*., 2013) logic gates are the single-rail inputs are required. Figure 6 shows the NOR gate realization employing the single-rail Domino logic. The proposed architecture of single-rail Domino logic is methodology circuit designed. The proposed single-rail Domino logic circuit designed by using cadence virtuoso software these as shown in Fig. 6 and 7.

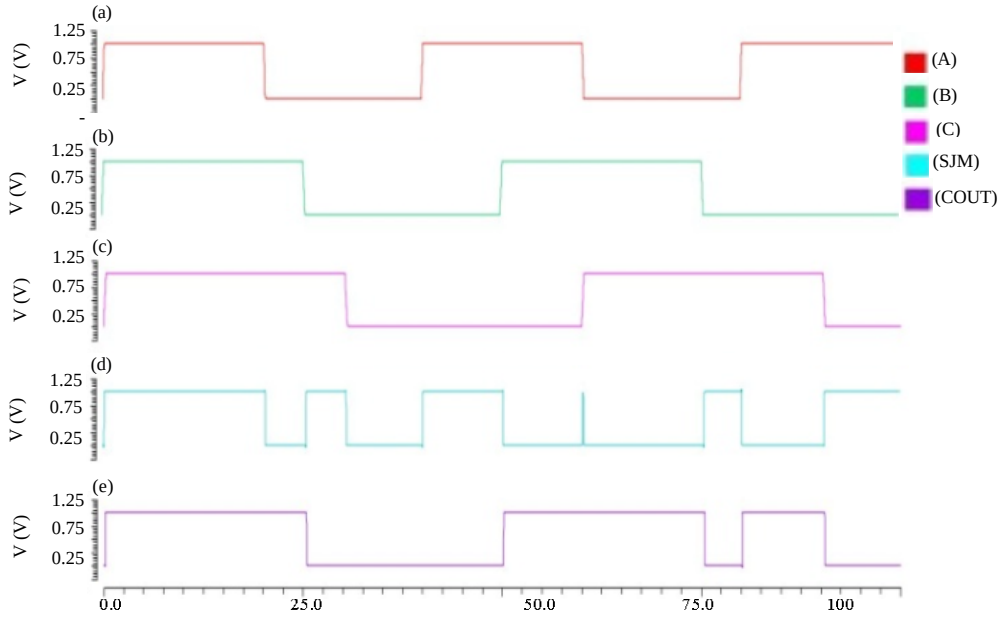

Fig. 7: Simulation results of full adder

RESULTS AND DISCUSSION

The circuit is simulated and analyzed using Cadence Virtuoso tool with GPDK 45 technology. The various full adders are analyzed for power, delay and power-delay product at various temperatures°C are tabulated.

Table1 shows the power, delay and Power Delay Product (PDP) of full static CMOS full adder Table 2 shows the power, delay and PDP of CPL full adder Table 3 shows the power, delay and PDP of dual rail domino logic full adder Table 4 shows the fast dual rail domino logic full Table 5 shows the proposed Single rail Domino logic full adder.

The proposed adder the power is decreased and slightly delay is increased. It is notice that the power-delay product is decreased. This can be used in the ALU to get high performance.

The full adders are designed with various pmos and nmos transistors like fast and slow configurations. Table 6 shows the power of different full adders by considering transistors as fast and slow type. The circuit is simulated for the configurations like fast-fast, slow-slow, fast-slow, slow-fast and static condition.

The circuit is designed in gpdk45 technology using Cadence virtuoso schematic editor and the simulations are done with Spectra tool. The functionality of the full adder is shown in Fig. 7. The delay power and power-delay product Histogram are shown in below (Fig. 8-10).

Table1: Power, delay and PDP of full static CMOS full adder

Temp (°C)	Power	Delay	PDP
250	8.96E-08	1.54E-11	1.38E-18
270	8.97E-08	1.54E-11	1.38E-18
300	8.99E-08	1.54E-11	1.38E-18
320	9.00E-08	1.54E-11	1.39E-18

Table 2: Power, delay and PDP of CPL based full adder

Temp (°C)	Power	Delay	PDP
250	9.92E-08	9.00E-11	8.93E-18
270	9.94E-08	9.00E-11	8.95E-18
300	9.97E-08	9.00E-11	8.97E-18
320	9.99E-08	9.00E-11	8.99E-18

Table 3: Power, delay and PDP of dual rail domino logic full adder

Temp (°C)	Power	Delay	PDP
25	7.46E-07	4.69E-08	3.50E-14
27	7.37E-07	4.69E-08	3.46E-14
30	7.59E-07	4.69E-08	3.56E-14
32	7.68E-07	4.69E-08	3.60E-14

Table 4: Power, delay and PDP of fast dual rail domino logic full adder

Temp (°C)	Power	Delay	PDP
25	7.08E-07	3.83E-11	2.71E-17
27	7.16E-07	3.83E-11	2.74E-17
30	7.27E-07	3.83E-11	2.78E-17
32	7.34E-07	3.83E-11	2.81E-17

Table 5: Power, delay and PDP of proposed single rail domino logic full adder

Temp (°C)	Power	Delay	PDP
25	1.60E-07	2.91E-12	4.66E-19
27	1.55E-07	2.91E-12	4.51E-19
30	1.67E-07	2.91E-12	4.86E-19
32	1.72E-07	2.91E-12	5.01E-19

Table 6: Power analysis of full adder

Full adder type	FF	SS	FS	SF	Static
Static CMOS	1.00E-07	8.06E-08	9.20E-08	8.61E-08	8.96E-08
PL CMOS	1.42E-07	7.36E-08	1.50E-07	1.41E-04	9.94E-08
Dual rail Domino logic	2.36E-06	2.43E-07	6.44E-07	1.04E-06	7.46E-07
Proposed fast dual rail Domino logic	2.27E-06	2.38E-07	6.42E-07	9.80E-07	7.15E-07
Proposed single rail Domino logic	3.02E-07	1.08E-07	1.97E-07	1.75E-07	1.60E-07

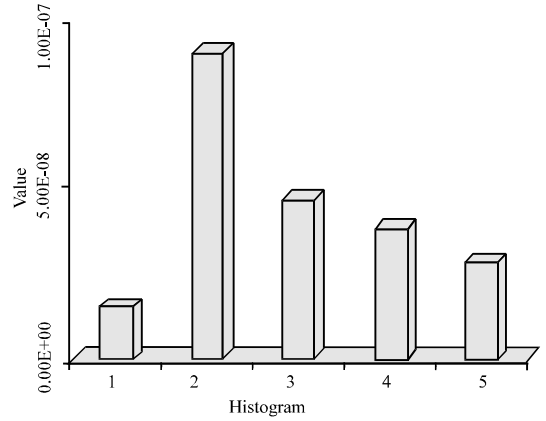

Fig. 8: Delay histogram for full adder

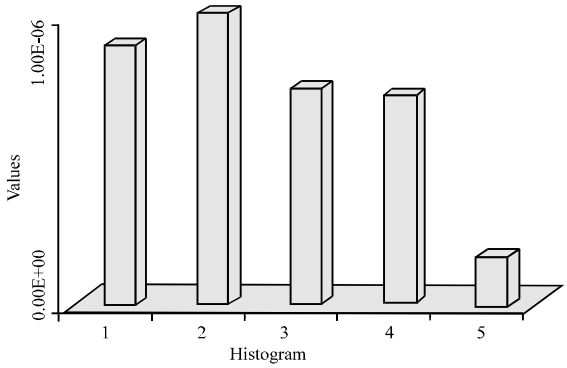

Fig. 9: Power histogram for full adder

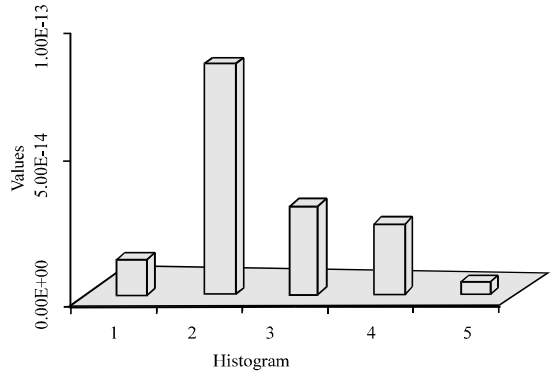

Fig. 10: Power-delay product histogram for full adder

CONCLUSION

In this study the various full adders like Static CMOS full adder, pass transistor full adder dual Domino logic full adder, high dual domino full adder and proposed single rail domino full adders are designed in 45 nm technology using GPDK 45 package. The circuit is simulated and analyzed using Cadence Virtuoso tool. The functionality is verified and the full adders are analyzed for power, delay and power-delay product at different temperatures and various transistor types. The proposed system has less power and less power-delay product. The proposed full adder can be used in ALUs and MACs for low power.

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