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Review on FPGA Implementation of 3D Distributed Arithmetic based DWT Architecture for Image Processing Applications

[1]Sukumar Beeda and [2]S. Chandra Mohan Reddy
[1]Department of ECE, JNTUA, Anantapuramu, Andhra Pradesh, India
[2]Department of ECE, JNTUA, College of Engineering, Pulivendula, Andhra Pradesh, India

Abstract: Image Processing (IP) is a method to perform some operations in the image for enhancing the clarity or extract the beneficial data from the image. Several methods are already available to enhance the quality of an image. Data transmission of an image is difficult when the size of the image becomes large. So, image compression is introduced the 3 Dimensional Discrete Wavelet Transform (3D DWT). The 3D DWT based image compression is used because of its higher coding efficiency and also better recovery of image. Image compression is used to compress the image size using either lossless or lossy image compression based methods. There are various compression methods available for reducing the image size. This study presented a survey of various methods which exist in the field of IP over FPGA and issues associated with individual methods.

Key words: Image processing, 3D-DWT, image compression, FPGA, digital images, methods

INTRODUCTION

An image compression system is used such as Context based Adaptive Variable Length Coding (CALVC) for 3D medical images. This CALVC used with the transform block including the 3D Integer Transform (IT) and DWT. The 3D DWT is used with Haar Wavelet transform (Ahmad *et al*., 2010a, b). For processing the infinite group of pictures, a lifting based parallel 3D DWT architecture is used. The working clock cycles of 3D DWT are minimized by using the two parallel spatial and temporal DWT modules (Darji *et al*., 2014). The 3D DWT comprises two types of feature extraction methods such as 3D sub band energy and 3D sub band overlapping cube. These methods are used for the classification of facial hyper spectral imagery and the datasets of feature vector are processed through the k-NN classifier. Distributive Arithmetic (DA) based parallel processor architecture is used in 3D DWT for minimizing the power consumption and storage space of the module. In this DA based 3D DWT module, the tap-merging technique is employed for reducing the size of DA look up tables. Based on the seperability property of the multi-dimensional haar and Daubechies, the DA based 3D DWT module is modified by using a cascade of 3 N-point one dimensional Haar/Daubechies and two transpose memories for a 3-D volume of N×N×N (Hegde and Vaya, 2011; Pandey and Behal, 2015; Ja'afar *et al*., 2013).

About 1-3D based DWT architectures are used for providing the time frequency representation that delivers a multi resolution outlook of the signal and these DWT structures also used for denoising the signal. The 3D DWT is widely used for medical applications because it gives high reconstruction property (Jarrah and Jamali, 2014). Designing of 3D DWT architecture is depends on the lifting scheme algorithm with 9/7 wavelet filters. By using the micro core engines, predict and update stages of lifting scheme are designed to improve the throughput. Lifting based 3D DWT is used without group of pictures restriction (Kumar *et al*., 2016; Das *et al*., 2010). Multiple watermarks algorithm such as 3D DWT DFT algorithm and it has no restriction of the amount of watermarks. The sign sequence of 3D DWT DFT algorithm is employed as a feature vector that is utilized to improve the robustness against JPEG compression, Gaussian noise, cropping attacks and median filer (Li *et al*., 2011). Overlapped grouping of frames is used in 3D DWT and the one level module does not allows a line buffer or frame buffer. The one level 3D DWT accepts only a frame buffer of size O (MN) for reducing the storage space (Mohanty and Meher, 2011).

The 3D Haar Wavelet Transform (HWT) is introduced with transpose based computation and DA mechanism is used for image compression on 3D medical images (Muharam and Ahmad, 2014). DA based 3D DWT structures are developed with Daubechies wavelet analysis bank filters dbN with N = 1, 2, …, 8. This

Corresponding Author: Sukumar Beeda, Department of ECE, JNTUA, Anantapuramu, Andhra Pradesh, India

architecture gives the higher efficiency in terms of resource utilization. Data transmission and sequence is handled by designing controllers, interfaces and protocols (Rivera-Juarico *et al*., 2012). Combination of 3D DWT with Set Partitioning In Hierarchical Trees (SPIHT) coding is used for compressing the Magnetic Resonance Imaging (MRI) images. The lifting based wavelet transformation is used in 3D DWT for improving the compression (Vakili and Khalili, 2015). The 3 Dimensional (3D) Haar Wavelet Transform (HWT) with transpose based computation and Dynamic Partial Reconfiguration (DPR) mechanism used in FPGA. This mechanism is used in a 3N-point one dimensional HWT and also in two transpose memories for a 3D volume of N×N×N suitable for 3D imaging applications (Ahmad *et al*., 2010a, b). A high precision low area lifting based architecture is introduced in the both lossy and lossless 3D multi-level Discrete Wavelet Transform (DWT). This system is improved by sharing the resource among the lossy and lossless models (Biswas *et al*., 2017).

Background of image processing: Image processing is a technique to improve the quality of an image or to obtain some information from the image. In IP the input is an image and the output should be an image or features/characteristics that is related to the image. Image processing developed in the year of 1960's for medical imaging, character recognition, satellite imagery, satellite imagery. After that, this process changed in the 1970's based on the low cost computers and dedicated hardware becomes available. From 1994-2000, the IP inducted in medical applications with faster computers. The 3D DWT is used in IP for reducing the hardware requirement and computation time and also it gives better quality of the image. The 3D DWT based IP generally includes 5 processes such as image display and printing, image editing and manipulation, image enhancement, feature detection and image compression.

Why FPGA in image processing?: The FPGA has the capability to perform in parallel input and output that allows to perform the operation of read and write simultaneously.

FPGA gives flexibility to reprogram and also improvement of new standards. The FPGA solutions grow quickly with no risk of undesirability by upgrading the FPGA in easy manner. Some convolution masks as the constant coefficient multiplier is implemented very efficiently by Look Up Table (LUT) based architecture.

Redundant operations avoided when the FPGA resources have more operations like loop fusion and loop unrolling. FPGA has more computational speed over conventional general-purpose hardware (Mittal *et al*., 2008).

MATERIALS AND METHODS

The 3D DWT architecture: The 3D discrete wavelet transform is performed by designing the flexible hardware architecture (Muniraj, 2016). Distributive Arithmetic (DA) algorithm is used in this 3D DWT. This DA algorithm has the capacity to perform the progressive computations by decreasing the buffering among the decomposition levels.

The 3D DWT is computed by processing a group of frames of size 8×8×8 with the DA algorithm. This 8×8×8 is processed in the first level of 3D DWT and second level processes the 4×4×4 size (LLL) component. Furthermore, this data's are decomposed into eight sub bands in the size of 2×2×2. The decomposition level of 3D DWT is shown in Fig. 1.

By applying three separate one dimensional transforms through the coordinate axis of image, the 3D DWT is being processed. The 3D data's are usually organized in the frame by frame manner. In that data's, the single frame has again rows and columns as like 2D case such as x and y direction often represented as spatial coordinates. Additionally, theses data's have one more dimension such as z axis which has time co-ordination for respective data. The order of the filtering does not matter in 2D decompositions. In the next decomposition step, only the approximation data of three 1D filtering along y, x and z-axis, one decomposition step results in 8 frequency sub bands and frame by frame 2D filtering being processed. DWT processor is build the 1D DWT modules, that comprises of low pass and high pass filters. These filter has to perform a convolution of filter coefficients and input pixels. After performing a one-level of 3D discrete wavelet transform, the volume of frame data is decomposed into HHH, HHL, HLH, HLL, LHH, LHL, LLH and LLL signals and it is shown in Fig. 2. The filtered results down sampling is represented as "↓2" that can be decomposed into smaller data along multi-level image decomposition processes. In Fig. 2, the H-pass and

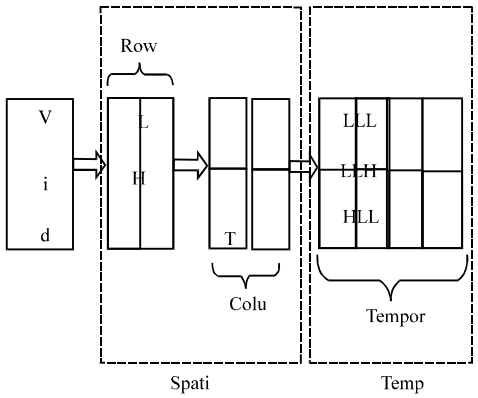

Fig. 1: Block diagram for 3D 1 level DWT decomposition

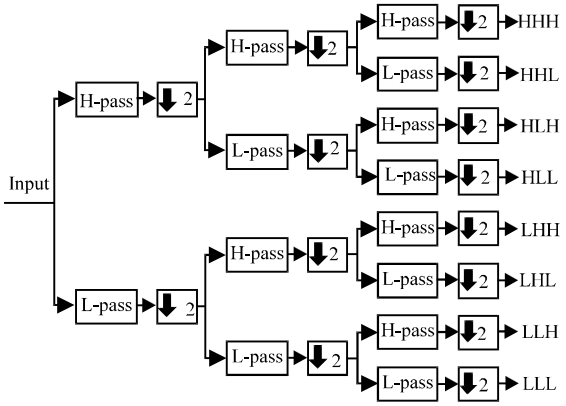

Fig. 2: Structure of one level 3D-DWT

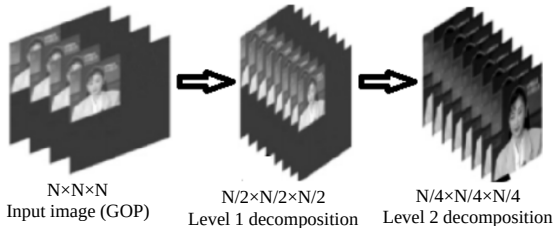

Fig. 3: Two level 3D decomposition

L- pass represents the high pass and low pass filters, respectively and also, Fig. 2 shows the two level decomposition of group of frames using 3D DWT. In first level, first set of frames of size 8×8×8 is decomposed into eight sub bands 4×4×4 and in second level the LLL component is decomposed into eight sub bands of size 2×2×2. The two level 3D decomposition is shown in Fig. 3.

RESULTS AND DISCUSSION

Image compression on FPGA: Image compression over 3D DWT is a method for decreasing the amount of data used to represent the digital image. This image compression is applied when the amount of data related to the visual information becomes large and it is used for the compact representation of an image storage or transmission is possible.

Principles behind compression: The amount of bits required to denote the information of an image is decreased by neglecting the redundancy that is present in the desired image. The redundancies are classified into three types such as spatial, spectral and temporal redundancies.

Spatial redundancy: Spatial redundancy happened due to the correlation or dependency among neighboring pixel values.

Spectral redundancy: Spectral redundancy created based on the correlation among various color planes or spectral bands

Temporal redundancy: Due to the correlation between frames of images, the temporal redundancy exists in the image processing.

Types of image compression: Image compression is broadly classified into two types such as lossless and lossy image compression. The better quality of the image is given only by lossless compression because high ratio compression in lossy compression methods and the decompressed image of lossy compression is not similar to the original image. So, only the lossless compression techniques are explained in this review.

Lossless image compression: Lossless image compression is a technique that retrieves the original image from the compressed image. It is used for minimizing the redundancy which is present in the image. This kind of compression is mainly used in medical imaging where the clarity of the image does not degrade due to the compression. The following compression techniques are going under the lossless compression such as run length coding, Huffman coding, LZW coding and area coding. Here, some of the methods are explained. Here, some of the lossless compression techniques are explained (Prakash and Gurumurthy, 2012).

Run length coding: String type of data are coded by the RLE method and the compression of RLE is functioned by counting the amount of adjacent pixels with the same gray-level value. The coefficients are encoded as a run length using the RLE in the quantized block. The amount of the count called as the run length. After that, the run length is coded and then loaded. The amount of pixels decides the amount of bits coded in the RLE. The block diagram and the internal architecture of run length encoding is given in Fig. 4a-c. Additionally, the data are compressed by defining many of the coefficients into zero. If there are no more non-zero coefficients, the coding is terminated by the end-of block. Input of the run length decoding is in the form of run/value combination. Consequently, the input is divided into run and value parts. Run represents the amount of zeroes present to output before sending out the non-zero level value in the run/value combination. Finally, the image which is encoded in the run length encoder is retrieved by run length decoder is given in Fig. 4b.

Huffman coding: Huffman coding produce the code as close as possible to the minimum bound and to the

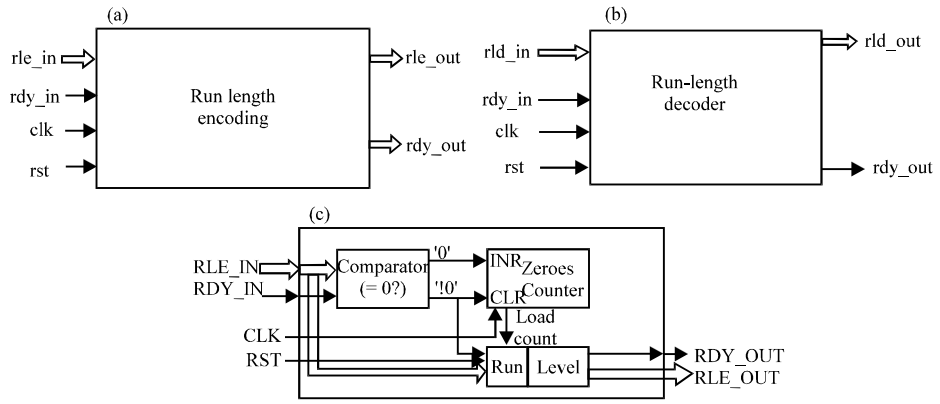

Fig. 4: a) Run length encoder; b) Run length encoder and c) Run length encoder internal architecture

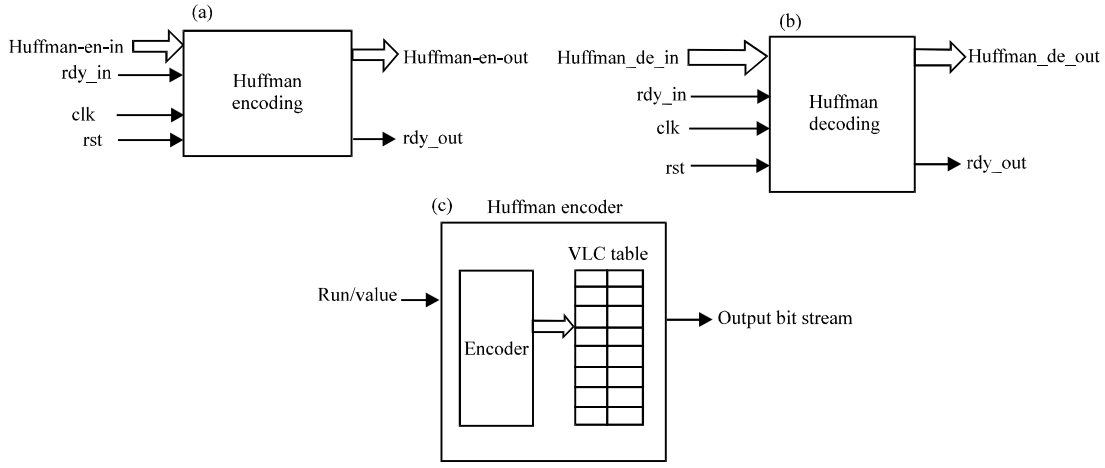

Fig. 5: a) Huffman encoder; b) Huffman encoder and c) Huffman encoder internal architecture

entropy. The occurrence probability decides the code values of Huffman encoding. Long code words and short code words are allotted to less and high probable value, respectively. Run/value combination pairing decide by Huffman coding which generated in decreasing probability. Correspondingly, the highest probability and less probability of run/value combination is given at the top and bottom of Huffman encoder. From that probability values, two least values are first paired and then added to generate the new probability value. Formation of new probability list is made by one entry as the previously added pair as well as the least run/value combinations in the new list is paired. This procedure sustains until the entire values become only one probability value. In each element the values 0 and 1 are arbitrarily allocated in each of the lists. The Look UP Table (LUT) is used for performing the Huffman encoding and the LUT is formed by the different run/value combination. The design of the Huffman encoder is simple and it requires less power consumption. The block diagram and internal architecture of the Huffman encoder is shown in Fig. 5c. The internal architecture of the huffman encoder is identical to the Huffman decoder as well as the Huffman decoder uses the VLC Huffman coding table which is used by the Huffman encoder. Huffman decoding the next coming input when the corresponding run/value combination is discovered and it is delivered to the output. Huffman decoder design is shown in the Fig. 5b. The results of this method carried in variable length coding. The compression ratio of Huffman coding is in the range of 10-50%.

Major issues in 3D image processing over 3D DWT: The major issues present in the image processing over FPGA as listed below (Table 1).

Hardware complexity: The system becomes unreliable, when it includes a more number of hardware components. Because the presence of hardware components consumes more space.

Table 1: Merits and demerits of the respective methods

Researchers	Title	Hardware resources	Clock frequency	Hardware used	Advantage	Disadvantage
Papadhopulli and Cico (2013)	Implementation in FPGA of 3D discrete wavelet transform for imaging Noise removal	Slices: 422 Flip Flops (FFs) LUTs: 907	-	FPGA	Less hardware resources are required	Difficulttoperfectreconstruction and alias cancellation
Mohanty and Meher (2011)	Memory-efficient architecture for 3-D DWT using overlapped grouping of frames	Slices: 13662 FFs: LUTs	40 Mhz	FPGA	Due to its less memory complexity,less dynamic power dissipated	High hardware resources are required, due to its adder complexity.
Darji *et al.* (2014)	Hardware efficient VLSI Architecture for 3-D Discrete Wavelet transform	Slices: 2490FFs LUTs:	91.87 MHz	FPGA	High throughput	Slight increase in area
Kumar *et al.* (2016)	Pipeline and parallel processor architecture for fast computation of 3D-DWT using modified lifting scheme	Slices: 49645 FFs: LUTs	373 MHz	FPGA	Low power consumption	Computation time is increased.
Venkateshappa *et al.* (2016)	An efficient VLSI architecture of 1D/2D and 3D for DWT based image compression and decompression using a lifting scheme	Slices: 244 LUT and FF pair:1749	254.58 Mhz	FPGA	High compression ratio in image compressing	High hardware resources are required
Vijayakumar and Ramachandran (2013)	FPGA approach for lossless compression of medical images using three-dimensional wavelet transform	Slices: FFs: LUTs:	-	FPGA	Less MSE and also color image compression is achieved	Storage and processing of data requires more cost
Roopa *et al.* (2016)	Design of enhanced 3D-Dwt for image transformation	Slices: FFs: LUTs:	-	FPGA	Less hardware cost	Processing time of the desired system is more.
Huang *et al.* (2011)	High-performance FPGA implementation of discrete wavelet transform for image processing	Slices: FFs: LUTs:	389.71 MHz in db8 wavelet (1D DWT)	FPGA	Compatibility in different wavelet types and maximum clock frequency.	More resources are occupied when the DWT has arbitrary wavelet with 16 orders
Chandrasekhar and Reddy (2012)	FPGA implementation of systolic array architecture for 3DDWT optimizing speed and power	Slices: 6059/ 13696 FFs: 5222/27392LUTs: 8025/27392	160.051 Mhz	FPGA	Less area and power consumption.	It has maximum delay
Akshay *et al.* (2012)	Implementation Of 3D DWT with 5/3 LeGall filter for image processing	Slices: FFs: LUTs:	85.6 Mhz	FPGA	High throughput	Size of the memory is increased
Manjunatha (2016)	Lossless image compression using enhanced wavelet transform.	Slices: 492/ 63168 FFs:371/ 126336LUTs; 942/126336	357.500 Mhz	FPGA	Less memory requirement and fast computation in processing	High latency
Karthikeyan *et al.* (2013)	An efficient VLSI architecture for 3D DWT using lifting scheme	Slices: 1792/ 14752 FFs:160/ 29504 LUTs: 3491/29504	10.775 Mhz 350 MHz	FPGA	Power consumption is low by avoiding multiplication and accumulation.	Large computation time
Zhang *et al.* (2016)	Memory-efficient high-speed VLSI implementation of multi-level discrete wavelet transform	Slices: FFs: LUTs:	(2D-DWT)	FPGA	High throughput and less computation time.	Size of the design architecture is large

Low frequency: Low frequency is not essential for displaying high resolution images and the medical images like stones in the kidney, blood flowing through blood vessels and internal organs of the body.

Delay: Due to the number of overheads in the FPGA system, the delay increase for example the required time for transmitting (upload) and receiving from reconfigurable processor is high.

Less throughput: For an effective data transmission high throughput level is required. If more amount of noise occurred during the data transmission, it affects the performance of desired system.

Table 1 shows the analysis of various image processing methods over 3D DWT and also it discusses about the merits and demerits of the respective methods.

CONCLUSION

In image processing, 3D DWT based image compression plays a major role in reducing the size of the digital image to reduce the storage space. On the other hand, processing of images generates the image into high clarity and also it helps to obtain the beneficial data from the image. In this study, various processing and compressing techniques over the digital images are discussed. There are several 3D DWT based image

processing methods discussed in this review related to image noise removal, memory efficient architecture, modified lifting scheme, medical image compression, systolic array architecture and legall filtering in image compression. The comparative study validates the different techniques and their advantages, disadvantages and performance. The main issues of 3D DWT over 3D image processing are noticed.

RECOMMENDATIONS

From the analysis, we can conclude that the memory efficient architecture, modified lifting scheme, systolic array architecture and legall filtering in image compression are more efficient to generate the image with less hardware resources, low power consumption and high throughput.

LIMITATIONS

These methods also have some constraints like more computation time and less bandwidth, high hardware resources and more energy consumption.

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