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Design and Simulation of Zeta Converter with ZVZCS Switching Technique

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Abstract: This study deals with the design of Zeta converter with ZVZCS switching technique for better efficiency, lower total harmonic distortion factor and power factor correction. It requires simpler control circuitry with fewer external components added with SEPIC converter. The basic operation of Zeta converter is explained and PI filter is used to reduce the harmonics. Like SEPIC DC/DC converter topology, the Zeta converter topology also provides a positive output voltage from an input voltage for boost and buck purposes. Inverse of Cuk converter. ZVZCS switching technique is used to reduce the THD. The performance of Zeta converter in open loop and closed loop is obtained using MATLAB Simulink. Zeta converter in closed loop shows better performance than open loop. The performance of Zeta converter is compared by comparing both open loop and closed loop. Zeta converter in closed loop has low THD value and power factor near to unity.

Key words: Zeta converter, THD (Total Harmonics Distortion), PFC (Power Factor Correction), ZVZCS (Zero Voltage Zero Current Switching), MATLAB Simulink, performance

INTRODUCTION

The traditional technique for AC-DC change utilizing an uncontrolled rectifier with one capacitor is not utilized as a part of because of issues, harmonic injection into AC control supply, poor power factor, high peak current, line voltage distortion, expanded EMI, additional burden and losses on lines. The advancement of power electronics of solid-state switch mode amendment converters has achieved an unmistakable level for enhancing power quality issues in the terms Power-Factor Correction (PFC) and reduced Total Harmonic Distortion (THD). The typical DC-DC converter topology utilizes boost converter, buck- converter, buck-boost converter, SEPIC and Cuk converter have their extraordinary constraints when they were utilized for a dynamic PFC alongside voltage regulation issues (Hu and Gong, 2015; Govindaraju *et al*., 2017; Koutroulis and Blaabjerg, 2012; Tao *et al*., 2008; Erickson and Maksimovic, 2007; Amudha *et al*., 2017a, b; Ramkumar *et al*., 2017a, b; Ramkumar, 2017).

In the proposed Zeta converter moderately new class of DC-DC converter is utilized for dynamic PFC and voltage direction. The value of being a segregated circuit, can work as both step up voltage and step down voltage of converter and having single stage (Govindaraju *et al*., 2017).

MATERIALS AND METHODS

Zeta converter: Power handling for both voltage regulation and power factor correction. The Zeta converter plays out an operation of non-modifying buck-boost similar that of a DC-DC SEPIC converter. But an application which requires more power, then the operation of a SEPIC converter is irregular mode. It is not alluring in light of the fact that it brings about high Root Mean Square (RMS) estimations of the currents creating elevated amounts of worry in the thyristor. In this proposed concept, a dynamic PFC is performed by utilizing a DC-DC Zeta converter working in Continuous Conduction Mode (CCM) where the furthermore included inductor current will take after the sinusoidal voltage waveform (Subramanian *et al*., 2017; Prabha *et al*., 2017; Yuvaraj *et al*., 2017; Ravichandran *et al*., 2017; Latha *et al*., 2017; Sivakumar *et al*., 2017; Krishnan *et al*., 2017; Kumar *et al*., 2016; Krishnan and Ramkumar, 2016) (Fig. 1).

Principle of operation: Examining on DC-DC converter Zeta waveforms it demonstrates that at equilibrium inductors L_1 normal current equivalents I_{IN} and inductor L_2 normal current equivalents output current IOUT, since, the i DC current through the flying capacitor CFLY is additionally same. Likewise there Stage-1[M_{ION}].

The switch's M_1 is in the ON state, so that, the voltages of V_{L1} and V_{L2} are equivalent to V_{in}. In this day and age at interval Diode D_1 is in OFF state with a switch

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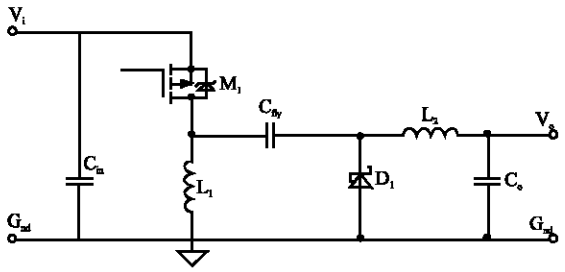

Fig. 1: Zeta converter

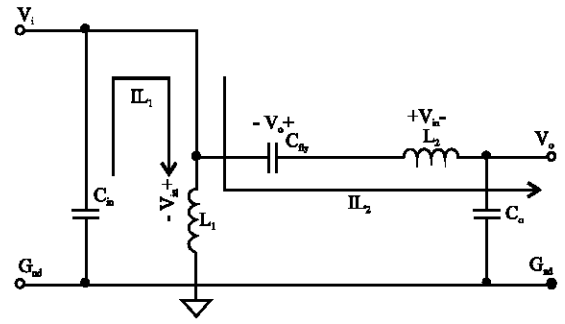

Fig. 2: Zeta converter during MOSFET ON time

voltage equivalent to (V_{in}+V_O) input voltage and output voltage. Inductor L_1 and L_2 get supply from the voltage source and their separate Inductive currents I_{L1} and I_{L2} are which is expanded straight upto proportion V_{in}/L_1 and V_{in}/L_2 individually. Correspondingly, the switch current I_{M1} = I_{L1}+I_{L2} is expanded step by step by a proportion of V_{in}/L where, L = $L_1.L_2/(L_1+L_2)$. Amid this period, the releasing of capacitor C_{fly} and charging of Capacitor C_0 happens. Stage-2 [M_1 OFF] (Fig. 2).

In this stage, the switch M_1 turns OFF and the D_1 Diode is in forward biased which starts to conducting. The voltage across the inductor L_1 and L_2 becomes equal to -V_o and inductor L_1 and L_2 transfer power to the Capacitor C_{fly} and the load simultaneously. The current of in the L_1 and L_2 decreases now gradually by a ratio of -V_0/L_1 and V_0/L_2. The current in the diode I_{D1} = I_{L1}+I_{L2} also gets decreases by a linearly by ratio of -V_0/L. At this period, the Voltage (V) across switch M_1 is V_M = V_{in}+V_0. Figure 3 shows the inductor current waveforms of the Zeta converter for an one cycle of operation in the steady state continues mode (Krishnan and Ramkumar, 2016; Sudhakar and Ramkumar, 2016; Sownthara and Ramkumar, 2016; Ramkumar and Krishnan, 2014; Krishnan *et al*., 2014; Sriragavi *et al*., 2017; Emayavaramban and Amudha, 2006a, b) (Fig. 4).

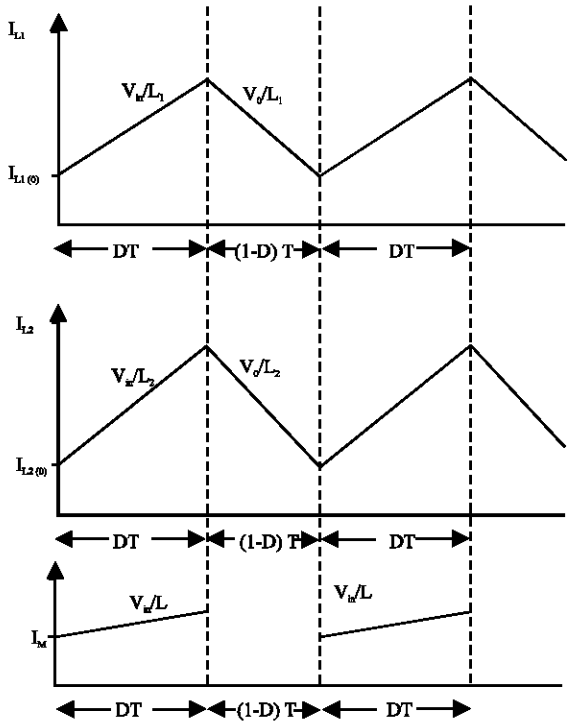

Fig. 3: Zeta converter waveforms

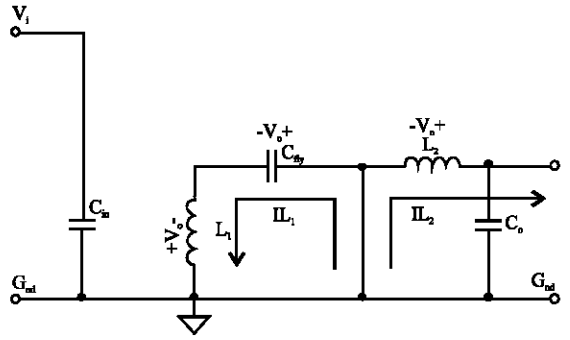

Fig. 4: Zeta converter during MOSFET off time

Design of components of Zeta converter: A Zeta converter plays out a non-altering buck-boost work. For a Zeta converter working in CCM, the duty cycle is characterized as:

$$D = \frac{V_{OUT}}{V_{IN}+V_{OUT}} \quad (1)$$

$$\frac{D}{1-D} = \frac{I_{IN}}{I_{OUT}} = \frac{V_{OUT}}{V_{IN}} \quad (2)$$

D_{max} occurs at $V_{IN(min)}$ and D_{min} occurs at $IN^{(max)}$

By Hu and Gong (2015) one of the initial phases in outlining any PWM switching controller is to choose how

much inductor ripple current, ΔI_L (PP), to permit. An excessive amount of builds EMI while too little may bring about unsteady PWM operation. A dependable guideline is to relegate an incentive for K between 0.2 and 0.4 of the normal info current (Ramkumar *et al*., 2014a, b, 2016; Kavitha and Vivekanandan, 2015; Kavitha *et al*., 2017; Manoharan and Amudha, 2015a, b; Vijayalakshmi *et al*., 2014a, b, 2015; Bhavithira and Amudha, 2014; Amudha, 2014).

In a perfect, firmly coupled inductor with every inductor having a similar number of windings on a single core, the coupling force the ripple current to be part similarly between the 2 coupled inductors. In a genuine coupled inductor, the inductors don't have meet same inductance value and the ripple current won't be precisely equivalent. In any case for a desired ripple current value, the inductance required in a coupled inductor is assessed to be half of what might be required if there were 2 separate inductors as appeared in Eq. 3 (Erickson and Maksimovic, 2007):

$$L1a_{min} = L1b_{min} = \frac{1}{2} \times \frac{V_{IN} \times D}{\Delta I_{L(PP)} \times f_{SW(min)}} \quad (3)$$

To represent load transient, the coupled inductor's immersion current rating should be no <1.2 times the steady-state peak current in the high-side inductor as processed in Eq. 4 (Subramanian *et al*., 2017):

$$I_{L1a\,(PK)} = I_{OUT} \times \frac{D}{1\text{-}D} + \frac{\Delta I_L}{2} \quad (4)$$

where, $I_{L1}b\,(PK) = I_{OUT} + \Delta I_L/2$ which is $< I_{L1}a\,(PK)$. Like a buck converter, the output of a Zeta converter has very low ripple. Equation 5 processes the part of the output ripple voltage that is expected exclusively to the capacitance value:

$$\Delta V_{C_{OUT}\,(PP)} = \frac{\Delta I_{L1b\,(PP)}\,[\text{at } V_{IN\,(max)}]}{8 \times C_{OUT} \times f_{SW(min)}} \quad (5)$$

where, $f_{SW(min)}$ is the minimum switching frequency. Equation 6 computes the component of the output ripple voltage that is due solely to the output capacitor's ESR (Koutroulis and Blaabjerg, 2012):

$$\Delta V_{ESR\_C_{OUT}\,(PP)} = \Delta I_{L1b\,(PP)}\,[\text{at } V_{IN\,(max)}] \times ESR_{C_{OUT}} \quad (6)$$

These 2 ripple-voltage components are phase shifted and do not directly add together. The output capacitor must have a RMS rating more prominent than the capacitor RMS current registered in Eq. 7 taking after:

$$I_{C_{OUT}\,(RMS)} = \frac{\Delta I_{L1b\,(PP)}\,[\text{at } V_{IN\,(max)}]}{\sqrt{3}} \quad (7)$$

The input capacitor and the coupling capacitor source and sink the same current levels but on opposite switching cycles. Similar to a buck converter, the input capacitor and the coupling capacitor need the RMS current rating (Eq. 8) (Prabha *et al*., 2017):

$$I_{C_{IN}\,(RMS)} = I_{C_C\,(RMS)} = I_{OUT}\sqrt{\frac{V_{OUT}}{V_{IN\,(min)}}} \quad (8)$$

Equation 9 and 10 compute the component of the output ripple voltage that is due solely to the capacitance value of the respective capacitors:

$$\Delta V_{C_{IN}\,(PP)} = \frac{D_{max} \times I_{OUT}}{C_{IN} \times f_{SW(min)}} \quad (9)$$

$$\Delta V_{C_C\,(PP)} = \frac{D_{max} \times I_{OUT}}{C_C \times f_{SW(min)}} \quad (10)$$

Equation 11 and 12 compute the component of the output ripple voltage that is due solely to the ESR value of the respective capacitors:

$$\Delta V_{ESR\_C_{IN}\,(PP)} = \left(I_{IN\,(max)} + I_{OUT}\right) \times ESR_{C_{IN}} = \frac{I_{OUT}}{1\text{-}D_{max}} \times ESR_{C_{IN}} \quad (11)$$

$$\Delta V_{ESR\_C_C\,(PP)} = (I_{IN\,(max)} + I_{OUT}) \times ESR_{C_C} = \frac{I_{OUT}}{1\text{-}D_{max}} \times ESR_{C_C} \quad (12)$$

Again, the 2 ripple-voltage components are phase-shifted and do not directly add together and for low-ESR capacitors, the ESR component can again be ignored. A typical ripple value is <0.05 times the input voltage for the input capacitor and <0.02 times the output voltage for the coupling capacitor (Balachander and Ponnusamy, 2012a, b; Balachander *et al*., 2012a, b; Balachander, 2012; Kuppusamy and Balachander, 2012; Ramkumar *et al*., 2018; Balachander and Amudha, 2017a, b; Sriragavi *et al*., 2017; Amudha *et al*., 2017a, b, 2012; Motapon *et al*., 2014; Kochcha and Sujitjorn, 2010; Singh and Chaturvedi, 2008).

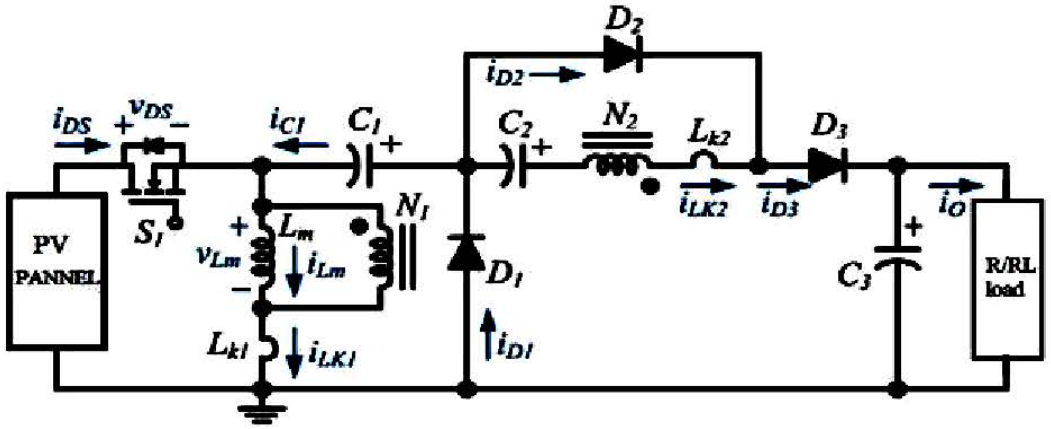

Fig. 5: Proposed Zeta converter

Converters operating principles of the proposed: Figure 3 demonstrates the circuit design of the proposed converter which comprises of two dynamic switch S_1, one coupled inductor, 3 Diodes D_1~D_3 and 3 Capacitor C_1~C_3. The coupled inductor is displayed as a charging inductor L essential spillage inductor L_{k1}, secondary leakage inductor L_{k2} (Fig. 5).

All parts are perfect. The On-state resistance RDS (ON) of the dynamic switches, the forward voltage drop of the diodes and the comparable arrangement resistance (ESR) of the coupled-inductor and output capacitors are overlooked the turns proportion n of the coupled inductor T_1 winding is equivalent to N_2/N_1 Figure 4 demonstrates some run of the mill waveforms amid one exchanging period in Constant Conduction Mode (CCM) operation. The working standard and the 5 working modes are portrayed as takes after (Vijayalakshmi *et al*., 2014a, b; Amudha and Rajan, 2012; Amudha and Christopher, 2012; Christopher and Christopher, 2012; Amudha and Rajan, 2013, 2014; Balachander, 2017; Balachander and Amudha, 2017a, b; Sangeetha and Balachander, 2016; Balachander and Vijayakumar, 2013a-d).

CCM operation

Mode 1 [t_0, t_1]: In this interval the Capacitor C_2 get vitality energy from the secondary leakage inductor L_{k2}. The current way is appeared in Fig. 6a; Switch S_1 and Diodes D_2 are leading. The source Voltage V_{in} is connected on charging inductor L_m and essential spillage inductor L_{k1}, the current i_{Lm} is diminished in the meantime, Lm additionally discharges its vitality to the optional twisting and also charges the Capacitor C_2 alongside the lessening in vitality equation:

$$\begin{aligned} &i_m(t) = i_{DS}(t) = i_{Lk1}(t) \\ &\frac{di_{Lm}(t)}{dt} = \frac{V_{Lm}}{Lm} \\ &\frac{di_{Lk1}(t)}{dt} = \frac{V_{in}\text{-}V_{Lm}}{L_{k1}} \\ &i_{Lk2}(t) = i_{Lm}(t)\text{-}i_{Lk1}(t) \end{aligned} \quad (13)$$

Mode 2 [t_1, t_2]: During this interval, source vitality vinis associated in arrangement with C_1, C_2, optional winding N_2 and L_{k2} to charge output capacitor C_3 and load R in the meantime, polarizing inductor L_m additionally gets vitality from V_{in}. The way of current current is appeared in Fig. 6b as outlined, Switch S_1 remains on and just Diode D_3 is in conduction. The i_{Lm}, i_{Lk1} and i_{D3} have been expanding in light of the fact that the V_{in} is intersection L_{k1}, L_m and essential winding N_1; L_m and L_{k1} are putting away vitality from V_{in} and in addition, V_{in} is additionally in arrangement with N_2 of coupled inductor T_1 and Capacitors C_1 and C_2 have been releasing their vitality to Capacitor C_3 and load R that prompts to increments in i_{Lm}, i_{Lk1}, i_{DS} and i_{D3}. This mode closes at $t = t_2$ at which turn S_1 is off (Shaik and Babu, 2012; Martins *et al*., 1996; Tse, 2003; Singh *et al*., 2008; Martins and De Abreu, 1993; Garcia *et al*., 2003; Lascu *et al*., 2005; Anonymous, 2007):

$$\begin{aligned} &i_{Lm}(t) = i_{Lk1}(t)\text{-}ni_{Lk2}(t) \\ &\frac{di_{Lm}(t)}{dt} = \frac{V_{in}}{Lm} \\ &i_m(t) = i_{DS}(t) = i_{Lm}(t)+(1+n)i_{Lk2}(t) \\ &\frac{di_{Lk2}(t)}{dt} = \frac{di_{D3(t)}}{dt} = \frac{(1+n)V_{in}+V_{C1}+V_{C2}}{Lk2} \end{aligned} \quad (14)$$

Mode 3 [t_2, t_3]: During this move interval, C_3 is being charged from auxiliary spillage inductor L_{k2} when turn S_1

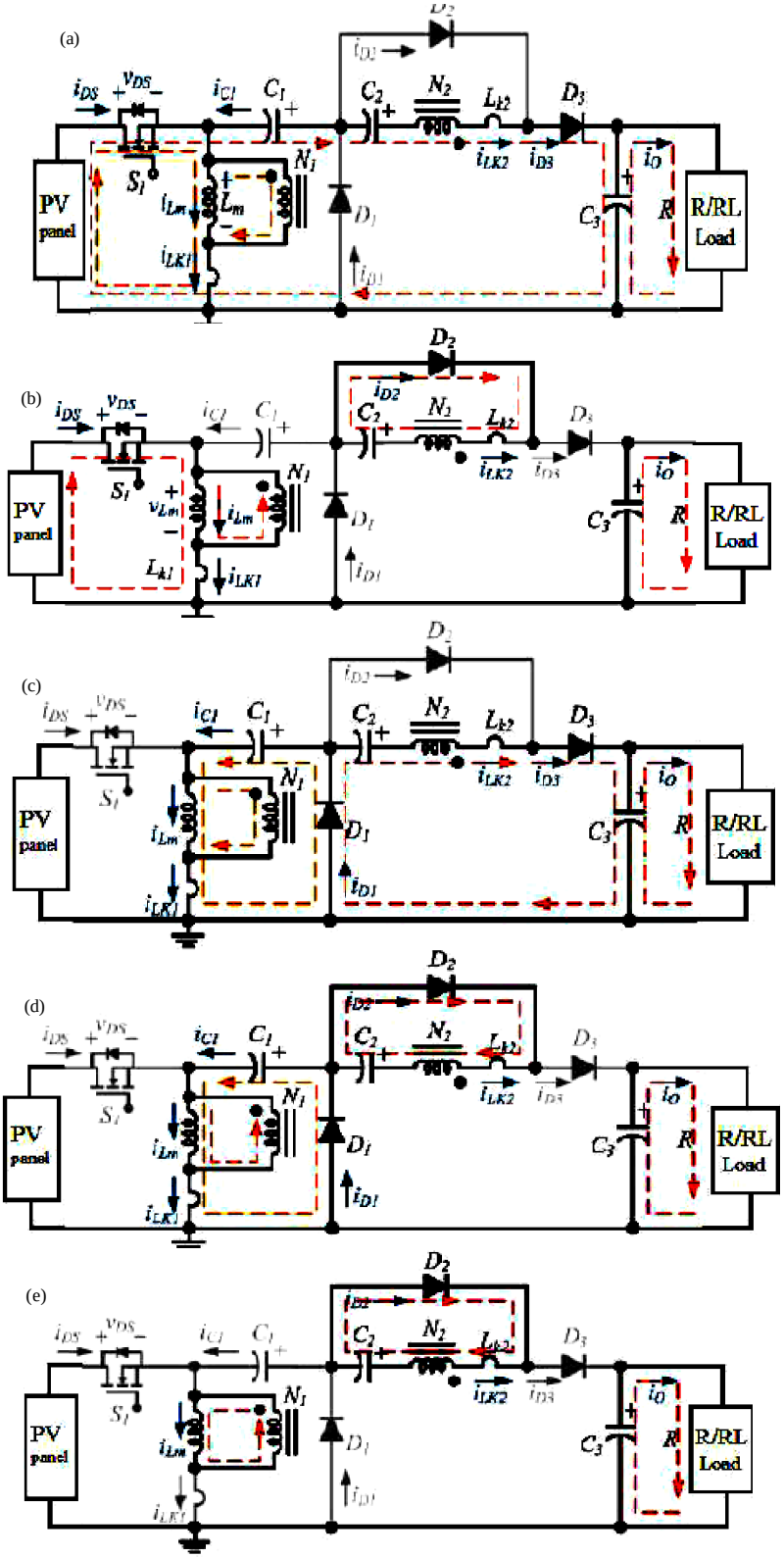

Fig. 6: During CCM operation, current flowing path in 5 modes operation: a) Mode 1; b) Mode 2; c) Mode 3; d) Mode 4 and e) Mode 5

is off. The present current way is appeared in Fig. 6 and the Diodes D_1 and D_3 are directing. The vitality put away in spillage inductor L_{k1} is coursing through Diode D_1 and the Capacitor C_1 is charged in a split second when S_1 off. Additionally, the L_{k2} keeps an indistinguishable current bearing from in the past mode. The auxiliary spillage inductor current i_{LK2} is being declined by $i_{Lm/n}$. Current i_{Lk1} when the expanding i_{Lk1} approaches the diminishing i_{Lm} this mode closes at $t = t_1$. Once when the current i_{Lk2} drops to zero, this mode ends at $t = t_3$:

$$\begin{aligned} i_{in}(t) &= i_{DS}(t) = i_{Lk1}(t) \\ \frac{di_{Lm}(t)}{dt} &= \frac{V_{Lm}}{Lm} \\ \frac{di_{Lk1}(t)}{dt} &= \frac{V_{in}-V_{Lm}}{L_{k1}} \\ i_{Lk2}(t) &= i_{Lm}(t)-i_{Lk1}(t) \end{aligned} \quad (15)$$

Mode 4 [t_3, t_4]: In this move interim, the vitality put away in charging inductor Lm is discharged all the while to C_1 and C_2. The present stream way is appeared in Fig. 6d what's more, the Diodes D_1 and D_2 are leading. As spillage vitality still courses through Diode D_1 and keeps on charging Capacitor C_1, currents i_{Lk1} and i_{D1} are relentlessly being diminished through T_1 and D_2, the L_m is conveying its vitality for charging Capacitor C_2. The vitality put away in Capacitors C_3 is released always to the heap R. The voltage crosswise over S_1 is the same as in the earlier mode. Current i_{D2} is expanding, yet, i_{Lk1} and i_{Lm} are diminishing, yet. This mode closes when current i_{Lk1} gets to be distinctly zero at $t = t_4$ (Singh *et al*., 2015; Chen *et al*., 2013; Vuthchhay and Bunlaksananusorn, 2008; Dhali *et al*., 2012; Wei and Batarseh, 1998).

RESULTS AND DISCUSSION

Conventional open loop Zeta converter with RL load: The significance of recreation is evident for the preparatory outline design of any system. System conduct and execution can be anticipated with the assistance of the reproduction. To confirm and examine the outline and execution of the preparatory stage, a re-enactment investigation of Zeta converter in open loop is perform med for info DC voltage of 15 V at 50 Hz and output DC Voltage of 8.5 V and 14 W output control rating with an exchanging recurrence of 10 kHz with RL load (Ramkumar, 2017).

Power circuit of Zeta converter with open loop is shown in Fig. 5. AC input voltage is shown in Fig. 6. Switching pulse and Vds for MOSFET is shown in Fig. 7. Output voltage and output current and output power are shown in Fig. 8-10, respectively, power factor for open loop Zeta converter is shown in Fig. 11. Total harmonic distortion is shown in Fig. 12 and 13. For conventional circuit THD value is very high (Sivakumar *et al*., 2017).

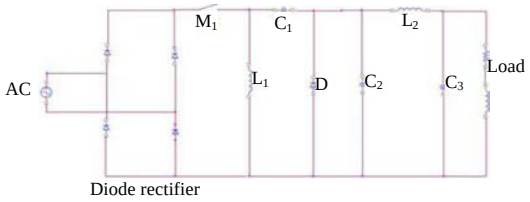

Fig. 7: Open loop Zeta converter

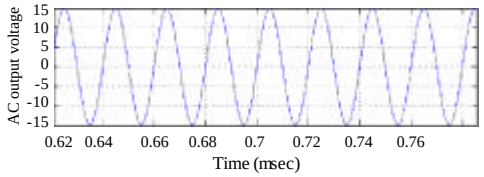

Fig. 8: AC input voltage

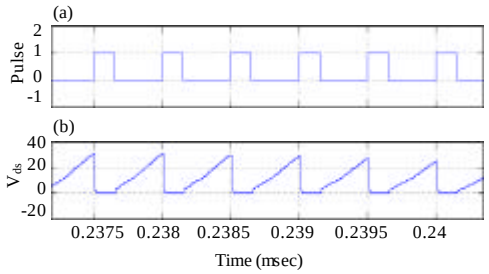

Fig. 9: Switching pulse and V_{ds} for M_1

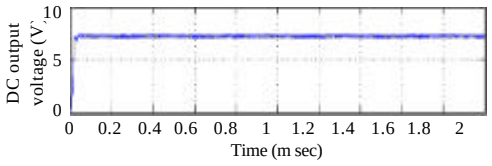

Fig. 10: Output voltage

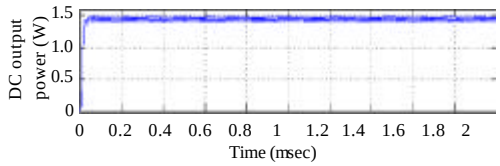

Fig. 11: Output power

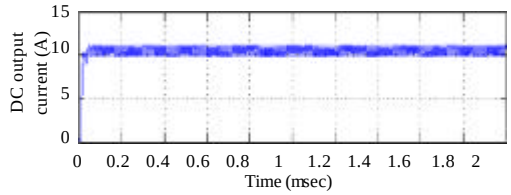

Fig. 12: Output current

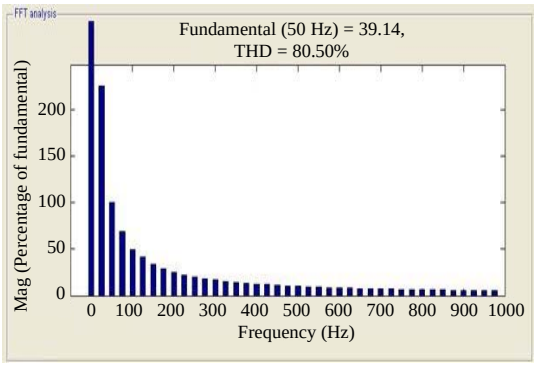

Fig. 13: FFT analysis for open loop Zeta converter

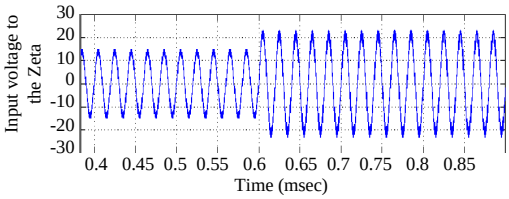

Fig. 14: Input voltage to the Zeta converter

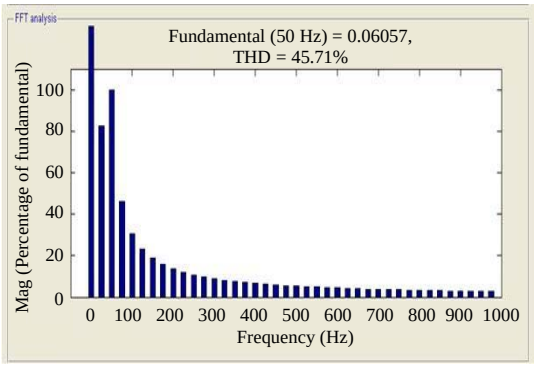

Fig. 15: FFT analysis for open loop Zeta converter with disturbance

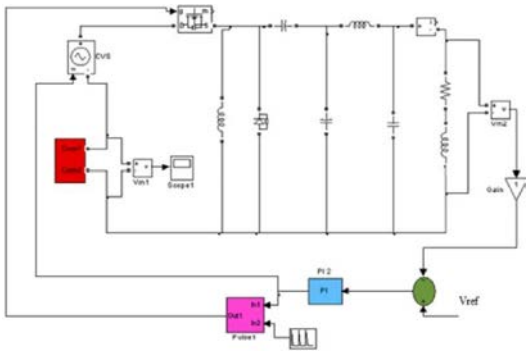

Fig. 16: Proposed closed loop Zeta converter with RL load

Conventional open loop Zeta converter with disturbance in the input side: In the circuit of conventional open loop

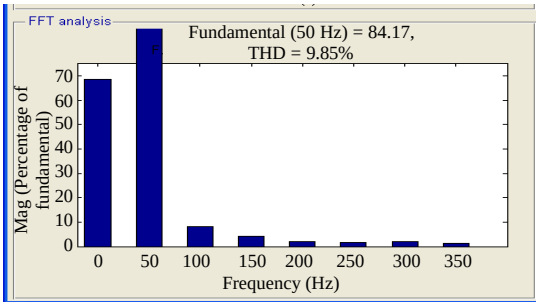

Fig 17: FFT analysis for closed loop Zeta converter

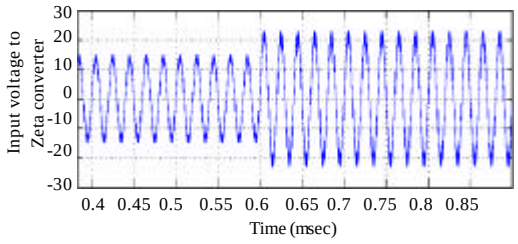

Fig. 18: Input voltages

Zeta converter, a step disturbance is given in the input side. Input voltage, output voltage, output current and output voltage of the circuit is shown in Fig. 14-17, respectively. Total harmonic distortion is shown in Fig. 18.

Proposed closed loop Zeta converter with RL load: The closed loop Zeta converter for PFC with RL load. It uses a very simple control feedback which only requires output voltage sensing (Subramanian *et al*., 2017).

At the input AC side a bridge rectifier is used for a PFC using an capacitor and inductor combination. A small value of V_o, compared to the reference value and resulting value, passes through the Proportional Integral (PI) controller generates the PWM output and which has been used for switching the MOSFET (M1). This kind of inherent PFC characteristics with constant duty ratio and switching frequency, offering an attractive solution for lower power applications (Erickson and Maksimovic, 2007).

The output voltage direction is given by the input circle as appeared in Fig. 19 where the output detected Voltage V_o is contrasted and a reference V_{ref} current and the blunder is enhanced in a corresponding essential (PI) controller which is contrasted and a saw-tooth slope V_s in this manner giving the beat to power switch. Subsequently, this circuit is controlled by the distinction in the on time interim and the steady exchanging recurrence f_s (Yuvaraj *et al*., 2017; Prabha *et al*., 2017).

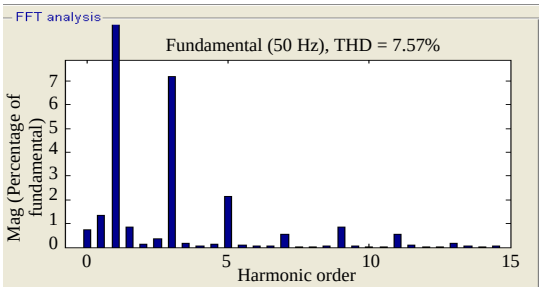

Fig. 19: FFT Analysis for closed loop Zeta converter with disturbance

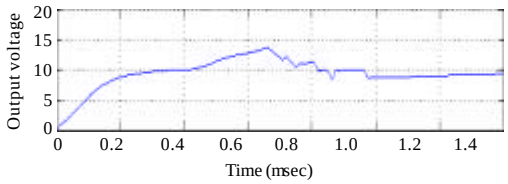

Fig. 20: Output current

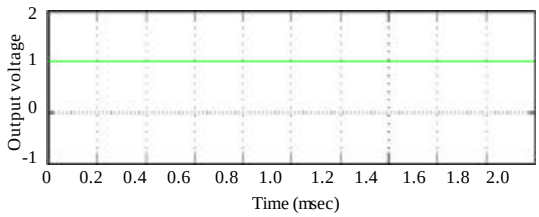

Fig. 21: Power factor proposed references ciruit

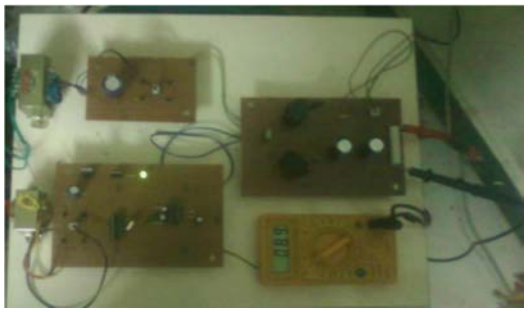

Fig. 22: Hardware setup

Input voltage, output voltage and output current are appeared in Fig. 20-22 individually. Control figure for closed loop circle Zeta converter is appeared in Fig. 22 (Tao *et al*., 2008)

Proposed closed loop Zeta converter with disturbance in the input side: In the circuit of closed loop Zeta converter, a step disturbance is given in the input side. Input voltage, output voltage and output current for the circuit is shown in Fig. 20-22. Total harmonic distortion is shown in Fig. 17 and 19 (Kochcha and Sujitjorn, 2010; Singh and Chaturvedi, 2008; Shaik and Babu, 2012; Martins *et al*., 1996; Tse, 2003; Singh *et al*., 2008; Martins and De Abreu, 1993; Garcia *et al*., 2003; Lascu *et al*., 2005; Anonymous, 2007; Singh *et al*., 2015; Chen *et al*., 2013; Vuthchhay and Bunlaksananusorn, 2008; Dhali *et al*., 2012; Wei and Batarseh, 1998).

Table 1: Closed loop Zeta converter

Input voltage	Output voltage	Output power	Efficiency (%)
12	4.30	3.80	92.0
13	7.60	11.40	93.1
14	8.10	13.13	94.0
15	8.45	14.29	94.5

Table 2: Open loop Zeta converter

Input voltage	Output voltage	Output power	Efficiency (%)
12	6.50	8.59	91.0
13	7.10	10.28	92.3
14	7.78	12.10	92.6
15	8.50	14.08	93.1

Experimental results: Hardware results are shown in the following section for proposed method and an experimental prototype model of the PWM Zeta converter has been constructed. The hardware setup with detailed specifications is shown in Fig. 23. IR2110 is used as the driver circuit. PIC16F84A is used as the processor. A Pi-filter is added to avoid control error caused by the switch noise.

Performance tabulation: Table 1 and 2 is discuss in the performance tabulation.

CONCULSION

The performance of Zeta converter is compared by comparing converter in both open loop and in closed loop. Zeta converter in closed loop has low THD value and power factor near to unity than open loop system. This study clarifies the pulse width regulated Zeta converter. In this study, design and simulation of Zeta converter in open loop and closed loop are taken for 9.2 V, 15 W output. Both the circuits are recreated with RL load. The closed loop Zeta converter has an efficiency of 96.5%. The THD of the closed loop Zeta converter is good comparing to open loop. The power factor level is very near to unity. The closed loop Zeta converter proposed circuit has low THD. It permits remedy of current working in discontinuous mode and in this way it is more sufficient for the application with high power gain. The efficiency of Zeta in open loop and closed loop is discussed in this study, respectively. Thus, Zeta converter in closed loop with ZVZCS gives better performance comparing it with to previous methods.

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