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Design and Simulation BPSK and QPSK Modulation Using VHDL

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Abstract: BPSK and QPSK are two techniques for modulation are simulated in this paper employing VHDL and Xilinx system software. Using VHDL to design the digital communications devices and implemented these devices on FPGAs without arranging new hardware. Besides, it can be support new protocols within seconds. Additionally, FPGAs provide a means for updating systems which are physically difficult to access, so, for those reasons FPGAs offer an ideal platform to implement adaptive communications algorithms. In this research, an approach is proposed digital modulator techniques which are comfortable for telemetry application and has significant features such as simplifying the hardware design and significant high data rate. In this research, a description is carried out for a method to implement the technique of modulation, BPSK and QPSK to transmit high data rate by using VHDL, Field Programmable Gate Array (FPGA) is selected to implement the mentioned technique. The proposed method is carried out successfully with VHDL language by using Xilinx ISE 10.2 design suite, SPARTAN-3FPGA also used to implement the previous technique.

Key words: BPSK, QPSK, FPGA, VHDL, digital modulator, communications algorithms

INTRODUCTION

Digital modulation is the process of converting the digital data bit to a waveform for transmission over noisy. Shift keying techniques for modulation means variation the carrier characteristics in accordance with information message signal. One of these techniques is Binary Phase Shift Keying (BPSK) which is common with wireless communication systems in addition, BPSK is simplest form of digital modulator in terms of structural and designing for both transmitter and receiver. The applications of BPSK modulation technique in general with wireless systems such as Wireless Personal Area Network (WPAN) due to its capability of reducing the BER (Park, 2005).

Due to its feature of normalized and smaller waveform of BPSK and very lesser amount of degraded by narrowband interference it's widely used with GPS services (Dedes and Dempster, 2005; Chaudhary *et al*., 2013).

These days, wireless communication system is an eminent platform in the field of communication due to the growing demand particularly in communication connectivity driven by wireless communication system and cellular applications.

An efficient transmission of information with wireless communication system is required with highly data rate. Several factors can be contributed to attain the mention aim one of these factors is the technique of modulation used with the system. With the same available bandwidth, modulation process can enhance the data rate transmission (Roddy, 2006). One of most common technique of modulation using now a days is Quadrature Phase Shift Keying (QPSK) it is created and developed from the basic one, PSK, modulation. QPSK is employing with satellite communication system, wireless Local Area Network (LAN), video conferencing and several systems of digital communication under Radio Frequency (RF) carrier (Kao, 2002; Misra, 2004).

Besides, the symbol can be transmitted with low rate by QPSK, rather than the other techniques of digital modulation such as QAM (Quadrature Amplitude Modulation) 64 and 32 with consuming lower power and low complexity of receiver circuit (John 2008; Stallings, 2007). The basic idea of QPSK modulation is the amplitude and frequency of the carrier unchanged just the phase is varying according to the input message signal and Q means there are four different of levels for representing the phases and each level corresponding two bits of input signal. These levels of representing the input signal illustrated with Table 1.

Field Programmable Gate Arrays (FPGA) is an important tool that to implement several logic circuits for different applications, so, proper understanding of logic circuit which the essential of electronic and computer circuits.

Table 1: The levels of representing input signals

No. of levels	Input state
0	00
1	01
2	10
3	11

In this research, FPGA is used to implement QPSK modulator which consume less power for transmission and get more efficient bandwidth transmission. The proposed technique employing the data that stored in the block of memory to produce the waveform according to the input message. Direct Digital Synthesizer (DDS) is used with the implementation of QPSK to generate sine wave which is representing the carrier needed for transmission the QPSK output. The proposed modulator successfully modeled with VHDL Hardware Description Language (HDL), simulated with Xilinx Integrated Software Environment (ISE) Software.

MATERIALS AND METHODS

The research in this study is made up of three major parts transmitter, receiver and channel modeling, respectively. Hardware Description Language (HDL) is used to implement the circuit of BPSK and QPSK system for baseband modulation system. Challenges are confronted with designing hardware, these challenges implies how to implement real and imaginary part with VHDL, perfect sine and cosine pass band circuit and how many clock cycle for each operation? Additionally, how operation can be completed in parallel with added operation? Still these challenges and details critically important while designing hardware is carried out. The system has been designed and implemented using VHDL and on Xilinx ISE WEB PACK.

The signal is transmitted over modeling channel which is modifies the transmitted signal to perform as transmitted over real wireless channel the signal is directly received by the second side (receiver).

Transmitter circuit: Figure 1 shows the block diagram of transmitter circuit which consists of two stages. First, the serial to parallel converter which used to convert the serial information bits to parallel, secondly, the BPSK or QPSK modulator which used to maps the output of serial to parallel converter into complex symbol.

These complex symbols are stream of modulated symbols and each stream are fed to the transmitter antenna.

Serial to parallel converter: One of the applications for shift register is a serial to parallel converter which is accept the input data as a serial and sends the output as a block of parallel data, the scheme of the used converter

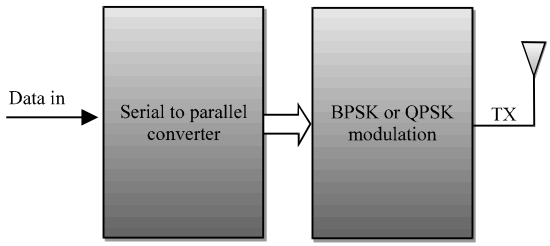

Fig. 1: Transmitter block diagram

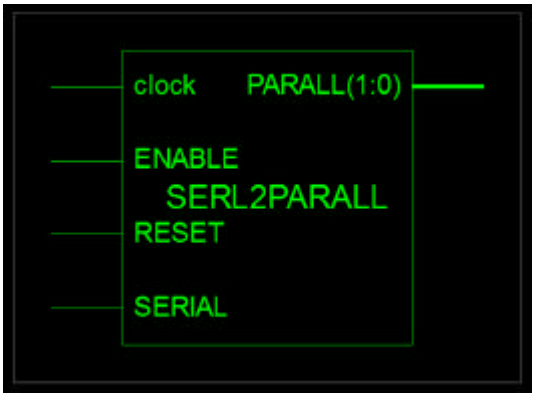

Fig. 2: A serial to parallel converter block diagram

Table 2: Pin description of each input/output port

Description	Signal	Direction	Size
Clock signal that clocks all internal serial to parallel engine component	CLOCK	Input	1
Reset signal that resets the serial to parallel when asserted	RESET	Input	1
Active-high enable input. When de-asserted, the serial to parallel is disabled	ENABLE	Input	1
Input data represented in binary bit stream	SERIAL	Input	1
Output data represented in parallel binary bit	PARALL	Output	2

with this research is shown with Fig. 2. The converter has 5 pins with function of these pins is, the first pin is the input for serial data, Enable input pin (ENABLE), Clock input (CLOCK), Reset input (RESET) and the Parallel data output (PARALLEL), respectively. With BPSK modulation, the output is (PARALLEL (1:0) while with QPSK is (PARALLEL (0:3).

VHDL code employed with designing the converter for serial to parallel was general, that's mean it easy to design and implement another types of serial to parallel converter such that converter with 0:15 lines. Table 2 explains the description for each input/output port and the time simulation for the serial to parallel converter is illustrated with Fig. 3.

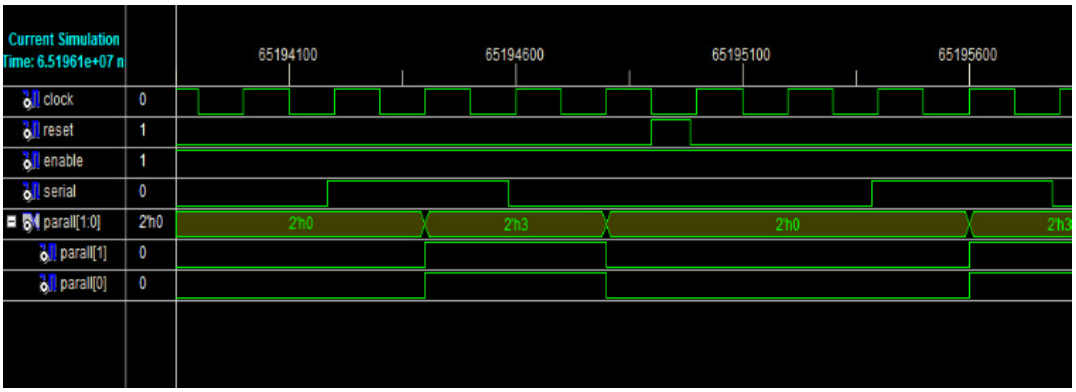

Fig. 3: The timing simulation for random value of a serial to parallel converter

RESULTS AND DISCUSSION

Modulation: The BPSK modulator circuit is a simple combinational logic which operates without any need for controller. The input to the BPSK is a single bit every clock cycle to produce a real and imaginary numbers each of 8 bit length. In this study, the constellation is represented by a real numbers -1 and +1 to represents logic 0 and 1, respectively. As such, the output becomes 10000000 and 01111111 when the input is 0 and 1, respectively. Which are corresponding to 128 and 127 unsigned decimal numbers.

Two BPSK circuits are connected in parallel to map the 2 bit output from the serial to parallel converter each BPSK process single bit every clock cycle.

In this study, a BPSK modulator is used in the proposed communication system and the required modification is also introduced in case of using a QPSK modulator instead. It is worth mention that, two QPSK circuits are used to map 4 bit serial to parallel output each one of them process 2 bit every clock cycle.

Figure 4 illustrates the BPSK modulator with a single bit input port (DATA) and two 8 bit output ports I and Q for real and imaginary parts, respectively. The timing simulation of the BPSK output (I and Q) is shown in Fig. 5 and the pin configuration is listed in Table 2.

The input group of bits is mapped into QPSK constellation by QPSK modulator which is the circuit of modulator is shown with Fig. 6. The modulator has one bit input data (DATA), 8 bits real part of complex number output (I) and eight bit imaginary part of complex number output (Q). Timing simulation of QPSK modulator is shown in Fig. 7 with random values, additionally the description of the circuit pins is illustrated with Table 3.

Demodulation of BPSK and QPSK: At the receiver which is the block diagram is shown with Fig. 8, we have designed the BPSK demodulator circuit which is shown in Fig. 9, the function of the demodulator is to get the original transmitted signal. The description of the pin circuit for BPSK and QPSK demodulation is illustrated with Table 4 and 5.

The same criteria that used with BPSK modulator at the transmitter is used in the BPSK demodulator. Demodulation input bit number will be altered compared with output of modulation as shown in Table 4. A (80) HEX will be converted as a 0 (1 bit) and a (7F) HEX will be a 1 (1 bit) as shown in Fig. 10.

Fig. 4: BPSK modulator circuit

Table 3: Pin description of each input/output port

Description	Signal	Direction	Size
Input data which represents binary bits	Data	Input	1 in BPSK
Output data which represents the real part of complex number in integers	I	Output	8
Output data which represents the imaginary part of complex number in integers	Q	Output	8

Table 4: Pin description of QPSK modulation circuit

Description	Signal	Direction	Size
Input data which represents binary bits	Data	Input	2 in QPSK
Output data which represents the real part of complex number in integers	I	Output	8
Output data which represents the imaginary part of complex number in integers	Q	Output	8

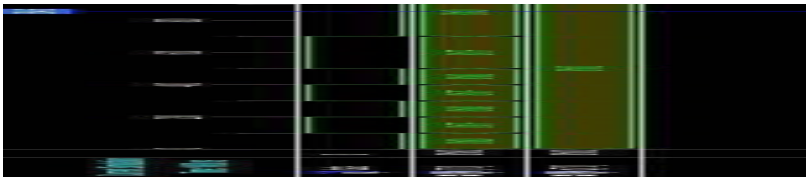

Fig. 5: Timing simulation of the BPSK modulator at random values

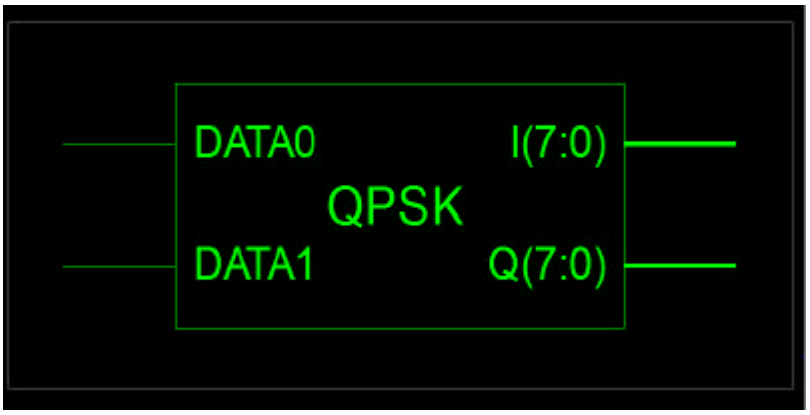

Fig. 6: QPSK modulation circuit

Fig. 7: Timing simulation of The QPSK modulator at random values

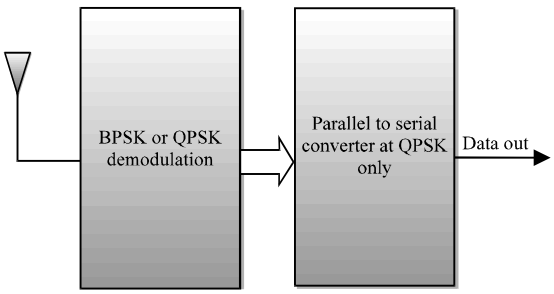

Fig. 8: Block diagram receiver

Fig. 9: BPSK demodulator circuit

The QPSK demodulator circuit is shown in Fig. 11 which demodulates the received signal to produce the transmitted binary bit stream, the output wave form of demodulation circuit is shown in Fig. 12.

Table 5: Pin description of QPSK and BPSK demodulation circuit

Description	Signal	Direction	Size
Output data which represents binary bits	Output	Output	In BPSK In QPSK
Input data which represents the real part of complex number	I	Input	8
Input data which represents the imaginary part of complex number	Q	Input	8

Parallel-to-serial: A parallel-to-serial converter is a typical application of shift registers. It consists of sending out a block of data serially. The parallel-to-serial converter circuit presented in Fig. 13.

The parallel-to-serial converter consist of two inputs signal, each one is 1-bit and one output signal as shown in Table 6.

Figure 14 shows the output waveform of parallel-to-serial converter. The effect of hazard state appears because two parallel signal will be appeared at one clock cycle instead of two state, so, it reduces required time to half.

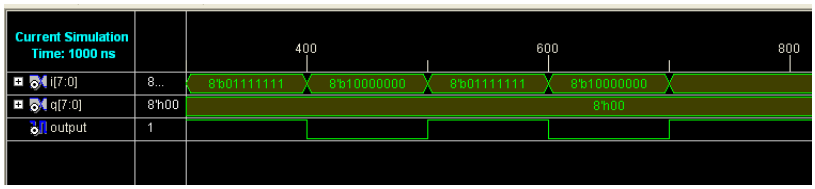

Fig. 10: Timing simulation of the BPSK demodulator at random values

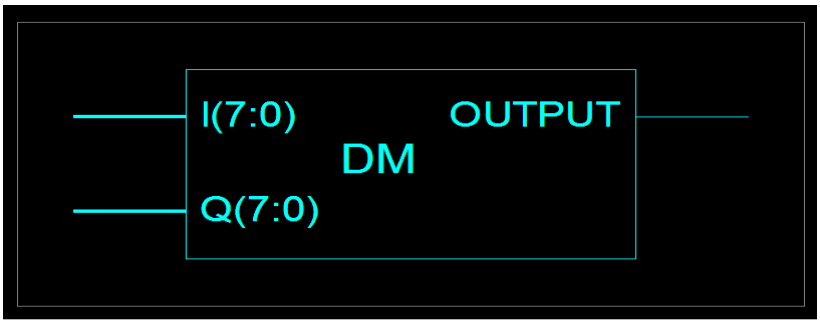

Fig. 11: QPSK demodulator circuit

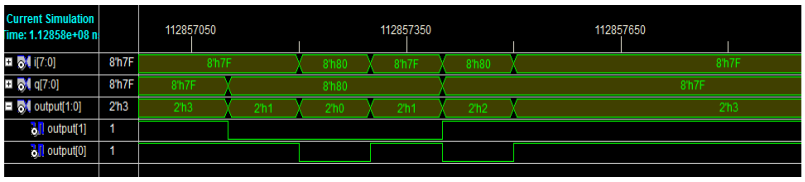

Fig. 12: Timing simulation of the QPSK demodulator at random values

Fig. 13: Parallel to serial circuit

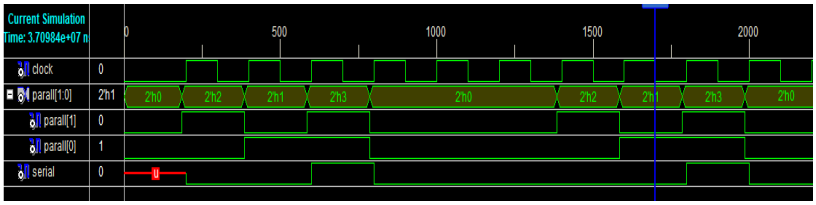

Fig. 14: Output waveform of parallel-to-serial converter

Table 6: Pin description of parallel-to-serial convert

Description	Signal	Direction	Size
Clock signal that clocks all internal serial to parallel engine component	Clock	Input	1
Input data represented in binary bit stream	A	Input	2 in QPSK
Input data represented in binary bit stream	B	Input	2 in QPSK
Output data represented in serial binary bit stream	Y	Output	1

CONCLUSION

Digital modulators circuit (BPSK and QPSK Models) have been design and implementation successfully with VHDL code using ISE 10.2 Software. A proposed research is a better performance with high data rate. The output of the circuit produced a BPSK or QPSK digital (square) signal waveform with the data rate with very low area requirement. Proposed technique simplifies the modulator to synthesize with FPGA or CPLD technologies and useful for various applications. Synthesis report shows that our proposed design consumes lesser area while providing high data rates. Some other techniques of modulation can further be implemented through our proposed technique.

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