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Fault Diagnosis in an Analog Circuit with Feedback

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Abstract: This study illustrates a method of fault diagnosis of analog circuits with feedback. In this study an efficient single catastrophic fault detection and identification approach for analog circuits is described using hierarchal testability procedure. The Simulation Before Test (SBT) method of fault diagnosis is used. The Circuit Under Test (CUT) is excited and output parameters are observed. The fault dictionary is developed for the CUT. Based on the deviation of the present response from fault free, fault detection and identification is done. The presented testing approach is applied on an analog benchmark circuit to the testing approach.

Key words: Catastrophic fault, fault diagnosis, Circuit Under Test (CUT), Simulation Before Test (SBT), fault dictionary, parameters

INTRODUCTION

The rapid growth in the present technology is leading to complex circuits in a single integrated circuit. There are different fault diagnosis methods for digital circuits. But fault diagnosis of analog circuits is more intricate when compared to digital circuits. There are two faults that occur in an analog system: hard faults and soft faults. Hard faults are also called as catastrophic faults and soft faults are called as parametric faults. The short circuit or open circuit of circuit components like resistors, capacitors, etc. is defined as hard fault or catastrophic fault. A catastrophic fault makes a component value to an unacceptable value. Whereas when the component value changes with respect to time, the fault is considered as soft fault or parametric fault.

There are numerous methods that have been proposed for fault diagnosis of analog circuits. Simulation After Test (SAT) and Simulation Before Test (SBT) are the two methods used for fault diagnosis (Bandler and Salama, 1985; Yuan *et al*., 2010). In simulation before test method the circuit simulations are done before testing. In SBT method, the response of the circuit with predefined input is compared with faulty response. The results of the simulations are stored in sequence and the entire stored pattern of simulation for all the cases is called as fault dictionary (Aminian and Aminian, 2001). The construction of the fault dictionary is a fundamental topic in the SBT (Slamani *et al*., 1994; Prasad and Babu, 2000). The approach proposed in this study allows us to detect and identify single catastrophic fault. For this purpose a fault dictionary is constructed. The proposed approach is described in detail for single catastrophic faults.

MATERIALS AND METHODS

Fault dictionary: A system is said to be faulty if the response of the system "Maps out" with the expected response. The fault diagnosis of analog system should detect the fault and identify the defective component which is the cause of the fault. Simulation before test method with fault dictionary can be used in fault diagnosis stage to detect a faulty component. Fault dictionary is constructed for a fault free system. The model of a fault dictionary is shown in Fig. 1. The left side column of the dictionary lists the faults and the top column has the parameters considered which help in detecting and identifying a fault. Each cell is filled with the value obtained for the respective, component analysis being done.

In this study, we build a fault dictionary pertaining to a single catastrophic fault among "N" possible faults. If there are 'n' components, there exist "2n" possible faults considering short circuit and open circuit of each component. Thus the fault dictionary has N patterns referring to faulty component and one pattern referring to fault free circuit, totally (N+1) patterns (Table 1). To generate the fault dictionary, few test nodes are identified and the respective parameters which help in fault detection and identification at each test node are noted.

Table 1: Model of a fault dictionary

Analysis for	Parameter 1	Parameter 2	Parameter 3	Parameter 4
Fault free	Value 1F	Value 2F	Value 3F	Value 4F
Component 1	Value 11	Value 12	Value 13	Value 14
Component 2	Value 21	Value 22	Value 23	Value 24
Component 3	Value 31	Value 32	Value 33	Value 34
Component 4	Value 41	Value 42	Value 43	Value 44

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Table 2: Components used in benchmark circuit

Name of the component	Quantity
Op-Amp	3
Resistors (R1-R15)	15
Capacitors (C1-C7)	7

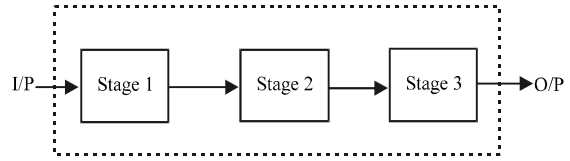

Fig. 1: An analog system with sub blocks without feedback

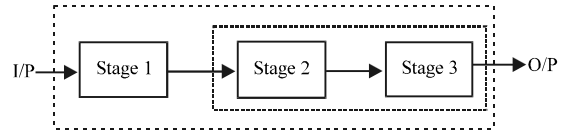

Fig. 2: An analog system with sub blocks having feedback

Analog benchmark circuit: Any system designed is expected to have a fault free response. The response obtained should meet the requirements for which the design has been proposed. An entire system can be bifurcated into blocks or stages. The whole design performance depends on individual blocks or stages performance. There can be two possible ways in which the sub blocks are linked with each other.

In the first category if there are 'n' sub blocks and are connected linearly, i.e., (n-1) sub block output will be connected to "nth" sub block and no component will be common to any of the sub block. Figure 1 shows an analog system with three stages connected linearly, i.e., output of stage 1 is connected to stage 2; output of stage 2 is connected to stage 3. This type of system can be considered as a system without any interconnections among sub blocks, i.e., without any feedback.

In the second category if there are "n" sub blocks which are connected in such a way that there can be interconnections between the sub blocks and there may be few components that will be common to any of the sub block. Figure 2 shows an analog system with three stages and stage 2 and 3 are interconnected, i.e., stage 3 fault can also influence stage 2 output. This type of system can be considered as a system with interconnections among sub blocks, i.e., with feedback.

The benchmark circuit considered is the elliptical filter. The Elliptical filter is one among the new proposed benchmark circuit along with ITC'97 benchmark circuits (Kondagunturi *et al*., 1999). The following are the components used in this benchmark circuit (Table 2).

In this study, single catastrophic fault detection and identification is analyzed for the elliptical filter. In this analysis, the assumption is the active element (op-amp) used in the design of benchmark circuit is fault free. The total number of hard faults that exist are: 2*(Total number of components) = 2*22 = 44.

Figure 3 shows an elliptical filter considered from analog benchmark circuits. In this circuit, the response parameters considered are measured at each op-amp. At each op-amp the measured response is termed as respective stage output. The simulated results of above design at each stage are give as Fig. 4 is the fault free response of elliptical filter. For V_{in} = 1V.

Stage 3:

- V_{out}: 62.925 mV
- -6 dB: 1.27 kHz
- -20 dB: 116.505 kHz

Stage 2:

- V_{out}: 55.4387 mV
- -6 dB: 1.61 kHz
- -20 dB: 160.136 kHz

Stage 1:

- V_{out}: 106.803 mV
- -6 dB: 0.8787 kHz
- -20 dB: 1.839 kHz

Effect of catastrophic faults in an elliptical filter: The elliptical filter which is designed with operational amplifiers and passive components can be bifurcated into three stages. In this study the catastrophic fault analysis (due to resistors and capacitors) on each stage is analyzed. The assumptions made in this analysis are:

- Only a single catastrophic fault is considered in the entire circuit
- All the active components used are fault free

The fault dictionary for the above design has been developed. For each fault every parameter is compared with its respective fault free value and the deviation is calculated. The algorithm for the detection and identification of the fault is based on the deviation with respect to fault free value.

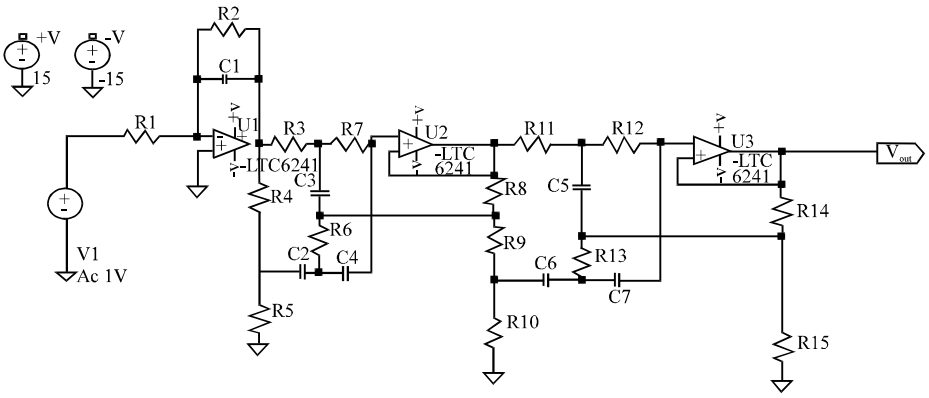

Fig. 3: Elliptical filter

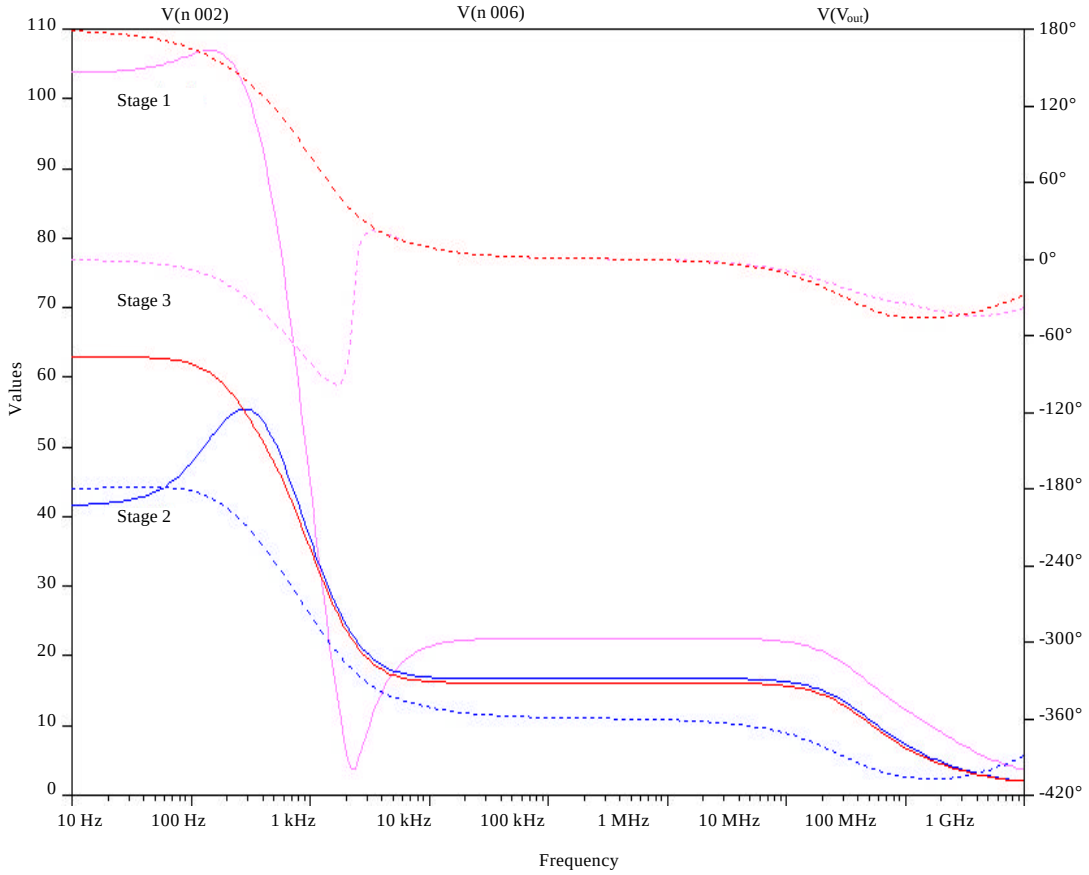

Fig. 4: Fault free frequency response (magnitude (solid line) and phase (dotted line) response curve of each stage, indicated with three different colors)

Any parameter with an increase or decrease of 1.5% is considered as acceptable range. The methodology used to detect and identify a single catastrophic fault in this circuit consisting of feedback is as follows (Fig. 5-10).

The stage1 is excited with an AC input of 1 V. Stage 1 is followed by stage 2 and 3. The parameters which were considered are measured at stage 3 are compared with fault free. If the deviations are within the acceptable range, it can be concluded that the design is fault free. If the deviations are unacceptable, it implies that there is an error. If the deviations are found to be unacceptable then measure the parameters at stage 2. If stage 2 parameters are found to

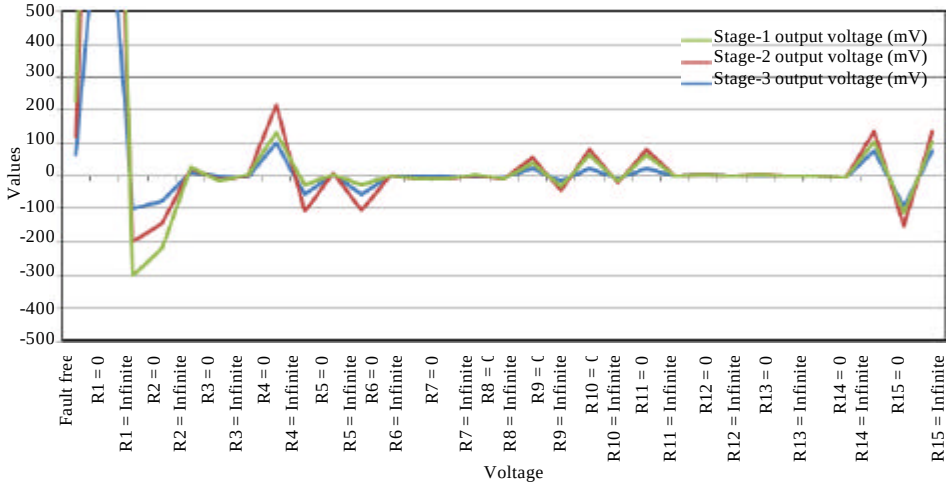

Fig. 5: Catastrophic fault effect on voltage at each stage due to resistor

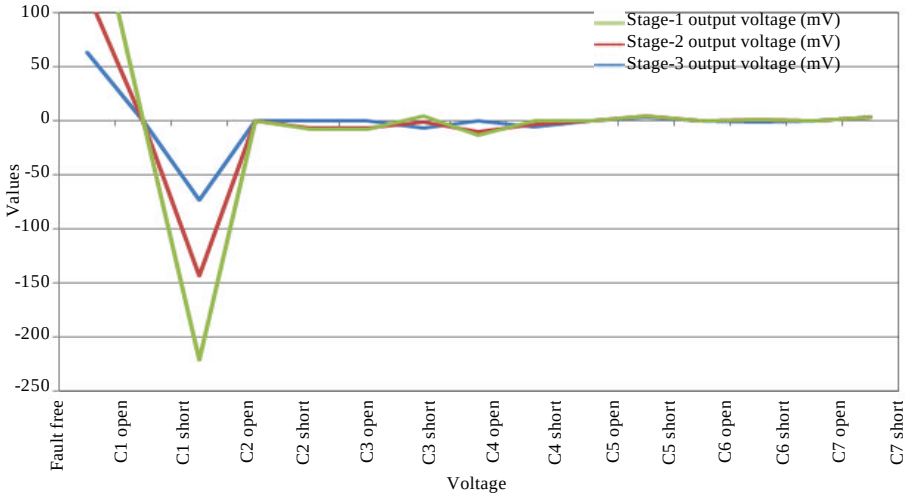

Fig. 6: Catastrophic fault effect on voltage at each stage due to capacitor

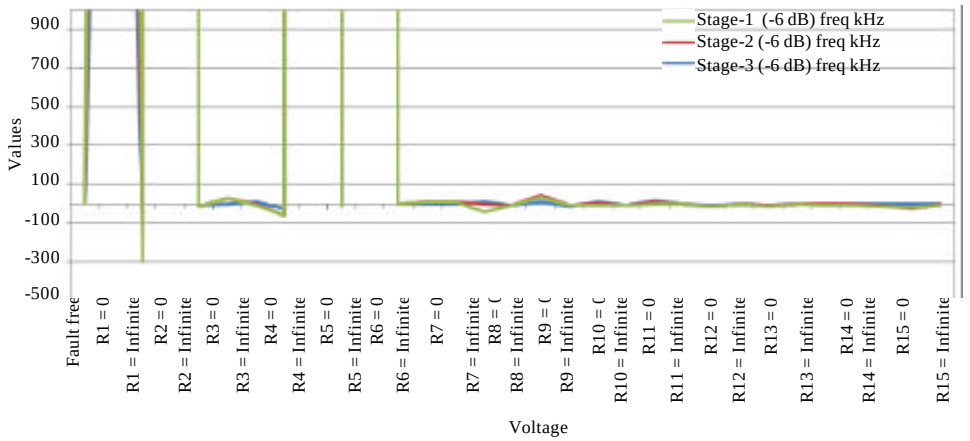

Fig. 7: Catastrophic fault effect on -6 dB frequency at each stage due to resistor

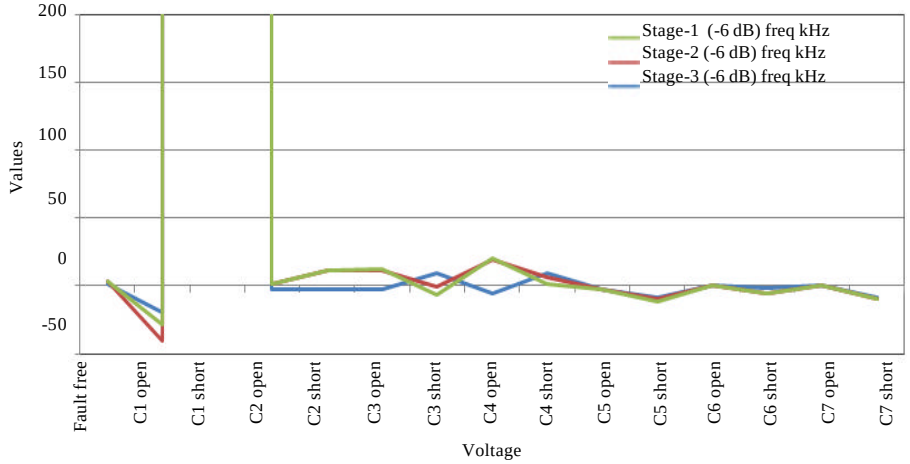

Fig. 8: Catastrophic fault effect on -6 dB frequency at each stage due to capacitor

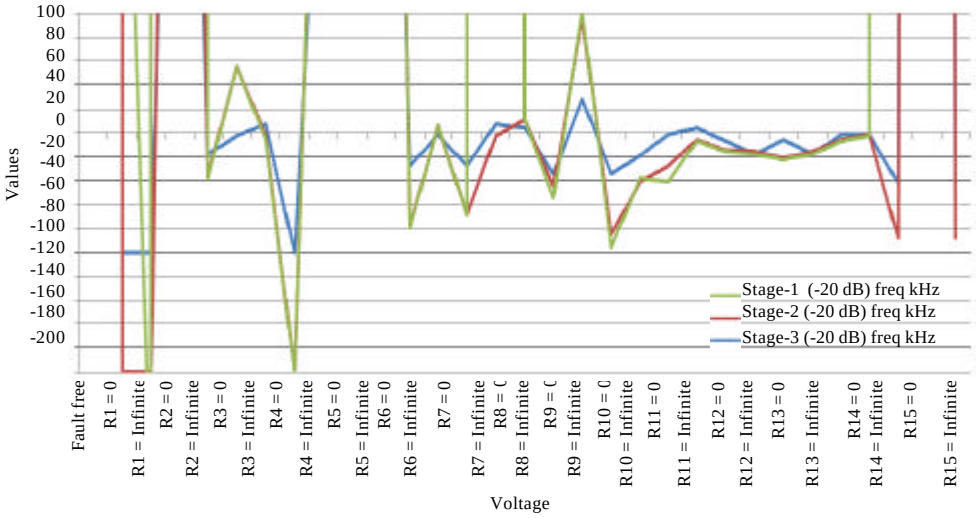

Fig. 9: Catastrophic fault effect on -20 dB frequency at each stage due to resistor

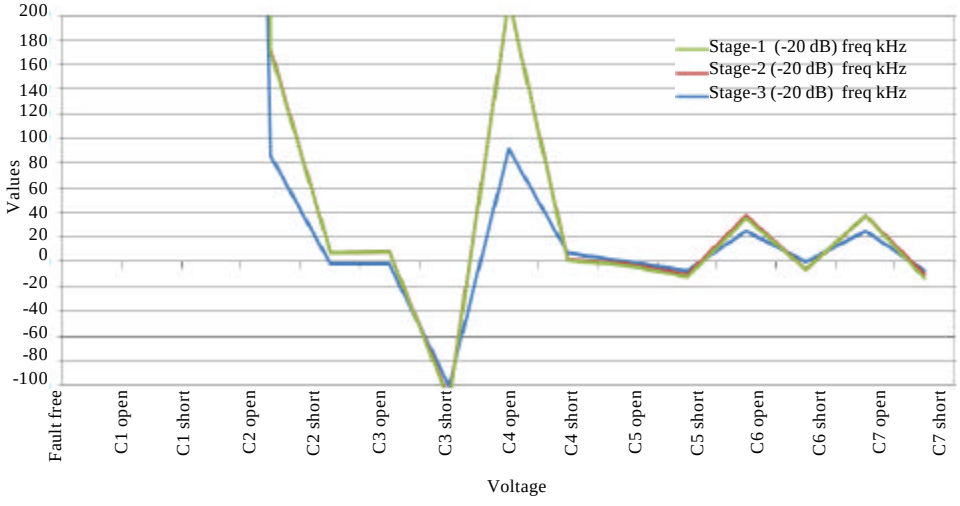

Fig. 10: Catastrophic fault effect on -20dB frequency at each stage due to capacitor

Table 3: Effect of catastrophic fault of each resistor on voltage observed at each stage (Deviated values are in terms of % increment or decrement compared with fault free)

Analysis for	Stage 3 output (mV)	Stage 2 output (mV)	Stage 1 output (mV)
R1 short	↑>100	↑>100	↑>100
R1 open	↓100	↓100	↓100
R2 short	↓73	↓69	↓76
R2 open	↑11	↑11	↑6
R3 short	NC	↓12	↓2
R3 open	↓5	↑5	↑5
R4 short	↑>100	↑>100	↓85
R4 open	↓56	↓48	↑75
R5 short	↑3	↑3	↓2
R5 open	↓55	↓47	↑76
R6 short	NC	↑1.7	NC
R6 open	NC	↓6	↓1.8
R7 short	NC	↓5	NC
R7 open	↓5	↑5	↑5
R8 short	↓3	↓5	↑3
R8 open	↑25	↑31	↓16
R9 short	↓13	↓28	↑9
R9 open	↑26	↑54	↓16
R10 short	↓5	↓12	↑4
R10 open	↑25	↑54	↓16
R11 short	NC	NC	NC
R11 open	↑2	↑3	NC
R12 short	NC	NC	NC
R12 open	↑2	↑3	NC
R13 short	NC	NC	NC
R13 open	NC	NC	NC
R14 short	↓2	↓1.51	NC
R14 open	↑76	↑59	↓33
R15 short	↓91	↓60	↑39
R15 open	↑77	↑59	↓33

Table 4: Effect of catastrophic fault of each capacitor on voltage observed at each stage (The deviated values are mentioned in terms % increment or decrement compared with fault free)

Analysis for	Stage 3 output (mV)	Stage 2 output (mV)	Stage 1 output (mv)
C1 open	NC	NC	NC
C1 short	↓73	↓69	↓78
C2 open	NC	NC	NC
C2 short	NC	↓6	NC
C3 open	NC	↓6	NC
C3 short	↓6	↑5	↑4
C4 open	NC	↓10	↓2
C4 short	↓5	↑1.87	↑3
C5 open	NC	NC	NC
C5 short	↑3	NC	NC
C6 open	NC	NC	NC
C6 short	NC	↑1.97	NC
C7 open	NC	NC	NC
C7 short	↑2	NC	NC

*NC→No change

Table 5: Effect of catastrophic fault of each resistor on -6 dB frequency observed at each stage (The deviated values are mentioned in terms % increment or decrement compared with fault free)

Analysis for	Stage 3 (-6 dB) freq (kHz)	Stage 2 (-6 dB) freq (kHz)	Stage 1 (-6 dB) freq (kHz)
R1 short	↑>100	↑>100	↑>100
R1 open	↓100.00	↓100.00	↓100.00
R2 short	↑>100	↑>100	↑>100
R2 open	↓5.70	↓5.73	NC
R3 short	NC	↑28	NC
R3 open	↑9	↓9.94	↓5.74
R4 short	↓23	↓34	↓2
R4 open	↑>100	↑>100	NC
R5 short	↓5	↓4	NC
R5 open	↑>100	↑>100	NC
R6 short	NC	↓2	NC
R6 open	↓2	↑13	NC
R7 short	↓2	↑13	NC
R7 open	↑9	↓11	↓43
R8 short	↓5	↓4	NC
R8 open	↑10	↑32	↓11
R9 short	↓13	↑4	↑3
R9 open	↑10	↓5	↓12
R10 short	↓9	NC	NC
R10 open	↑14	↓7	↓9
R11 short	↓2	NC	NC
R11 open	↓9	↓2	NC
R12 short	NC	NC	NC
R12 open	↓8	↓2	NC
R13 short	NC	NC	NC
R13 open	↓2	NC	NC
R14 short	↓4	NC	NC
R14 open	NC	↓4	↓9
R15 short	↓4	↓20	↑6
R15 open	NC	NC	↑8

Table 6: Effect of catastrophic fault of each capacitor on-6dB frequency observed at each stage (The deviated values are mentioned in terms % increment or decrement compared with fault free)

Analysis for	Stage3 (-6 db) freq (kHz)	Stage2 (-6 db) freq (kHz)	Stage1 (-6 db) freq (kHz)
C1 open	↓19	↓21	↑12
C1 short	↑>100	↑>100	↑>100
C2 open	↓2	↑4	NC
C2 short	↓2	↑14	NC
C3 open	↓2	↑14	NC
C3 short	↑9	↓9	↓5
C4 open	↓5	24	NC
C4 short	9	↓3	↓4
C5 open	↓2	NC	NC
C5 short	↓8	NC	NC
C6 open	NC	NC	NC
C6 short	NC	↓4	NC
C7 open	NC	NC	NC
C7 short	↓8	NC	NC

*NC→No change

be in acceptable range, it implies that the error could be a component in stage 3 and which is not common with stage 2. If the stage 2 parameters are found to be unacceptable, then it indicates that the fault is with a component which is common with stage 2 and 3. In this case, stage 2 and stage 3 is together considered as single block. Based on the deviation and the parameter considered the fault varies. The same procedure is continued for the entire procedure and all the faults are detected and identified. If a component is common to two stages then the two stages are considered to be a single stage (Table 3-8).

Table 7: Effect of catastrophic fault of each resistor on -20dB frequency observed at each stage (The deviated values are mentioned in terms of % increment or decrement compared with fault free)

Analysis for	Stage 3 (-20 dB) freq (kHz)	Stage 2 (-20 dB) freq (kHz)	Stage 1(-20 Db) freq (kHz)
R1 short	↓99	↓99	↑>100
R1 open	↓100	↓100	↓100
R2 short	↑>100	↑>100	↑>100
R2 open	↓17	↓18	↓3
R3 short	↓3	↑58	NC
R3 open	↑7	↑10	↓3
R4 short	↓99	↓99	NC
R4 open	↑>100	↑>100	↓1.57
R5 short	↑>100	↓17	NC
R5 open	↑>100	↑>100	NC
R6 short	↓27	↓50	NC
R6 open	NC	↑8	NC
R7 short	↓27	↓40	NC
R7 open	7↑	↓10	↑>100
R8 short	↑4	↑6	NC
R8 open	↓34	↓9	↓10
R9 short	↑28	↑67	↑6
R9 open	↓34	↓50	↓11
R10 short	↓18	↓22	↓3
R10 open	NC	↓26	↓12
R11 short	↓4.5	↓9	NC
R11 open	↓7	↓7	NC
R12 short	↓17	NC	NC
R12 open	↓5	↓14	NC
R13 short	↓17	NC	NC
R13 open	NC	↓4	NC
R14 short	NC	NC	NC
R14 open	↓42	↓46	↑>100
R15 short	↑>100	↑>100	↑ 24
R15 open	↓42	↓45	↑>100

Table 8: Effect of catastrophic fault of each capacitor on -20 dB frequency observed at each stage (Deviated values are mentioned in terms of % increment or decrement compared with fault free)

Analysis for	Stage 3 (-20 dB) freq (kHz)	Stage 2 (-20 dB) freq (kHz)	Stage 1 (-20 dB) freq (kHz)
C1 open	↑>100	↑9	↑68
C1 short	↑>100	↑>100	↑>100
C2 open	↑85	↑85	NC
C2 short	NC	↑9	NC
C3 open	NC	↑9	NC
C3 short	↓99	↓10	NC
C4 open	↑91	↑>100	NC
C4 short	↑7	↓5	NC
C5 open	NC	NC	NC
C5 short	↑7	↓3	NC
C6 open	↑24	↑12	NC
C6 short	NC	↓5	NC
C7 open	↑24	↑12	NC
C7 short	↓7	↓3	↓3

*NC➔No change

RESULTS AND DISCUSSION

Consider the component R2. If R2 is shorted as it is in stage 1, the response of stage 1 gets deviated as compared with fault free. The stage 1 fault is propagated till the last stage and hence, the responses of all the three stages are deviated from fault free. Figure 11 shows the effect on voltage of each stage when R^2 is shorted. Similarly, consider R8, placed after stage 2. It is interconnected to all the three stages. When this resistor is open it affects all the three stages.

Figure 12 shows the effect on voltage of each stage when R8 is open. Consider C3, it is not interconnected to stage 1, hence, when this capacitor is open it is not affecting stage1 response whereas stage 2 and 3 responses get deviated. Figure 13 shows the effect on voltage of each December 17, 2018 stage when C3 is open. Figure 14 shows the identified single catastrophic faults.

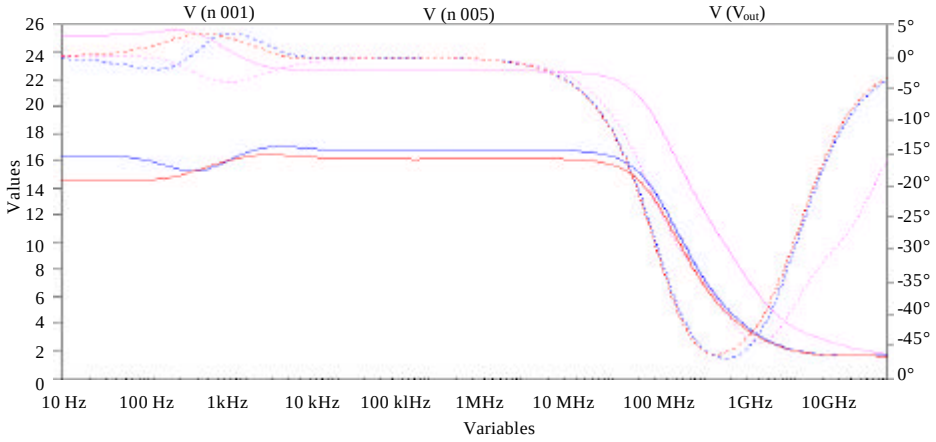

Fig. 11: Effect of R2 short on each stage

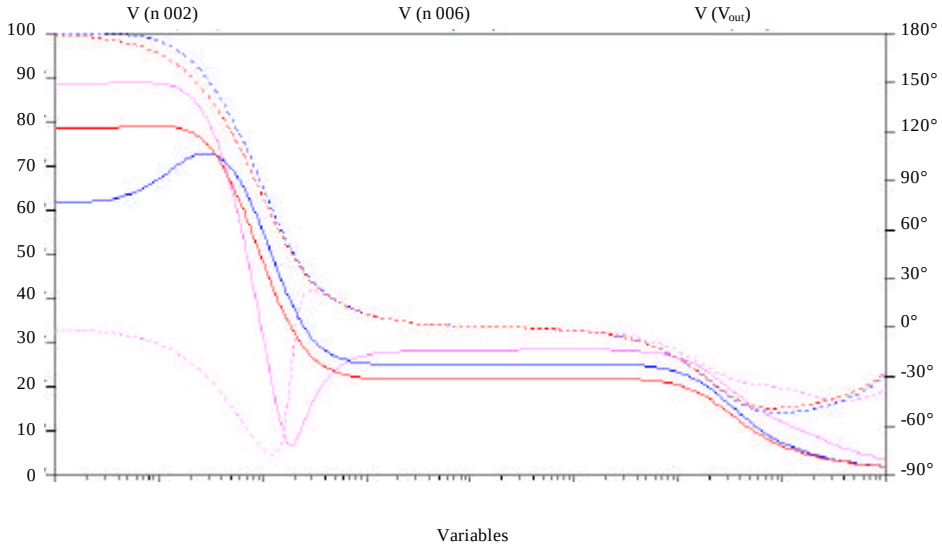

Fig. 12: Effect of R8 open on each stage

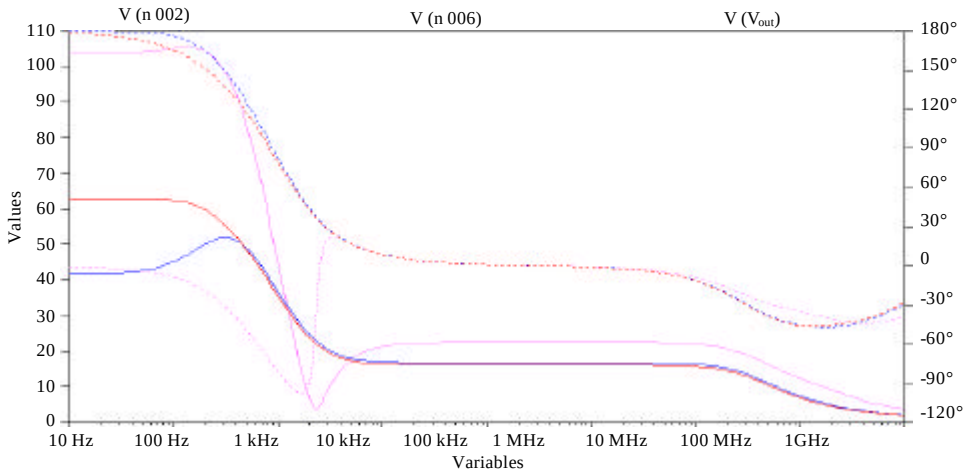

Fig. 13: Effect of C3 open on each stage

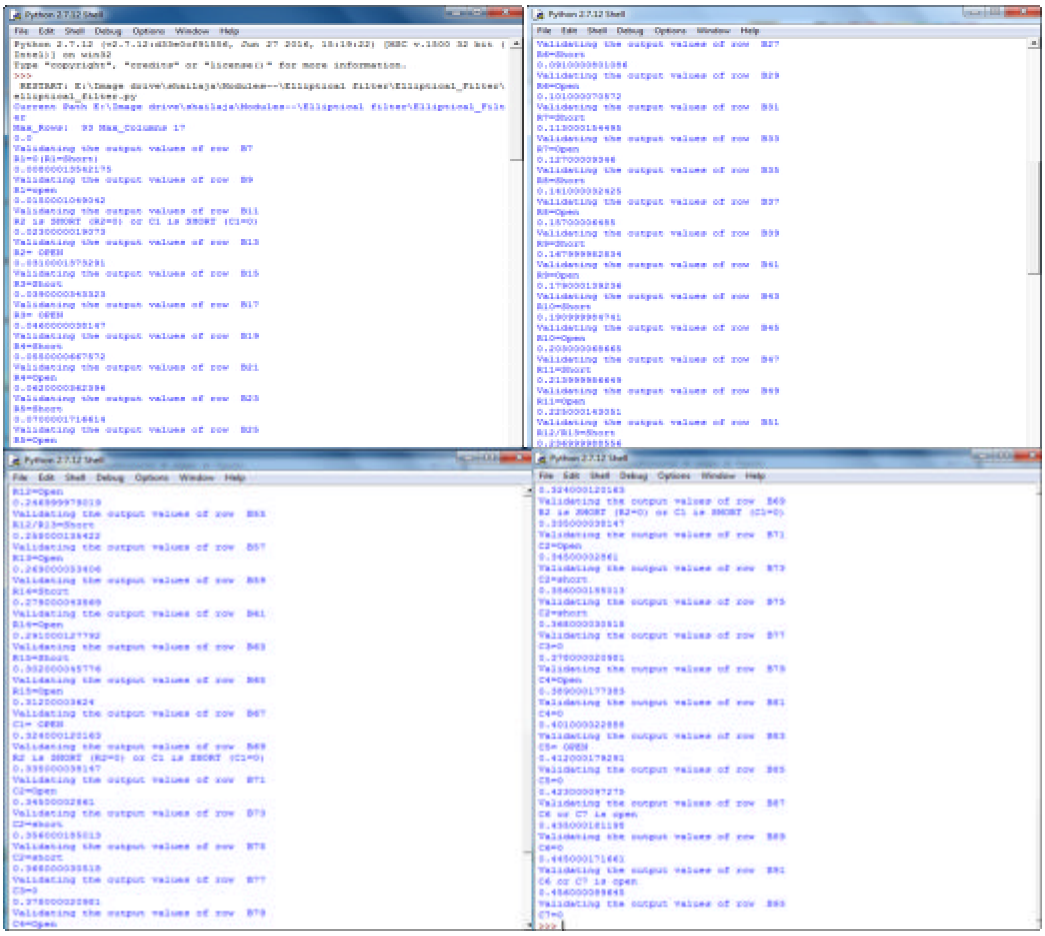

Fig. 14: Identified single catastrophic faults

CONCLUSION

In this study, a methodology has been proposed for catastrophic fault identification in an analog system with feedback. For this, a benchmark analog circuit has been considered and designed. The fault dictionary has been developed for the circuit considered. All the catastrophic faults have been diagnosed.

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