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Energy Storage Management Control for Nine-Level Inverter based on Super-Capacitors

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Abstract: In this study, modified multilevel inverters based on Newton Raphson (NR) and Particle Swarm Optimization (PSO) techniques were presented. A NR and PSO techniques were presented for Selective Harmonics Elimination (SHE) solution in a modified Cascaded H Bridge Multilevel Inverter (CHB-MLI). The Selective Harmonic Elimination Pulse-Width Modulation (SHE-PWM) is a powerful technique for harmonic minimization in multilevel inverter. The proposed design was used to charge the energy storage such as battery, super capacitor. NR and PSO techniques were used to determine the switching angles by solving the non-linear equation's analysis of the output voltage waveform of the modified CHB-MLI in order to control the fundamental component. The proposed techniques based on NR and PSO techniques are capable to minimize the Total Harmonic Distortion (THD) of output voltage of the modified CHB-MLI within allowable limits. A comparison has been made between NR and PSO techniques related to optimization in order minimize harmonic distortion. The main aims of this study cover design, modeling, construction and testing of a laboratory the modified topology of the CHB-MLI for a single-phase prototype for nine levels. The experimental results of the prototype were also, illustrated. The controllers based on NR and PSO were applied to the modified multilevel inverter. The Digital Signal Processing (DSP) TMS320F2812 is used to implement these modified inverters control schemes using NR and PSO method. The proposed controller was then coded into a DSP TMS320F2812 board. The inverter offers much less THD using PSO scheme compared with the NR scheme.

Key words: Harmonics, PSO, modified multilevel inverters, Digital Signal Processor (DSP), nine level, NR scheme

INTRODUCTION

Multilevel power conversion was first introduced 25 years ago (Babaei *et al*., 2013; Rashid, 2004; Rasheed *et al*., 2016; Jones and Satiawan, 2013). The general concept involves utilising a higher number of active semiconductor switches to perform the power conversion in small voltage steps. There are several advantages to this approach when compared with traditional two-level power conversion. The smaller voltage steps lead to the production of higher power quality waveforms and also, reduce the dv/dt stresses on the load and the electromagnetic compatibility concerns. Another important feature of multilevel converters is that the semiconductors are wired in a series-type connection which allows operation at higher voltages. However, the series connection is typically made with clamping diodes which eliminate over voltage concerns. Furthermore, since, the switches are not truly series connected, their switching can be staggered which reduces the switching frequency and thus, the switching losses. In order to lower harmonic content to improve the output waveform for voltage inverter, reduce the size of the filter utilized and the level of Electromagnetic Interference (EMI). Numerous topologies to realize this connectivity which can be generally divided into three major categories, namely, diode clamped MLI, flying capacitor MLI and separated DC sources cascaded H-bridge CHB-MLI. Type of MLI which using a single DC source rather than multiple sources is the diode-clamped MLI. While FC type is designed by series connection of capacitor clamped switching cells. CHB switches are connected in parallel and series in order to provide high power demand and high-power quality (Mondal *et al*., 2003; Krismadinata *et al*., 2013; Bandaru and Subbarayudu, 2011; Fri *et al*., 2013; Abdel-Rahim *et al*., 2013; Lei and Peng, 2013). For improving the quality of the output voltage inverter for two types of MLI as symmetriscal and asymmetrical, both types are very effective and efficient for multilevel inverter utilize reduced number of switching devices with hybrid topologies for the conventional and non-conventional multilevel inverter topologies to create

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a specified number of output voltage levels in operating in higher voltage levels based on DC voltage supply (Babaei *et al*., 2012; Ahmed *et al*., 2010). Reduced number of switches with installation area and cost and has simplicity of control system with a high number of steps associated using a new topology of Cascaded Multilevel Inverter (CHB-MLI) has been presented by Ahmed *et al*. (2010). A Current Source Inverter (CSI) apply a new topology for multilevel with reduced number of switches to generate desired output current for multilevel based on Sinusoidal Pulse Width Modulation (SPWM) method. This topology employs (n+7)/2 switches and (n-1)/2 current-sharing inductors for an n-level CSI has been developed by Hosseini *et al*. (2009). For 5-level single-phase inverter has been developed by Field Programmable Gate Array (FPGA). The digital control technique is generated based on multi carrier PWM in Altera DE2 board which has many features that allow design based on DC supply application of the system device have been implementation simulation and experiment results by Halim and Rahim (2011). A seven-level inverter has been simulated via. implementation of PWM techniques to reduce Total Harmonic Distortion (THD). Therefore with decrees number of gate driver in the circuit, there will be an increase for high voltage inverter. The circuitry consists DC supply and smaller (CHB-MLI) blocks connected in series to implementation its characteristic output waveform (Nedumgatt *et al*., 2012).

The energy SC as storage charged to applied modified CHB-MLIs. Important coding in order to control the modified CHB-MLIs using NR and PSO techniques for optimisation of the output of the modified CHB-MLIs for nine-levels is also, created and then embedded into DSP TMS320F2812. Most of the researchers applied PSO technique in a single phase of a conventional CHB-MLIs. The NR and PSO techniques are used to calculate switching angles with the capability to eliminate harmonics of the output CHB-MLIs. Finally, in this study method is evaluated and validated through experimental results.

MATERIALS AND METHODS

Super-Capacitor (SC) Model: A SC can be modeled by using some standard circuit components as shown in Fig. 1. This circuit design is used because a similar circuit

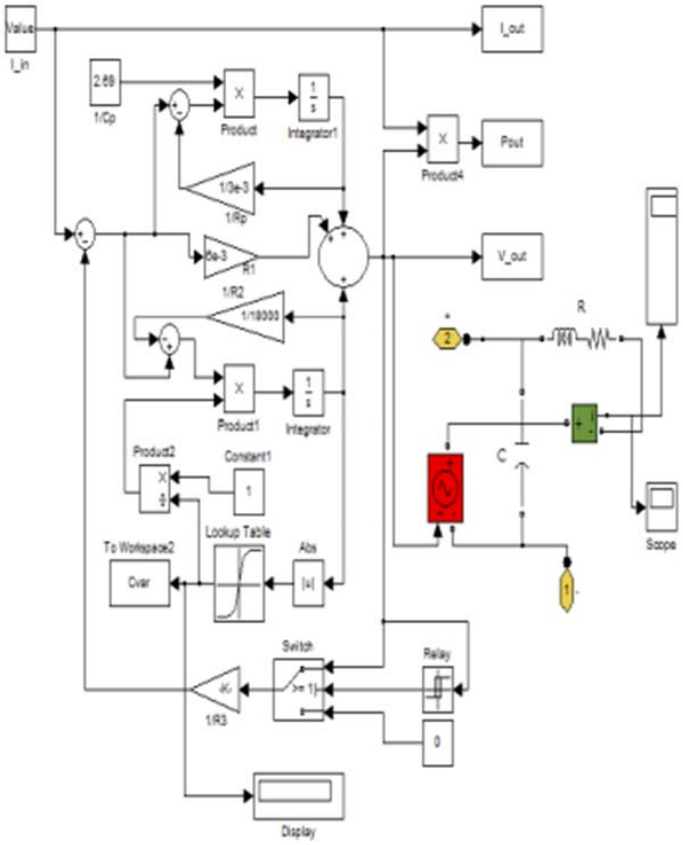

Fig. 1: Simulink model of SC

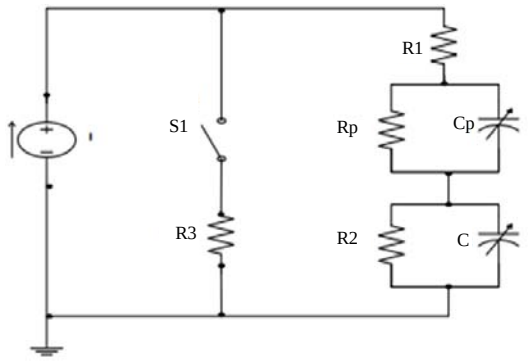

Fig. 2: The basic circuit model of the SC (EPOCS)

is presented in the datasheet for the SC from EPCOS and because of recommendations from the project supervisor. Simulink is used to create the first model of the SC according to, the basic circuit described in Fig. 2. Initial model testing is done with a simple circuit consisting of a resistance in series with a capacitance and resistance in parallel. This base circuit manages to show the basic function of the SC (Al-Janad *et al*., 2014). By adding more components until the circuit described in Fig. 1 is achieved, the accuracy of the model is improved. The Simulink Model used as the basic model of the SC is shown in Fig. 2. The relay block controls the switch that connects the balancing Resistance R3 to the circuit (Al-Janad *et al*., 2014).

Main capacitance: The capacitance value can be calculated in two different ways. The first method is to look at the voltage derivative during the charging of the Super-Capacitor (SC). The relation between voltage derivative and the capacitance is:

$$= \quad \text{dt} \qquad (1)$$

where, C = the capacitance. Using this relation, the capacitance can be calculated for different parts of the voltage curve. When high currents are used, other effects than the capacitance can affect the voltage level. These effects can cause the calculated capacitance value to be incorrect.

Switching operation modes of modified CHB-MLIS for nine-levels: The block diagram of a modified CHB-MLIs with SC source based on controller PSO algorithm as shown in Fig. 3. The switching mode operation of the proposed of a single-phase modified CHB-MLIs for nine-levels can be illustrated Fig. 4. As previously

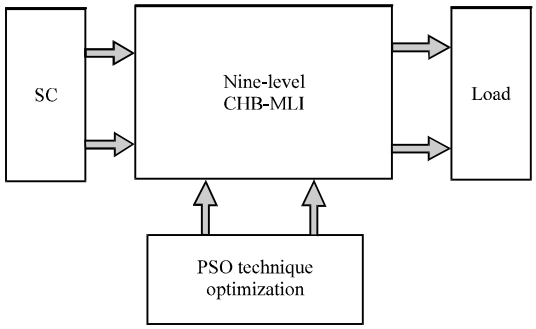

Fig. 3: Block diagram of a modified CHB-MLIs with SC source using PSO algorithm

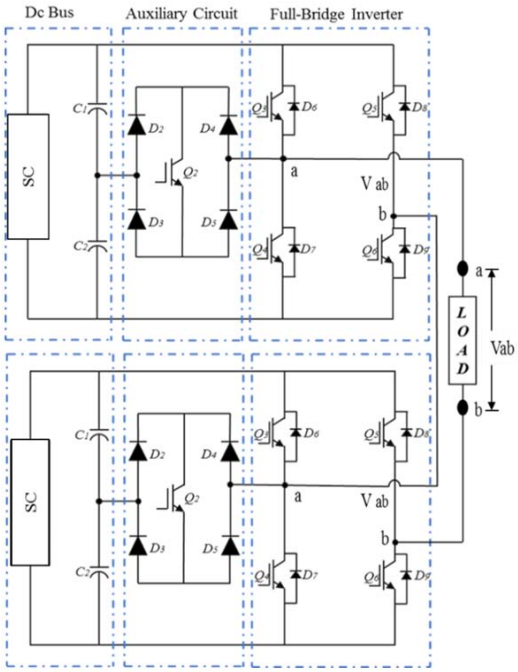

Fig. 4: Proposal modified of a CHB-MLI, single-phase nine-level topology

mentioned the proposed topology adopts a full-bridge configuration with an auxiliary circuit comprising four diodes and a switch and generates half-level DC bus voltage. To depict each switch's switching pattern, Fig. 5 shows the timing diagram or switching pattern of modified CHB-MLIs. The output voltages of modified CHBMLIs for nine levels can be summarized as described in Table 1. As a solution, this research presents a nine-level PWM inverter with output voltages V_{dc}, $V_{dc/2}$, $V_{dc/3}$, $V_{dc/4}$, zero, $V_{dc/4}$,-$V_{dc/3}$,-$V_{dc/2}$ and -V_{dc}. Increased number of output levels reduces harmonic content.

This section discussed the switching operation modes of modified CHB-MLIs for nine levels topology.

The switching operation modes are in state A-J as shown in Fig. 6, state A of Fig. 6 mentioned the equivalent power circuit of the proposed modified CHBMLIs in order to generate the output voltage level of V_{dc}. In order to achieve V_{dc} voltage level switches S_1, S_4, S_6 and S_9 must be in the state 1 or in ON conditions. Power switches S_1, S_4, S_9 and S_{10} are in state 1 in order to generate output voltage level of $V_{dc/2}$ as mentioned in state B of Fig. 6. Power switches S1. In Fig. 6, state C shows the equivalent power circuit of the proposed modified CHBMLIs to generate the output voltage level of $V_{dc/3}$. Power switch of Fig. 6 S_4, S_5, S_9 and S_{10} are in the state 1 to achieve $V_{dc/3}$ of voltage level. In Fig. 6, state D shows the equivalent power circuit of the proposed inverter to generate the output voltage level $V_{dc/4}$. Power switches S_4, S_5, S_8 and S_9 are in state 1 to achieve $V_{dc/4}$ voltage level. In Fig. 6, state E shows the equivalent power circuit of the proposed inverter to generate the output voltage level zero. To achieve zero level power switches S_3, S_4, S_8 and S_9 are in the state 1. In Fig. 6, state F shows another possibility to obtain zero voltage level. Power switches S_1, S_2, S_6 and S_7

Table 1: Output voltage for nine level to the switche's On = 1-Off = 0 condition

V_o	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	S_{10}
V_{dc}	1	0	0	1	0	1	0	0	1	0
$V_{dc/2}$	1	0	0	1	0	0	0	0	1	1
$V_{dc/3}$	0	0	0	1	1	0	0	0	1	1
$V_{dc/4}$	0	0	0	1	1	0	0	1	1	0
0	0	1	1	0	0	0	1	1	0	0
0*	1	1	0	0	0	1	1	0	0	0
$-V_{dc/4}$	0	1	0	0	1	1	1	0	0	0
$-V_{dc/3}$	0	1	0	0	1	0	1	0	0	1
$-V_{dc/2}$	0	1	1	0	0	0	1	0	0	1
$-V_{dc}$	0	1	1	0	0	0	1	1	0	0

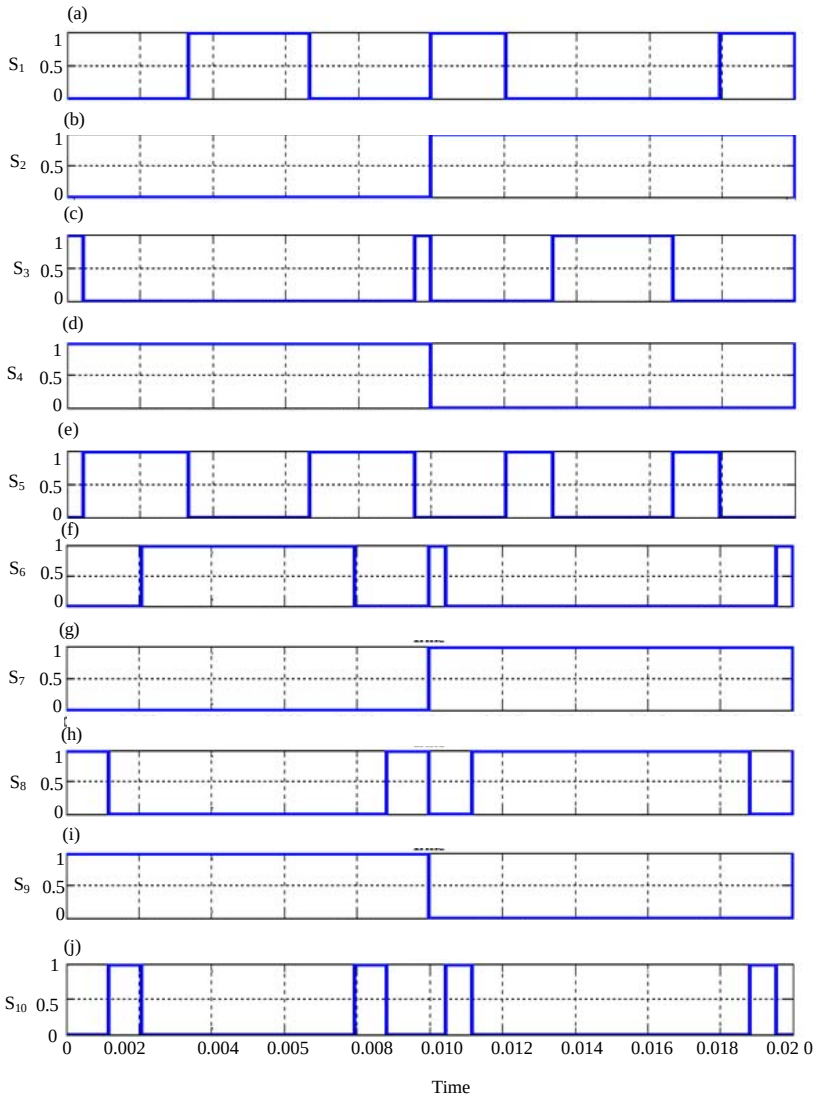

Fig. 5: a-j) Switching pattern of modified CHB-MLIs for nine-levels

are in state 1 to generate the zero level. In Fig. 6, state G shows the equivalent power circuit of the proposed inverter to generate the output voltage level-$V_{dc/4}$. Power switches S_2, S_5, S_6 and S_7 are in the state 1 to achieve -$V_{dc/4}$ voltage level. In Fig. 6, state H shows the equivalent power circuit of the proposed inverter to generate the output voltage level -$V_{dc/3}$. Power switches S_2, S_5, S_7 and S_{10} are in the state 1 to achieve -$V_{dc/3}$ voltage level. In Fig. 6, state I show the equivalent power circuit of the proposed inverter to generate the output voltage level -$V_{dc/2}$. Power switches S_2, S_3, S_7 and S_{10} are in the state 1 to achieve -$V_{dc/2}$ voltage level. Finally, in Fig. 6, state J shows the equivalent power circuit of the proposed inverter to generate the output voltage level -V_{dc}. Power switches S_2, S_3, S_7 and S_8 are in the state 1 to achieve -V_{dc} voltage level.

Analyses of the proposed topologies of a modified CHB-MLIS for nine levels

Fourier series for output voltage of proposed of a modified CHB-MLIS for nine level: The equations for 9-levels based on the Fourier series are described below (Vijayakumar *et al*., 2015):

$$\begin{aligned} f(t) &= f_{\theta 1}(t) + f_{\theta 2}(t) + f_{\theta 3}(t) + f_{\theta 4}(t) \\ &= \sum_{n=1,\,2,\,5}^{\infty} \frac{2V_{dc}}{n\pi}(V_{dc_1}\cos(1\alpha_1)) \\ &+ V_{dc2}\cos(3\alpha_2) + V_{dc3}\cos(5\alpha_3) + \\ &V_{dc4}\cos(7\alpha_4)\sin(nwt) \end{aligned} \quad (2)$$

Where:

V_{dc} = Voltage of each voltage source that was in unity

θ_i = The switching angles

From (2-1), four equations were resulted in eliminating the 5th harmonic.

$$\begin{aligned} V_{AN} &= V_{dc1} + V_{dc2} \\ b_n &= \frac{2V_{dc}}{\pi}\left\{\begin{matrix}\cos(n\alpha_1) + \cos(n\alpha_2) \\ \cos(n\alpha_3) + \cos(n\alpha_4)\end{matrix}\right\} n = 1,2,3,4 \end{aligned} \quad (3)$$

Equation 3 has s variables (θ_1, θ_2, θ_3 and θ_4) where, $0 < \theta_1 < \theta_2 < \theta_3 < \theta_4 < \pi/2$ and a solution set is obtained by assigning a specific value to the fundamental component, Vf and equating s-1 harmonics to zero as given below:

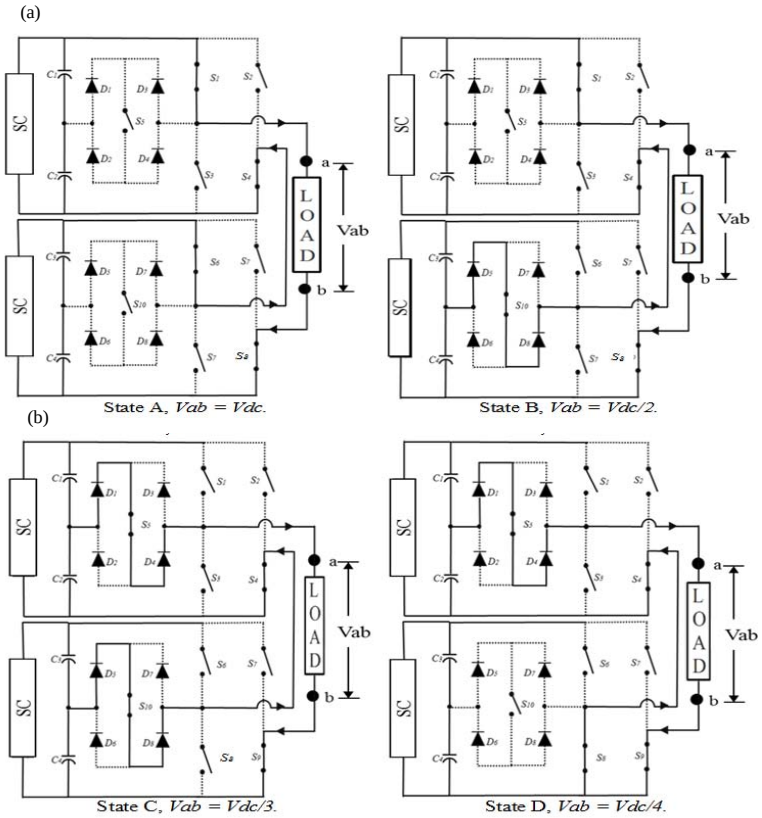

Fig. 6: Continue

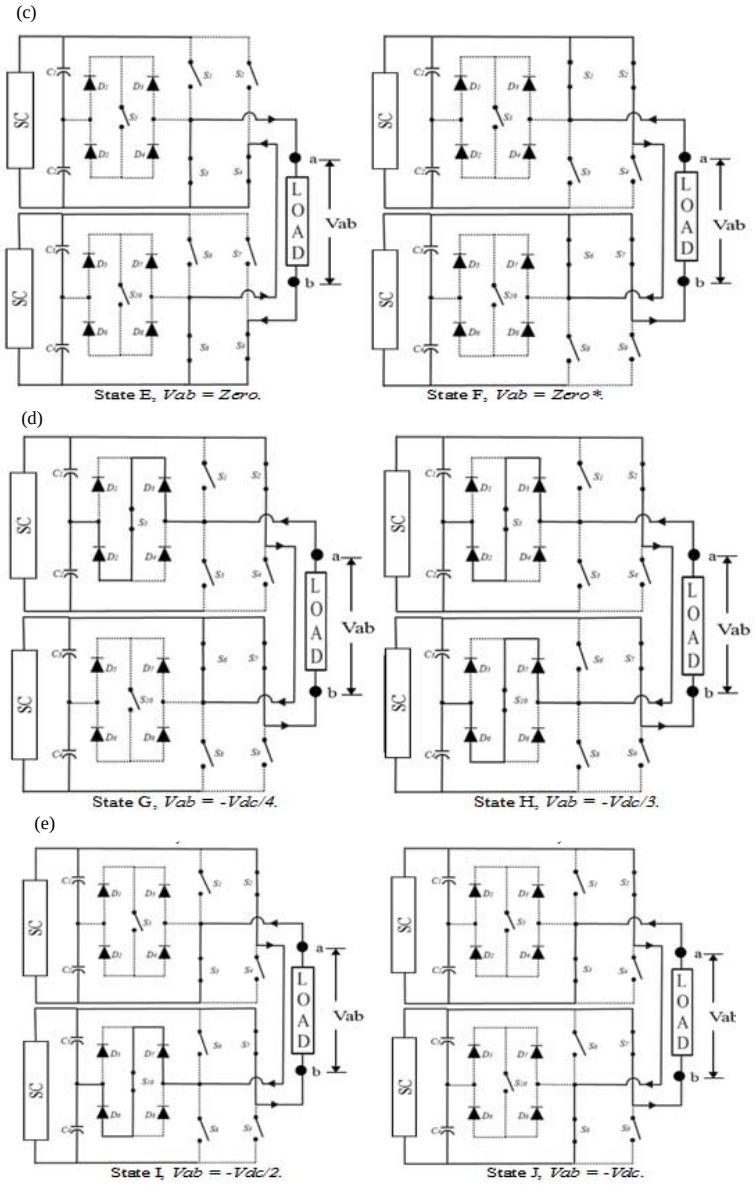

Fig. 6: a-e) Switching operating modes access of the modified CHB-MLIs for nine levels

$$\begin{aligned} &V_1\cos(\theta_1)+V_2\cos(\theta_2)+V_3\cos(\theta_3)+V_4\cos(\theta_4)=4m\\ &V_1\cos(3\theta_1)+V_2\cos(3\theta_2)+V_3\cos(3\theta_3)+V_4\cos(3\theta_4)=0\\ &V_1\cos(5\theta_1)+V_2\cos(5\theta_2)+V_3\cos(5\theta_3)+V_4\cos(5\theta_4)=0\\ &V_1\cos(7\theta_1)+V_2\cos(7\theta_2)+V_3\cos(7\theta_3)+V_4\cos(7\theta_4)=0 \end{aligned} \tag{4}$$

where, m = Vf/(2V_{dc}/π) and it is related to the modulation index MI by MI = m/sec where, 0<MI<1. An objective function is then needed for the optimisation procedure selected as a measure of effectiveness of eliminating selected order of harmonics while maintaining the fundamental component at a pre-specified value. Therefore, this objective function is defined as:

$$\begin{aligned} F(\theta_1,\theta_2,\ldots,\theta_s)=&\left[\sum_{n=1}^{s}V_1\cos(\theta_n)-m\right]^2+\\ &\left[\sum_{n=1}^{s}V_2\cos(3\theta_n)\right]^2+\left[\sum_{n=1}^{s}V_s\cos(2s-1)\theta_s\right]^2 \end{aligned} \tag{5}$$

The optimal switching angles are obtained by minimising Eq. (5) subject to the constraint $0<\theta_1<\theta_2<\theta_3<\theta_4<\pi/2$ and consequently, the required harmonic profile is achieved. The main challenge is the non-linearity of the transcendental set of Eq. 4 as most iterative techniques can be used with nine levels of the modified CHB-MLIs as shown in Fig. 7 of each step is explained as:

NR technique: The values of the conducting angles θ_1, θ_2, θ_3, θ_4 can be chosen by solving the transcendental equations using a modulation index formula Eq. 5 to obtain the suitable:

$$M = \frac{\pi V f}{2V_{dc}} \ (0 \leq M \leq 1) \tag{6}$$

where, modulation index values, MI. Other angles which are θ_5 until θ_{16} can be obtained by referring the output waveform of 9-levels of a modified CHB-MLIs theory in Fig. 5. The procedure of detecting attributes and configuration of a system is called optimisation. For only 1st, 3th, 5th and 7th harmonics can be eliminated chosen to be removed. Thus, the switching angle can be found by solving transcendental equations by using NR technique. In order to generate S_1, S_2, S_3, …, S_{16}, for 9-levels inverter, the switching pattern as shown in Fig. 5 are turned on and off in the right sequence in order to produce 9-level output voltage waveform of a modified CHB-MLIs. These switching angles are then examined for their corresponding THD given by:

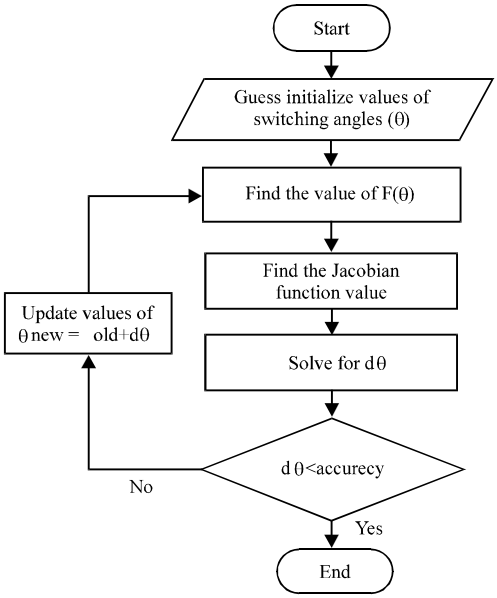

Fig. 7: General flow-chart of NR of the modified CHB-MLIs

$$THD_V = \frac{\sqrt{\sum_{n=1}^{\infty} V_n^2}}{V_1} \tag{7}$$

The effect of optimised angles for nine-levels are α_1, α_2, α_3 and α_4, on the THD and the modulation index is shown in Fig. 8. By using MATLAB coding for number of iterations, it can be easily concluded that the modulation index equal 0.81. However, the THD value of nine-levels equal to 9.4%.

Particle swarm optimization PSO technique: PSO has become a very popular technique in solving non-linear optimization problems. Many types of evolutionary algorithms; particle swarm is preferred primarily because of its computational efficiency, simplicity and ability to avoid local optima. PSO has the following key advantages over other evolutionary optimization techniques (Al-Othman and Abdelhamid, 2009; Letha *et al*., 2016; Gupta and Mahanty, 2015; Alamri *et al*., 2015). The PSO algorithm are required to

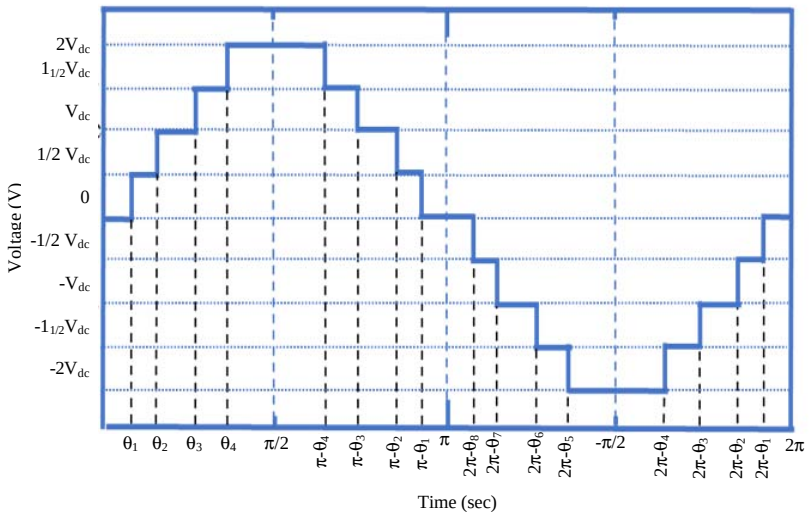

Fig. 8: Vab at low switching frequency of modified CHB-MLIs, for 9-levels

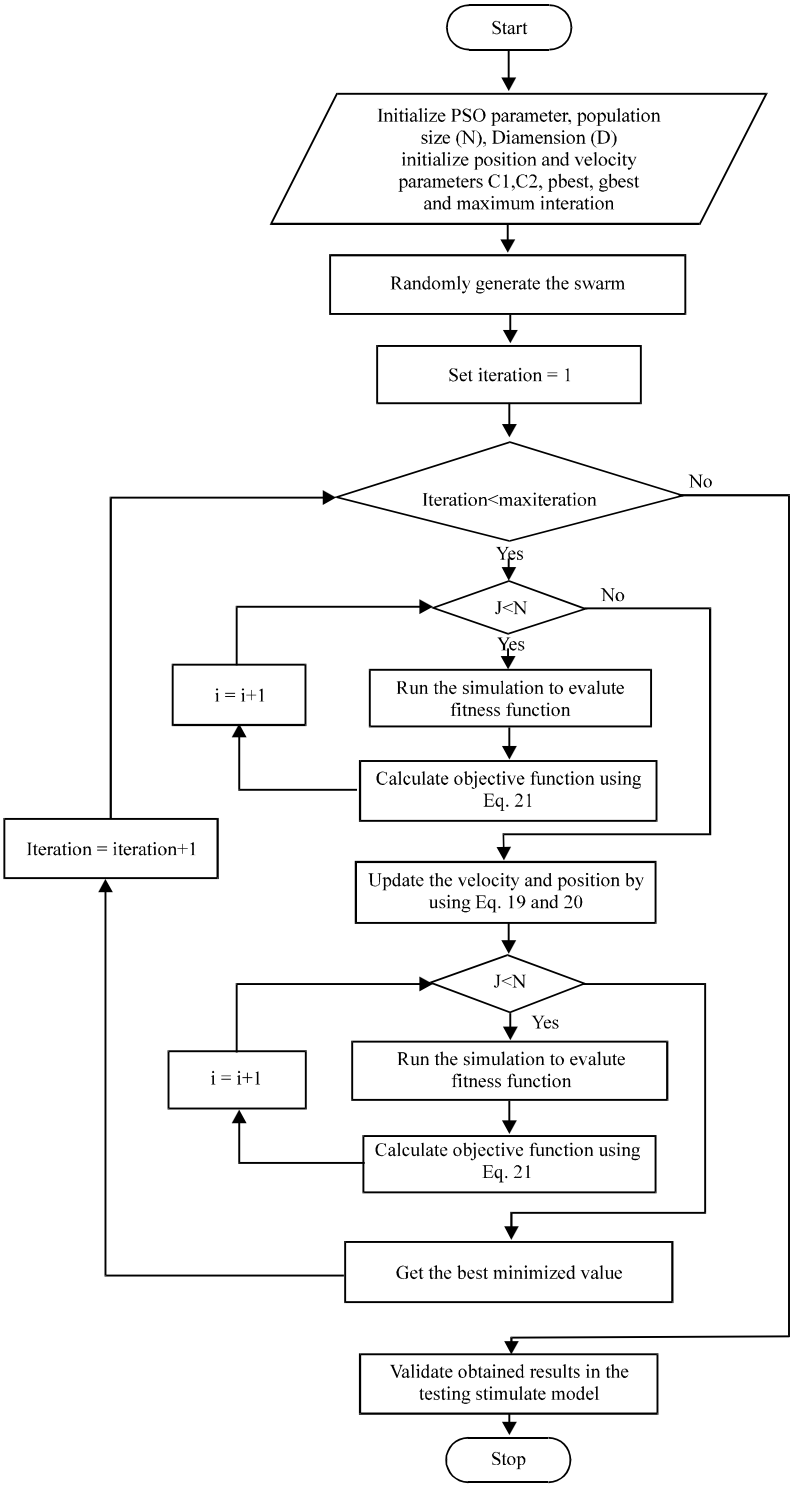

Fig. 9: General flow chart of PSO of a modified CHB-MLIs

solve nonlinear equations based on SHE algorithm for solving the transcendental equations in order to optimise best switching angles. The number of iteration algorithm is solved using MATLAB coding to get better angles and harmonic. From number of iteration PSO algorithm.

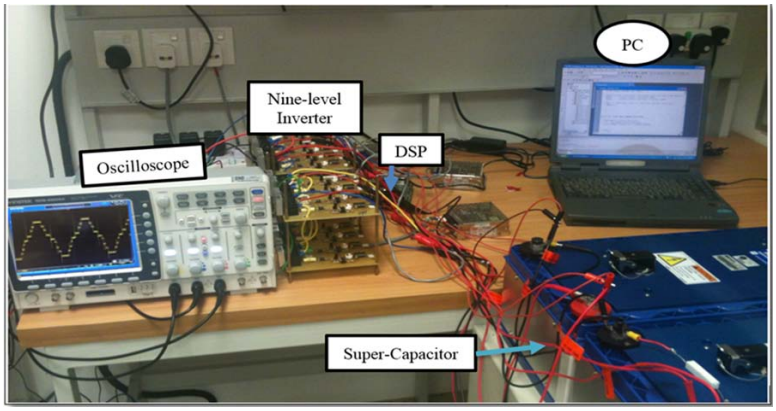

Fig. 10: The development of a single-phase of modified CHB-MLIs for nine-levels

Step 1: Initialise the system parameters such as velocity vector V_i, location vector X_i, personal best particle vector P_i, particle inertia weight C0 and global best vector P_g. Assign the values of generations as 100, population size as 40, cognitive parameter C1 as 0.5 and social parameter C2 as 1.25.

Step 2: Check for the case 0<(C1+C2)<2 and (C1+C2)/2<C0<1, if the two cases are satisfied then the system will be guaranteed to converge to a stable equilibrium point. If false, go to step 1.

Step 3: Update the velocity, $V_i(t+1)$:

$$V_{ij}(t+1) = V_i(t)+\gamma_{1i}(P_i-x_i(t))+\gamma_{2i}(G_i-x_i(t)) \quad (8)$$

Step 4: Update the Position, $X_i(t+1)$:

$$X_{ij}(t+1) = X_{ij}(t)+V_{ij}(t+1) \quad (9)$$

Where:

i = The particle index
j = The index of parameter of concern to be optimised
x = The position of the ith particle and jth parameter
k = The discrete time index, v is the velocity of the ith particle and jth parameter
P = The best position found by the ith particle and jth parameter (personal best)
G = The best position found by swarm (global best)
c = A random uniform number between [0,1] applied to the ith particle
u = The inertia function, a is the acceleration constants

Step 5: Now, utilize the fitness function in order to evaluate the particle:

$$THD_V = \frac{\sqrt{\sum_{n=1}^{\infty} V_n^2}}{V_1} \quad (10)$$

For harmonic reduction elimination. For switching angles 9-level α_1, α_2, α_3 and α_4 are selected in order to selective harmonics 1st, 3th, 5th, 7th eliminated.

$$\begin{aligned} F(1) &= (\cos(\alpha_1)+\cos(\alpha_2)+\cos(\alpha_3)+\cos(\alpha_4))-ma \\ F(2) &= (\cos(3*\alpha_1)+\cos(3*\alpha_2)+\cos(3*\alpha_3)+\cos(3*\alpha_4)) \\ F(3) &= (\cos(5*\alpha_1)+\cos(5*\alpha_2)+\cos(5*\alpha_3)+\cos(5*\alpha_4)) \\ F(4) &= (\cos(7*\alpha_1)+\cos(7*\alpha_2)+\cos(7*\alpha_3)+\cos(7*\alpha_4)) \end{aligned} \quad (11)$$

Step 6: Check the constraints $0\le\alpha_1\le\alpha_2\le\alpha_3\le\alpha_4\le\pi/2$.

Step 7: Check for the case $P(x_i)<P(P_i)$, if i = i+1 not satisfied then, execute to step 3.

Step 8: If the produced location of the particle is the best then update by change with the previous location as $P_i = X_i$.

Step 9: Update the global best location as P_g = min (P neighbour).

Step 10: Switching angles are optimised the best. Accomplish the solution of the problem. The general flow chart of PSO of a modified CHB-MLIs is shown in Fig. 9 and each step is explained below:

The hardware of modified CHB-MLIS for nine levels: The construction of the nine, levels of modified CHB-MLIs involves integrating the 10 pieces of power switching semiconductor IGBTs-IHW30N90T with snubber circuits, as shown in Fig. 10 IGBT possessed the capability of operating up to 250 kHz switching frequency and in supplying electric current at 60 A at 25°C and in becoming 30 A when the temperature of the IGBTs reached 100°C.

Normally, it can operate at 600 V DC towards the break down voltage at 900 V DC. These IGBTs can accept a maximum of ±30 V gate to emitter voltage pulse. More information pertaining to this IGBT-IHW30N90T. Besides, the single-phase switching signal to those IGBTs came from the gate drives circuits. The important aspects in the selection of IGBT had been the voltage of the IGBT collector to emitter. If the output phase voltage inverter designed had been 600 V AC (peak to peak), then a voltage source DC at 2×600V or 848.53 V DC super capacitor as storage would be needed to avoid break down voltage on IGBTs as the inverter output was loaded with resistance and inductance. Besides, the switching sequence of the voltage across IGBT had been similar to the voltage SC DC source. Another aspect was the electric current capacity that allowed flow through the IGBTs. This means that if the inverter was designed to drive the motor with high current, then IGBT with high current should be chosen due to its ability in conducting frequency switching. With high-frequency capability of IGBTs, then, high switching frequency, instead of low switching, could be applied on single-phase nine-level of a modified CHB-MLIs, so that, it could produce output with less harmonics.

RESULTS AND DISCUSSION

Experimental results of CHB-MLIS (MI = 0.81) using NR and PSO techniques: In order to obtain the optimisation of the output of a nine-level modified CHB-MLIs, a source code for optimisation using C language based on the NR and PSO techniques has been developed. The developed source code was then embedded into DSP-TMS320F2812. Figure 11 and 12 show the timing diagram of a modified

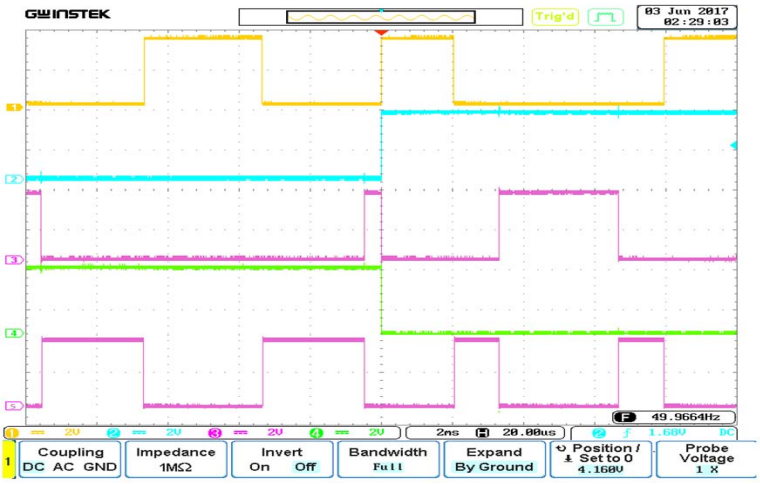

Fig. 11: Timing diagram of a modified CHB-MLIs of nine levels for cell one comprising S_1-S_5 switches with MI = 0.81 using NR technique

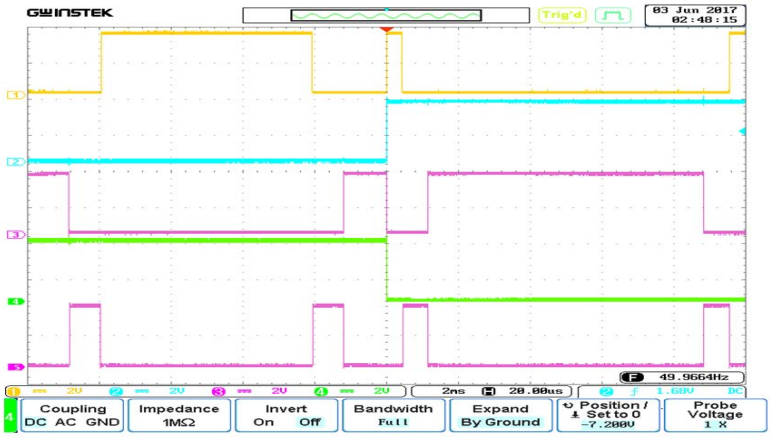

Fig. 12: Timing diagram of a modified CHB-MLIs of nine levels for cell two comprising S_1-S_5 switches with MI = 0.81 using NR technique

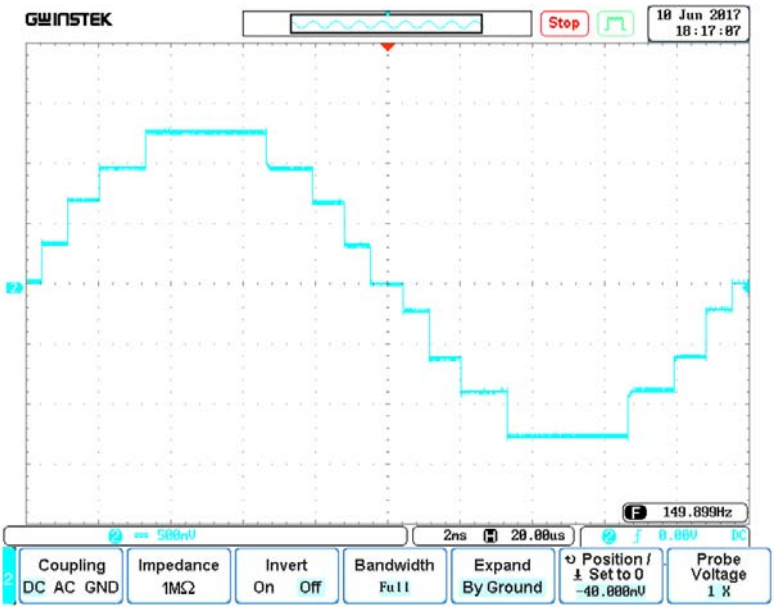

Fig. 13: Optimisation of output voltage waveform of a nine-level modified CHB-MLIs with MI = 0. 81 using NR technique

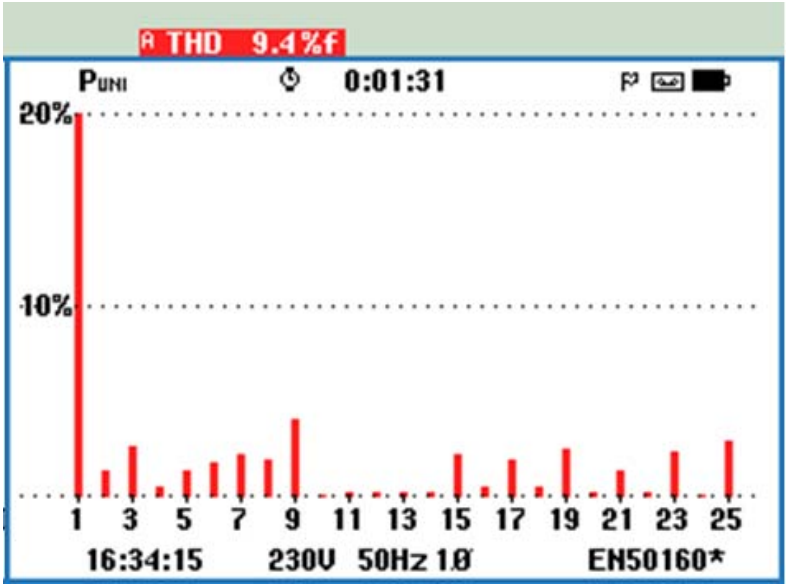

Fig. 14: Optimisation harmonic spectrum of output voltage waveform of a modified CHB-MLIs with MI = 0.81 using NR technique

CHB-MLIs of nine levels. There are two cells available in the configuration of a modified CHB-MLIs of nine levels as shown in the methodology. Each cell comprises five switches including bi-directional switch, namely S_1-S_4 and bi-directional switch S_5. From these figures, it is noted that the ten switches have equal switching periods using a switching frequency of 2500 Hz. The switching angles of a modified CHB-MLIs of nine levels were calculated using the NR technique and the obtained values of switching angles are equal to θ_1 = 9.6730, θ_2 = 19.37820, θ_3 = 36.7 and θ_4 = 59.3966. These switching angles have been coded into the source code and then embedded into DSP-TMS320F2812 in order to generate the output of the inverter waveform. In the source code programming, one cycle has the duration of 0.02s with an MI value of 0.81.

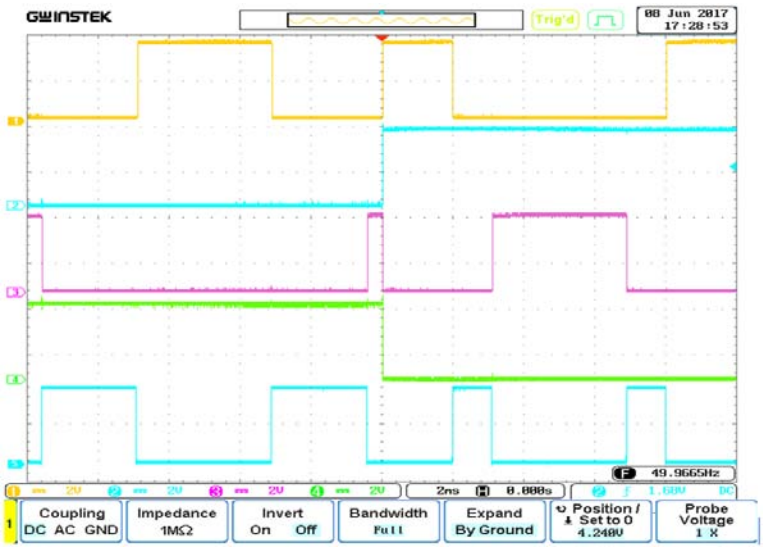

Fig. 15: Timing diagram of a nine-level modified CHB-MLIs for cell one comprising S_1-S_5 switches with MI = 0.81 using PSO technique

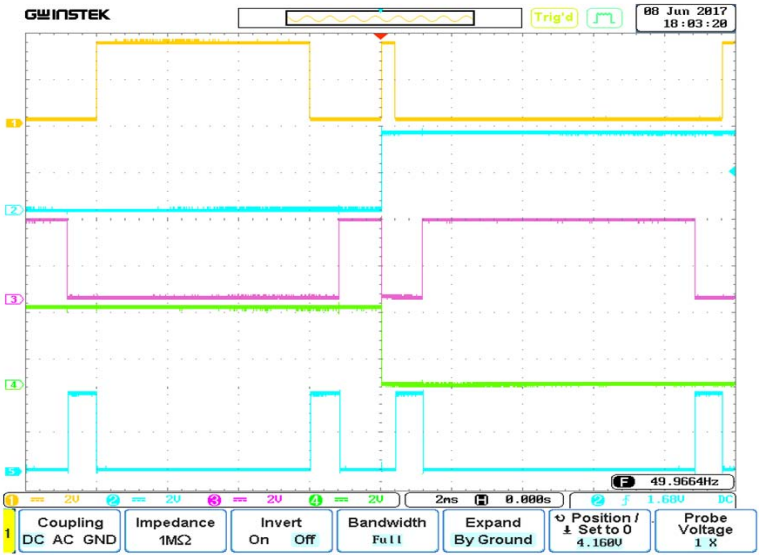

Fig. 16: Timing diagram of a nine-level modified CHB-MLIs for cell two comprising S_6-S_{10} switches with MI = 0.81 using PSO technique

Based on the obtained timing diagrams, the optimisation of output voltage waveform of a nine-level modified CHB-MLIs using the NR technique has been produced as shown in Fig. 13. In order to eliminate the specific order harmonics of the inverter output, the SHE technique of the fundamental switching frequency scheme is used. In this research, a modified CHB-MLIs with equal DC sources based on the super capacitor is used. The modulation strategy used here is SHEPWM, in which the nonlinear equations are involved. In order to obtain optimised switching angles for the low order harmonics, the NR and PSO methods are utilised. The output voltage harmonics of a modified CHB-MLIs using NR were measured as shown in Fig. 14 and its THD values are equivalent to 9.4%.

In Fig. 15 and 16 present the results of timing diagram of a modified CHB-MLIs of nine levels based on the PSO technique. The optimised switching angles obtained is equal to θ_1 = 7.2334, θ_2 = 21.0801, θ_3 = 35.9295 and θ_4 = 55.918.

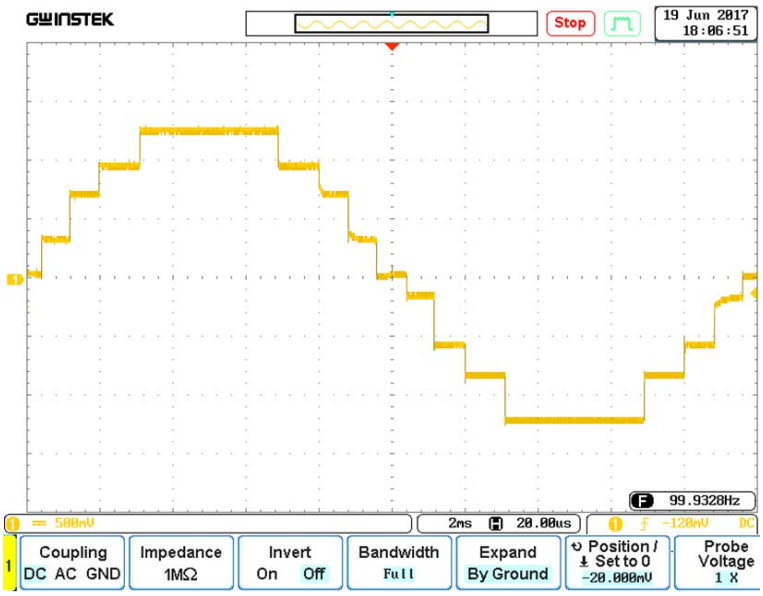

Fig. 17: Optimisation of output voltage waveform of a nine-level modified CHB-MLIs with MI = 0. 81 using PSO technique

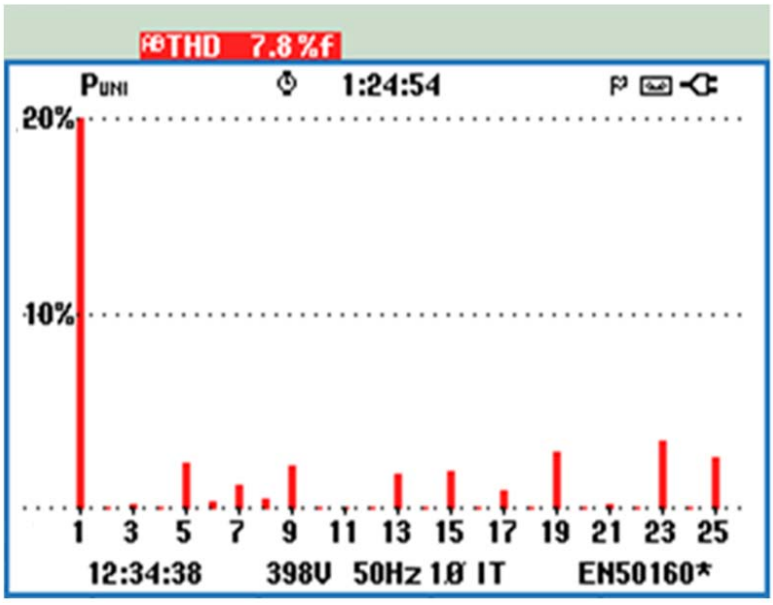

Fig. 18: Optimisation harmonic spectrum of output voltage waveform of a nine-level modified CHBs-MLIs with MI = 0.81 using PSO technique

Table 2: Overall values of MI, switching angles and THD for voltage of modified CHB-MLI for nine-levels based on NR and PSO techniques

Nine-level	MI	θ_1	θ_2	θ_3	θ_4	THD phase V (%)
NR	0.81	9.673	19.37	36.7	59.39	9.4
PSO	0.81	7.23	21.08	35.92	55.91	7.8

Figure 17 shows the optimisation of the output voltage waveform of a modified CHB-MLIs using the PSO technique. The optimisation of output voltage waveforms of a modified CHB-MLIs was smoother than the optimisation for the NR technique due to the inaccurate calculation of the switching angles. Figure 18 shows the optimisation harmonic spectrum of the output voltage waveform of a modified CHB-MLIs using PSO with THD values equivalent to 7.8%. As shown in Table 2 overall

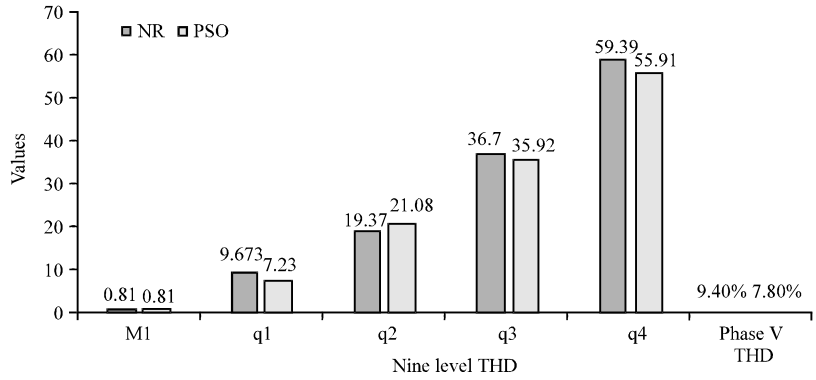

Fig. 19: Overall values of MI, versus the switching angles and the values of THD for voltage of modified CHB-MLI of 9-levels based on NR and PSO

values of MI, switching angles and THD for voltage of modified CHB-MLI for nine-levels based on NR and PSO techniques. Figure 19 shows the MATLAB plotting output for switching angles and the THD values for voltage based on NR and PSO techniques.

CONCLUSION

The experimental results showed that the higher level of inverter it will produce lower harmonics contents of the modified CHB-MLIs using the both techniques. However, PSO technique produce lower content of THD of the modified CHB-MLIs output voltage waveform compared to NR technique due to switching angles of the PSO technique is simple and efficient based on supply SC as storage. The coding based on NR and PSO techniques were then stored into DSP-TMS320F2812. However, PSO technique produce lower content of THD of the modified CHB-MLIs output voltage waveform compared NR technique due to switching angles of the PSO technique is simple and efficient.

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