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Aggressive Development of Qunatum-Dot Cellular Automata Technology (QCA) in Computers and Communications Networks

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Abstract: Higher speed, small area and more battery life are the prime factors in the fields of communication and information technologies. Complementary Metal Oxide Semiconductor (CMOS) technology uses presently for the physical network systems designs which have lot of limitations when it scaled to a nano-level, scientists and researchers have proposed several alternative technologies as solutions to replace CMOS by Quantum dot Cellular Automata (QCA) technology. QCA is one such promising alternative technology and possible solution for a perfect replacement of CMOS technology for designing digital circuits such as combinational and sequential circuit which have more occupation in the communication and computer systems. In this study, the sequential circuits D flip flop and shift register have been implemented with QCA technology. First, proposed a novel design of D Flip Flop (D-FF) and then the proposed D-FF has been utilized to implement the various shift registers (SISO, SIPO and PIPO). QCA based designs offers the features of significant reduction in design area, cell count and superior performance in speed as compared to the existing CMOS designs. QCA based clocked DFF offers an improvement of 45% in cell count, 65% design area and 60% minimizes the number of clock zones requirement.The proposed QCA design of clocked DFF with clear provides clear provide an improvement the cell count by 44, 40% in the design area and 40% clock zones reductionin relative to the existing designs. All these proposed designs are captured and simulated using a designing tool called QCA Designer 2.0.3.

Key words: CMOS, Quantum Cellular Automata (QCA), D-flip flop, Serial-In-Serial-Out (SISO), shift register, PIPO

INTRODUCTION

As the size of the conventional CMOS technology shrinkage down to cope up with the Moore's law about beyond 20 nm, it causes significant power dissipation and other short channel effects take place. Consequently, further CMOS scaling becomes more difficult and the design complexity disrupt the circuit operations. QCA is one of the most attractive, promising alternatives to the CMOS in designing digital circuits at nano scale using computational dots. The advantages of QCA are higher switching speed (up to terahertz frequency), lower power consumption and high packing density (Tougaw and Lent, 1994; Kim, 2010). QCA is a transistor less technology and is based on the fundamental principle of quantum confinement. These advantages have caused aggressive development of QCA technology in the field of nano computers/processors and in communication networks. In this study, an optimized and an efficient QCA based D-FF has been proposed and designed exploiting the inherent property of QCA clocking zones. The proposed D-FF layout is much more efficient in terms of cell count, design area and delay. In this study layout of efficient and optimized three different 4-bit shift registers (SISO, SIPO and PIPO) are designed usingproposed QCA D-FF. The designs and simulationsare performed using QCA Designer Version 2.0.3 Software tool. The simulation results are provided to verify the designs.

Background of QCA: The basic element in QCA technology is the QCA cell which consists of four 5 nm diameter charge containers known asquantum dots. These four quantum dots are placed at the corners of 18×18 nm^2

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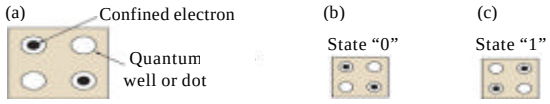

Fig. 1: a) Unpolarized cell; b) Polarization-1 (Logic '0') and c) Polarization +1 (Logic '1')

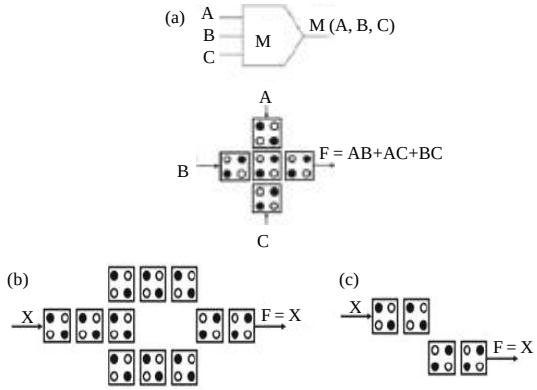

Fig. 2: a) 3-input majority gate; b) Robust inverter and c) Corner inverter

area. Each QCA cell contains two free electrons positioned in two quantum dots and the remaining two dots are empty. Electrons inside the cell always tend to occupy antipodal structures as a result of their mutual electrostatic repulsion. The two electrons in a cell can quantum mechanically tunnel between diagonal dots but they cannot tunnel between cells. QCA structures can be formed by an array of quantum cells with in which every cell has an electrostatic interaction with its neighboring cells. QCA cell is driven to one of three possible states in which one is unpolarized and two are polarized states based on the clock phase as in Fig. 1 (Lent *et al*., 1993). Fig. 1a is the relax state or unpolarized state and two possible polarization states represent two logical values Logic '0' and '1' are shown in Fig. 1b and c, respectively.

The logic elements in QCA: Most primitive gates of QCA are NOT gate and majority gate (Huang *et al*., 2007; Walus *et al*., 2004; Kim *et al*., 2007; Momenzadeh *et al*., 2005). To implement any Boolean function, the NOT gate and three input majority gate are required.

Majority gate: It is basic logic component in QCA circuit design. It has five QCA cells, three binary inputs and one output as in Fig. 2a. A-C are binary inputs and Y is the output. The output Y is given by Boolean Eq. 1:

$$Y = AB+AC+BC \quad (1)$$

where, M is the majority function, the output of a QCA majority gate is a binary value. Truth table of the majority

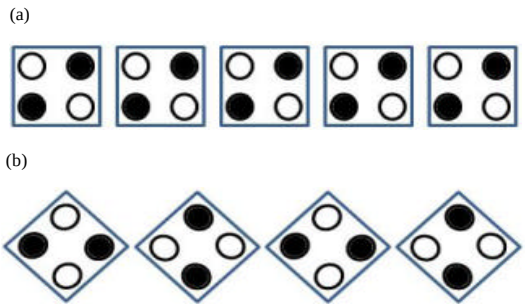

Fig. 3: QCA wires: a) Simple wire and b) Inverted wire

Table 1: QCA majority gate truth Table

Inputs			Outputs
A	B	C	Y
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

is shown in Table 1. By fixing one of the input of majority gate to a particular logic value and and or gates can be implemented. If one of the input of the majority gate is held at polarization P = +1(Logic '1'), then majority gate perform logical or operation over other remaining two inputs, otherwise, if P = -1(Logic '0') then majority gate perform and logical operation over the remaining two inputs.

Inverter: This is another main logic element which produces complement of the input. The robust structure of the inverter as well as corner inverter has been shown in Fig. 2b and c, respectively. With these basic gates, i.e., and gate or gate and inverter any logical function can be implemented (Tougaw and Lent, 1994).

QCA wire: QCA wire structure is formed by an array of QCA cells to transmit the binary signal from one end to the end as in Fig. 3. QCA wiring can be implemented in two ways. Simple binary wire can be formed by taking series connection of QCA cells with 90° orientation to transfersame logical value from one end to another end and the series connection of QCA cells with 45° orientation to get inverted binary wire.

QCA clocking scheme: QCA clock plays important role in fixing the direction of propagation of signal and to provide power to run a circuit (Liu and Lent, 2004). A four phase clocking scheme used with QCA cells. A clock zone divided into four phases:

- Switch
- Hold
- Release
- Relax as in Fig. 4.

The phase lag between two adjacent clock zones are equal to 90° and the phase lag between non-adjacent clock zones, i.e., clock 0 and 2 as well as clock 1 and 3 equal to 180°. Clock phase controls the inter dot barrier energy during the change of binary logic states from '1-0' or '0-1'. The barrier among the quantum dots are either raised or lowered depending on the different phases of the clock. In switch phase the inter dot barriers begin to raise to fix the polarization of the cell. In hold phase, the intra-barrier is too high which will not allow altering the position of electron. Hence, the orientation of cell holds the same state as that of switch state. In release phase the inter dot barrier again starts to be reduced and the cell starts moving to an unpolarized state. Finally, in the relax phase, there is no interdot barrier is present and said to be in the unpolarized state (Asfestani and Heikalabad, 2017; Tahoori *et al*., 2004; Momenzadeh *et al*., 2004; Ahmad *et al*., 2014; Sarkar, 2013; Vetteth *et al*., 2003; Beigh and Mustafa, 2015).

Existing work on QCA D-FF

QCA based D-FF: It can be built by a QCA binary wire consisting of four clock zones as shown in Fig. 5a. Latching can be obtained through timing by using four phases of clock assignment. Simple QCA D-FF structure implementation does not have the provision of separate external clock control signal as input. This limitation overcomes by incorporating the clock as shown in Fig. 5b. Boolean expression of the D-FF with clock control is given by Eq. 2:

$$Q_{(t)} = Dclk + \overline{clk}Q_{(t-1)} \quad (2)$$

To reset the D-FF output 'Q', another input clear active low signal is assigned as shown in the Fig. 5c. Recently proposed clocked QCA D-FF requires cell count 33, design area 0.02856 μm^2 and number of clock zones 5 as shown in Fig. 6a. As combination of four clock zones constitute one clock cycle 5 clock zones form 1.25 clock cycles.

Another D-FF depicted in Fig. 6b need cell count 35, design area 0.03635 μm^2 and latency 5 clock zones. The D-FF which require cell count 33, design area 0.03513 μm^2 and latency 1.25 clock cycles presented in Fig. 6c. Figure 6d shows QCA D-FF which needs 43 QCA cells, design area 0.04687 μm^2 and 5 clock zones. The QCA D-FF depicted in Fig. 6e need cell count 48, design area 0.04817 μm^2 and 5 clock zones. Another D-FF design requires 43 cells, 0.0556 μm^2 and 7 clock zones shown in Fig. 6f. The design presented in Fig. 6g need cell count 68, design area 0.09187 μm^2 and latency 1.75 clock cycles.

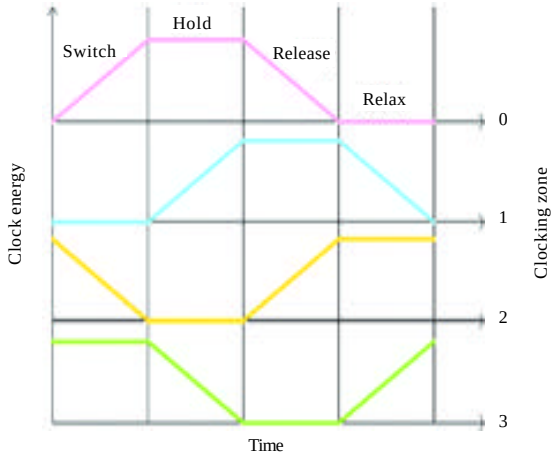

Fig. 4: Four phase QCA clock zones

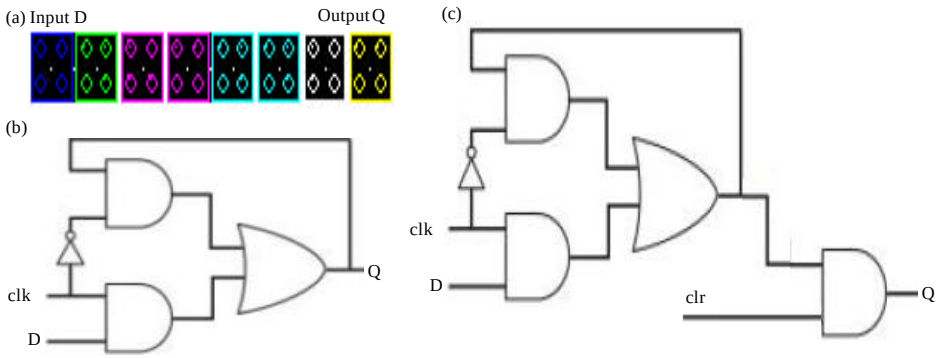

Fig. 5: a) Unclocked simple QCA D-FF; b) Clocked QCA D-FF and c) Clocked QCA D-FF with clear signal

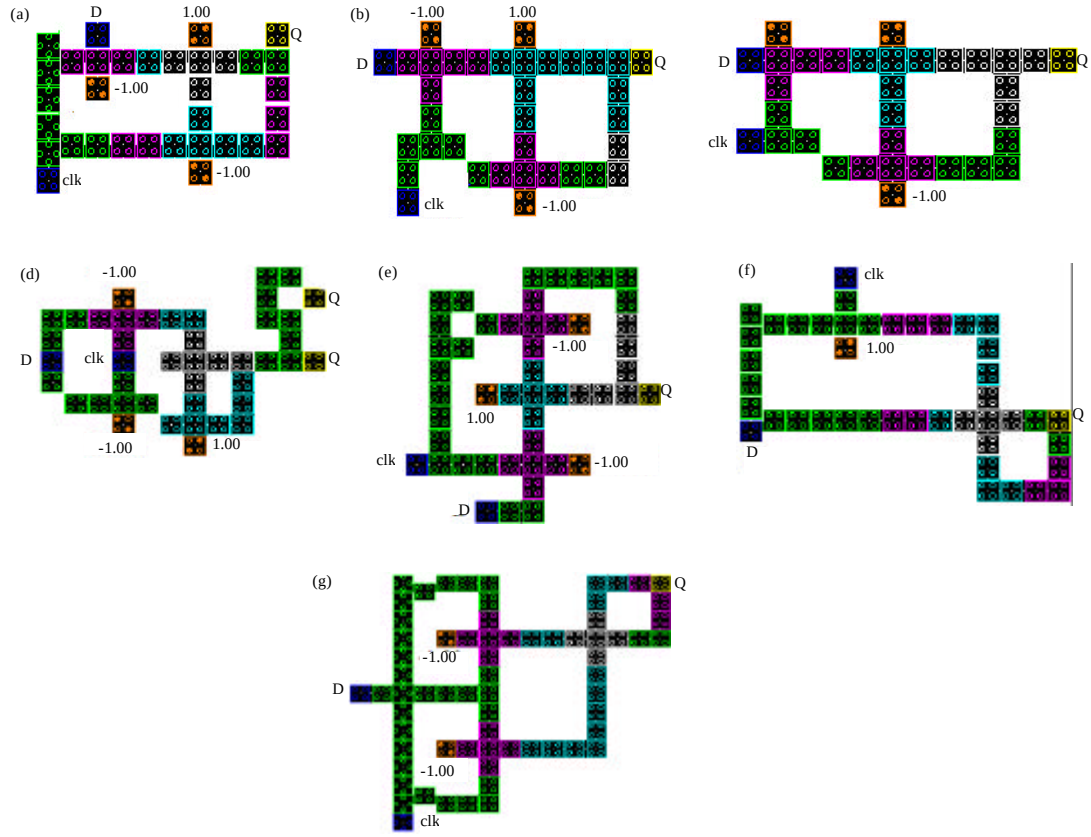

Fig. 6: QCA layouts: a) Reshi *et al.* (2015); b) Beigh and Mustafa (2015); c) Ahmad *et al.* (2014); d) Chakrabarty *et al.* (2018); e) Dehkordi *et al.* (2011); f) Sarkar (2013) and g) Vetteth *et al.* (2003)

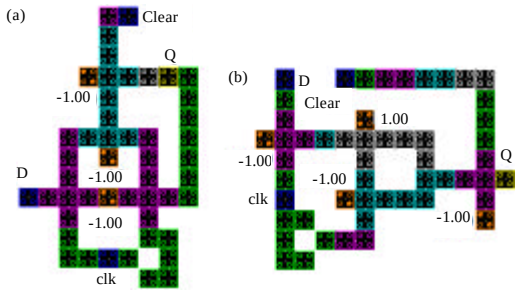

Fig. 7: QCA layouts: a) Purkayastha *et al.* (2018) and b) Sabbaghi-Nadooshan and Kianpour (2014)

QCA clocked D-FF with clear: QCA clocked D-FF with active low clear signal shown in Fig. 7a require cell count 48, design area 0.05 μm^2 and 3 clock zones as in Fig. 7a (Beigh and Mustafa, 2015). Figure 7b shows the design which need cell count 52, design area 0.07 μm^2 and 6 clock zones (Dehkordi *et al.*, 2011).

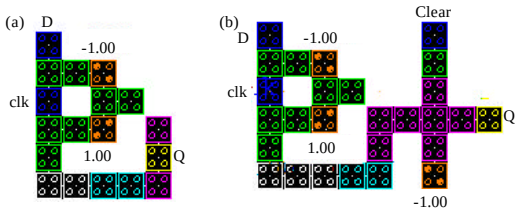

Fig. 8: Proposed QCA D-FF: a) Clocked and b) Clocked with clear

MATERIALS AND METHODS

Proposed QCA D-FF: In proposed QCA D-FF, the arrangement of QCA cells employs the inherent characteristics to perform the functionality of D-FF as shown in Fig. 8 (Reshi *et al.*, 2015). The proposed clocked DFF design requires cell count 18, design area 0.01 μm^2 and 2 clock zones as depicted in Fig.8a. The proposed D-FF with clear signal need 27 QCA cells, design area 0.03 μm^2 and 2 clock zones as shown in Fig. 8b. Proposed clocked D-FF simulation results have been

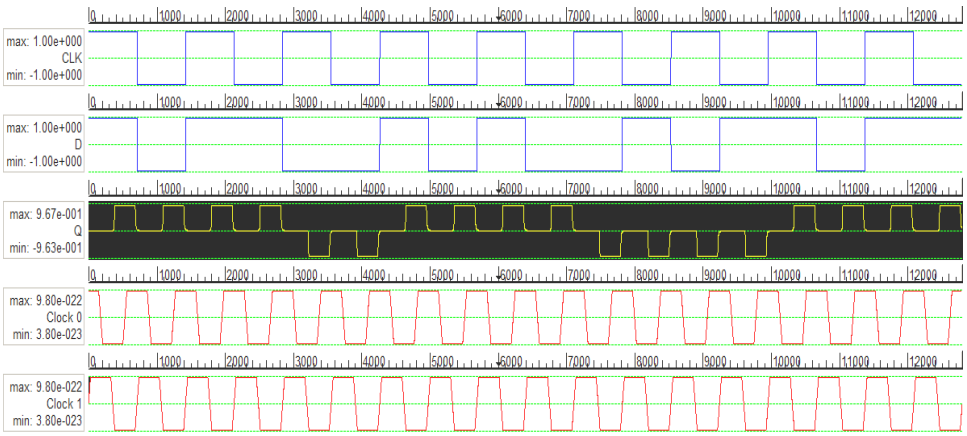

Fig. 9: Simulation results of proposed clocked QCA D-FF

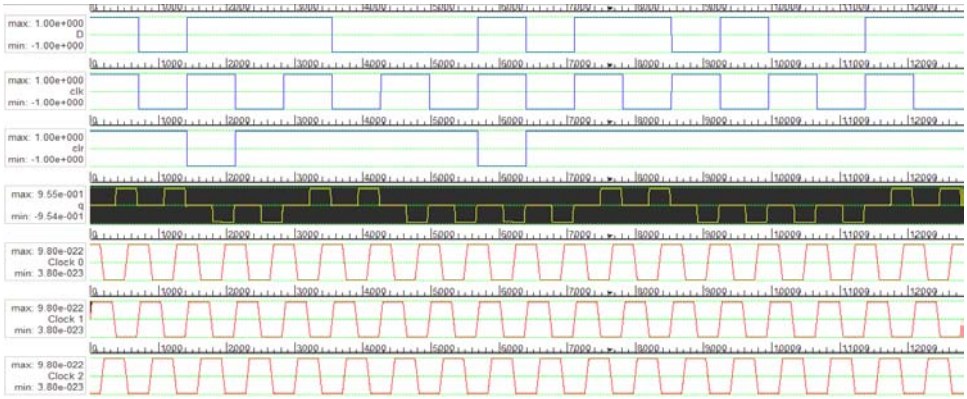

Fig. 10: Simulation results of proposed clocked QCA D-FF with clear signal

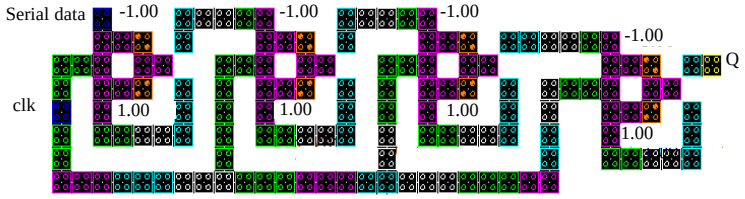

Fig. 11: Proposed SISO SR with clocked D-FF

shown in Fig. 9. The proposed clocked D-FF has been used to generate an area efficient and optimized 4 Bit Shift Registers (4-Bit SRs) such as Serial Input Serial Output (SISO), Serial in Parallel Out (SIPO) and Parallel in Parallel Output (PIPO) shift registers (Fig. 10).

Proposed 4-bit SISO register: Area efficient and optimized 4-bit SISO SR designed with proposed D-FF is in Fig. 11. Here, the proposed SISO SR occupies an area of 0.1156 μm^2, 138 cells and latency of 3.75 clock cycles (Fig. 12).

Proposed 4-bit SIPO register: Proposed clocked QCA D-FF has can be used to generate an area efficient and optimized 4-bit SIPO SR is shown in Fig. 13. Here, the 4 bit SIPO SR occupies an area of 0.11 μm^2, 138 cells and latency of 3.75 clock cycles (Fig. 14).

Proposed 4-bit PIPO register: An improved version of 4-bit PIPO SR in terms of cell count, design area and latency generated using proposed D-FF is shown in Fig. 15 and 16. Here, the 4-bit PIPO SR occupies an area of 0.117 μm^2, 133 cells and latency of 0.75 clock cycle.

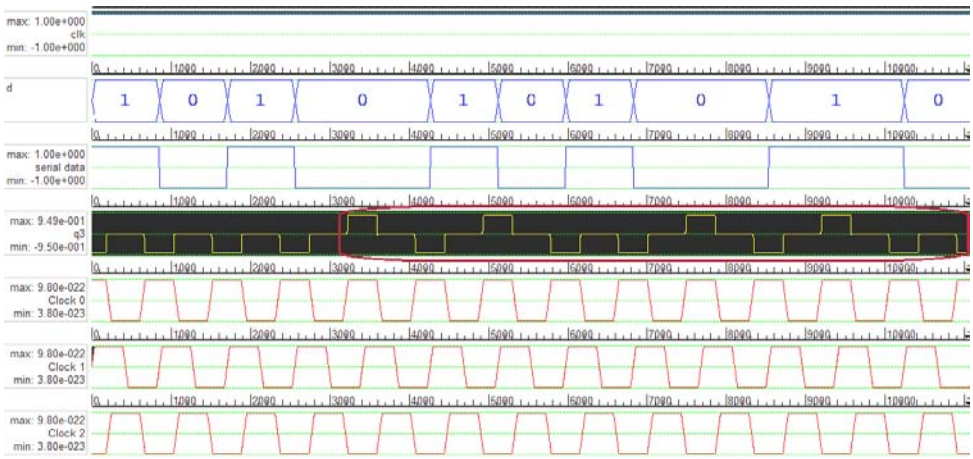

Fig. 12: Simulation results of SISO shift register using proposed clocked QCA D-FF

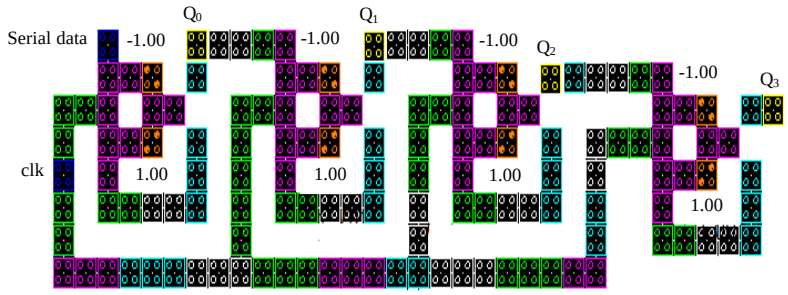

Fig. 13: SIPO SR using proposed clocked QCA D-FF

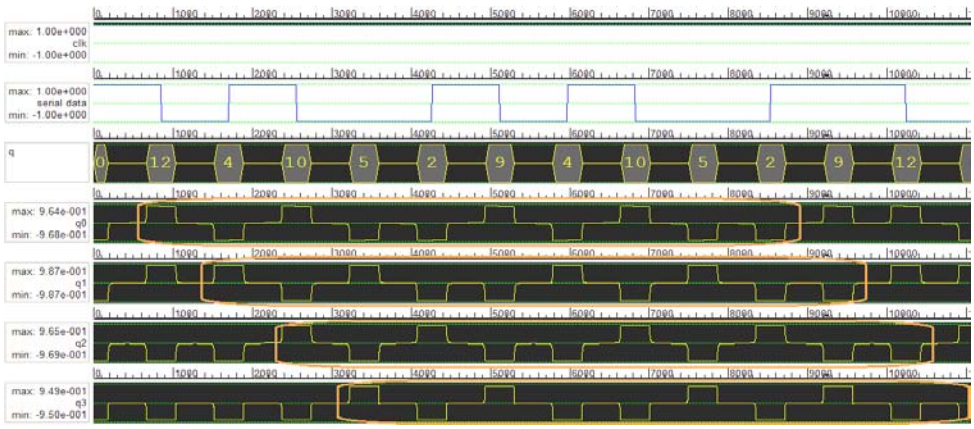

Fig. 14: Simulation results of SIPO shift register using proposed clocked QCA D-FF

Proposed 4 bit SISO register using D-FF with clear: Area efficient and optimized 4-bit SISO SR has been implemented using proposed D-FF with clear signal is shown in Fig. 17.

An active low clear signal is used to reset the D-FF irrespective of input and clock. Here, the 4-bit SISO SR occupies the design area of 0.19 μm^2, 215 QCA cells and latency 3.75 clock cycles (Fig. 18).

Proposed 4-bit SIPO register using D-FF with clear: Proposed clocked QCA D-FF has been used to design an area efficient and optimized 4-bit SIPO SR as shown in Fig. 19-22. Here, the 4 bit SIPO SR occupies an area of 0.19 μm^2, 215 QCA cells and 3.75 clock cycles latency.

Proposed 4-bit PIPO register using D-FF with clear: An improved version of 4-bit PIPO SR in terms of cell count,

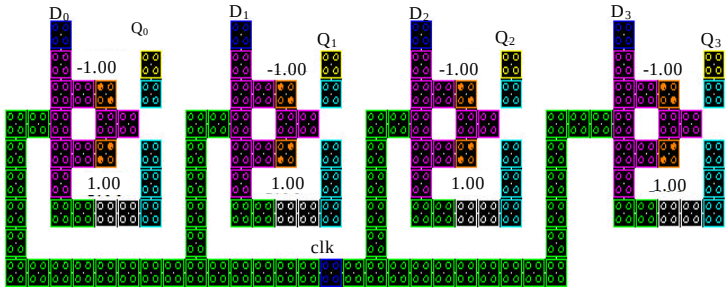

Fig. 15: PIPO SR using proposed clocked QCA D-FF

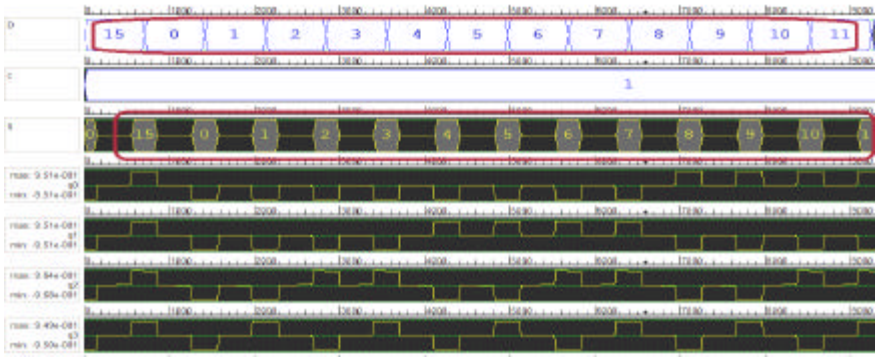

Fig. 16: PIPO shift register using proposed clocked QCA D-FF

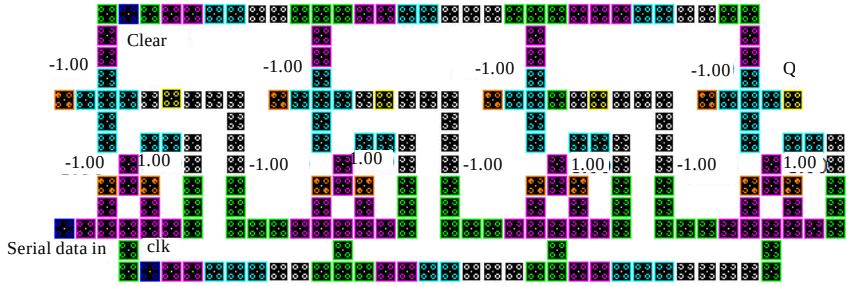

Fig. 17: SISO SR using proposed clocked D-FF with clear

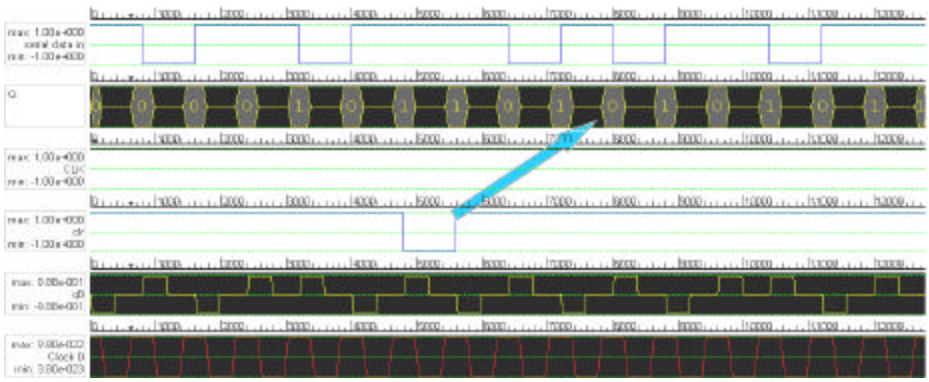

Fig. 18: SISO shift register using proposed clocked QCA D-FF with clear

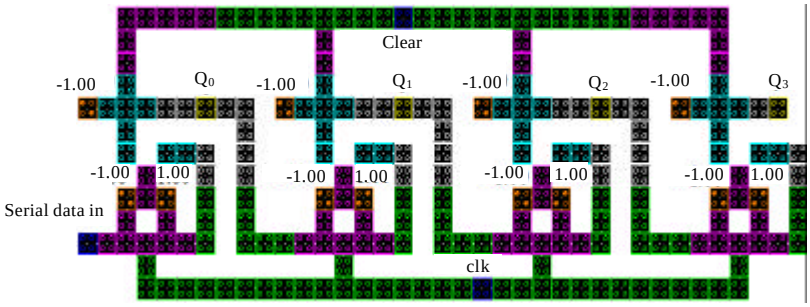

Fig. 19: SIPO SR using proposed clocked QCA D-FF with clear

Fig. 20: Simulation results of SIPO shift register using QCA clocked D-FF with clear

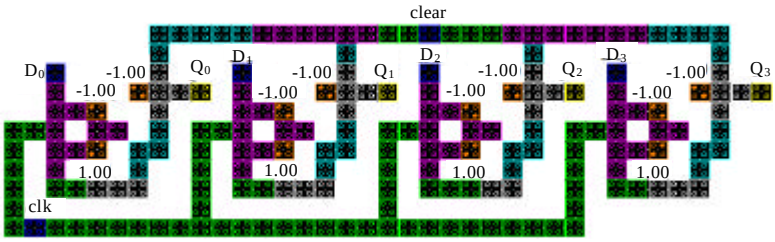

Fig. 21: PIPO SR using proposed clocked QCA D-FF with clear

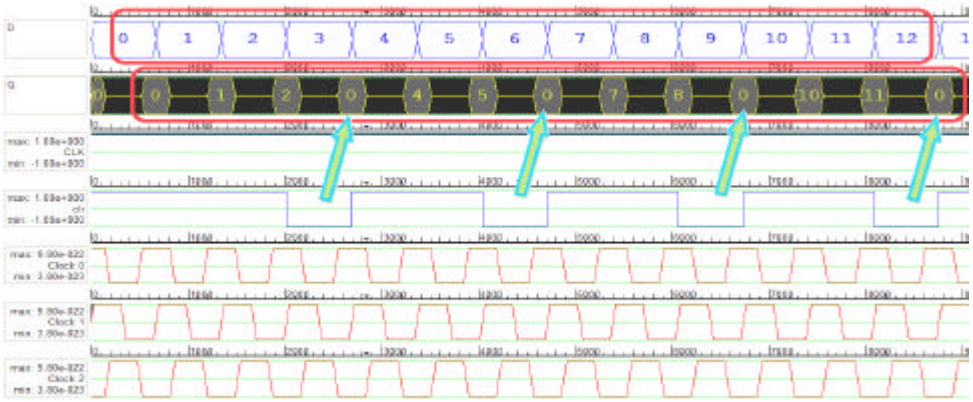

Fig. 22: Simulation results of PIPO shift register using QCA clocked D-FF with clear

design area and latency is implemented using proposed QCA D-FF with clear as shown in Fig. 21. Here, the 4-bit PIPO SR occupies an area of 0.18 μm^2, 206 QCA cells and latency is 1 clock cycle (Fig. 22).

RESULTS AND DISCUSSION

Performance analysis of existing and proposed clocked D-FFs: The comparison of various types of clocked QCA D-FF has been shown in Table 2. As shown in Table 2, the proposed design provides an improvement of 45% in the cell count, 65% in the design area, 60% in number of clock zones compared to existing best clocked DFF designs.

According to Table 3, SISO shift register using proposed clocked QCA DFF provides 28% improvement of cell count, 39% design area and 12% reduction in number of clock zones relative to best existing designs.

From Table 4, it can be observed that the proposed design offer an improvement of 28% cell count and 42% design area and 12% in the clock zones compared to existing best SIPO shift register designs.

From the observation of performance analysis of Table 5 of various PIPO shift registers, it can be seen that the proposed design allows an improvement of 23% cell count, 37% in the design area and 40% in the number of clock zones relative to the existing PIPO shift register design.

According to Table 6, the proposed QCA clocked DFF with clear provides 44% improvement of cell count, 40% in the design area and 40% improvement in clock zones compared to best existing designs.

By the observation of performance analysis of Table 7 it can be noticed that the proposed design offer an improvement of 13% cell count and 31% design area compared to existing best PIPO shift register designs.

Table 2: Comparison of various types of clocked D-FF

References	Cell count	Ratio	Design area (μm^2)	Ratio	Latency (in clock zones)
Proposed	18	1.00	0.01000	1.00	2
Reshi *et al.* (2015)	33	1.83	0.02856	2.86	5
Beigh and Mustafa (2015)	35	1.94	0.03635	3.63	5
Ahmad *et al.* (2014)	33	1.83	0.03513	3.51	5
Chakrabarty *et al.* (2018)	43	2.39	0.04687	4.69	5
Dehkordi *et al.* (2011)	48	2.67	0.04817	4.82	5
Sarkar (2013)	43	2.39	0.05560	5.56	7
Vetteth *et al.* (2003)	68	3.78	0.09187	9.18	7

Table 3: Comparison of various SISO shift registers

References	Cell count	Ratio	Design area (μm^2)	Ratio	Latency (in clock zones)
Proposed	138	1	0.11	1.00	15
Reshi *et al.* (2015)	191	1.38	0.18	1.63	17
Ahmad *et al.* (2014)	204	1.48	0.22	2.00	16
Beigh and Mustafa (2015)	194	1.40	0.22	2.00	16

Table 4: Comparison of various SIPO shift registers

References	Cell count	Ratio	Design area (μm^2)	Ratio	Latency (in clock zones)
Proposed	138	1.00	0.11	1.00	15
Reshi *et al.* (2015)	191	1.38	0.19	1.72	17

Table 5: Comparison of various PIPO SRs

References	Cell count	Ratio	Design area (μm^2)	Ratio	Latency (in clock zones)
Proposed	133	1.00	0.12	1.00	3
Reshi *et al.* (2015)	173	1.30	0.19	1.58	5

Table 6: Comparison of various QCA based clocked D-FF with clear

References	Cell count	Ratio	Design area (μm^2)	Ratio	Latency (in clock zones)
Proposed	27	1.00	0.03	1	2
Purkayastha *et al.* (2018)	48	1.78	0.05	1.67	3
Sabbaghi-Nadooshan and Kianpour (2014)	52	1.92	0.07	2.33	6

Table 7: Comparison of various PIPO SRs using QCA clocked D-FF with clear

References	Cell count	Ratio	Design area (μm^2)	Ratio	Latency (in clock zones)
Proposed	206	1.00	0.18	1.00	3
Purkayastha *et al.* (2018)	236	1.14	0.26	1.4 4	314

CONCLUSION

In this study the design methodology and the simulation results for proposed design of QCA based D-FF with and without clear signal and the implementation of various SRs using proposed designs have been discussed. The proposed designs are efficient in terms of area, delay and cell count. Bi-stable vector engine of the of QCA designer tool has been used to carry out the simulations of the proposed designs. The exclusive feature of modularity property associated with the proposed QCA based D-FFs and SRs can be extended to any high order design or even may be used as fundamental building block of a general purpose nano computers/processors and in computer networks. The proposed designs will therefore, prove note worthy in designing complex sequential circuits.

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