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Design, Optimization and Simulation of III-Nitride Power Heterostructure Field Effect Transistor

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Abstract: An enhanced design for a GaN/AlGaN HFET is proposed in this study, the proposed design is the multi-layered metal stack design of a HFET using the metals and thicknesses of Ti (250Å)-Al (750Å)-Ti (100Å)-Al (750Å)-Ti (100Å)-Au (250Å). This novel design has been proposed before and is an enhancement of the traditional Ti-Al-Ti-Au. The aim of the prosed design was to obtain better ohmic contact performance with the Ti-Al and multi-layering being the difference between the two. The two HFETs are expected to perform differently with the proposed design showing better ohmic metalization, consistent with past results and which have been proven using MATLAB simulation of its performance. The Ti-Al multi-layer metal stack returned a resistance value of 3.23 Ωmm while the traditional model had values of 3.40 Ωmm. The proposed Ti-Al multi-layer model also had better performance in terms of current densities with a value of 0.12 Amm^{-1} compared to the traditional design that had 0.08 Amm^{-1}. Al mole fraction was observed to have a direct effect on leakage performance, leakage being an important performance factor. The MATLAB results showed convergence, falling within the 1×10^{-10} and 1×10^{-6}. The results were also comparable to those from past research.

Key words: Field Effect Transistors (FET), ohmic contacts, metal stack, MATLAB, convergence

INTRODUCTION

The field effect in Physics, refers to the modulation of a material's electrical conductivity by applying an external electric filed. For metals, due to the large electron density of the electrons that respond to the applied field, the penetration of the external applied electrical filed is so small that it can only reach a short distance into a material. To overcome this problem, semi-conductors with lower electron densities that can also have holes are instead used; these semi-conductors can respond better to the external applied electric field, resulting in greater material penetration by the field. The semi-conductor's conductivity is altered by the electric filed penetration close to its surface, a phenomenon termed 'field effect' which is what underlies the operation of field effect transistors. Field Effect Transistors (FET) are devices that make use of an electric field to control current flow when aa voltage is applied to the gate terminal, altering conductivity between the source and drain terminals in a single-carrier type of operation (Miao *et al*., 2015). FETs have drain, source and gate terminals, roughly corresponding to the collector, emitter and base in bi-polar junction transistors. There are various types of FETs such as the MOSFET, FREDFET and HFET, the latter of which is the type under discussion in this study (heterostructure FET) which is made by utilizing band-gap engineering in tertiary semiconductors (Jain *et al*., 2013). To achieve higher and better performance, wide band-gap materials are preferred because the higher energy gap implied enables the devices to operate at higher temperatures: as temperatures increase, the band-gaps generally shrink; adversely affecting operations and this is a problem with the usual semiconductors. One group of wide band-gap semiconductor materials are the III-Nitride family (Al, In, Ga) N that have excellent wide band-gap properties, making them suitable for modern applications in opto-electronics and electronics (Ferreyra *et al*., 2017). The focus of this study is the III-Nitride power heterostructure field effect transistor and their design, optimization as well as simulation.

GaN/AlGAN Hetero-junction Filed Effect Transistors (HFETs) are a new generation of high frequency and high power semiconductors that came into the limelight in 1993 and have been improved continuously in their design ever, since, outperforming most other technologies applied in semiconductors. The III-Nitride HFETs have generated high maximum fT (gain cut off frequencies) of 163 GHz and fmax (maximum gain cutoff frequencies) of 230 GHz at 2 Amm^{-1} current densities, making them (GaN/AlGAN HFETs) ideal for power conversions and amplifying power making them ideal in applications such as high power inverters and high performing radars (Mahajan *et al*., 2014).

MATERIALS AND METHODS

The material system of III-Nitrides (GaN/AlGaN HFETs): The superior performance achieved by the GaN/AlGaN HFETs is due to the superb III-Nitride material system qualities including excellent electron mobility, thermal conductivity, electron saturation velocity and breakdown field. The III-Nitride HFETs are precisely referred to as GaN/ Al_xGa_{1-x} HFETs where, x is representative of the mole fraction of Al and helps make the III-Nitrides superior in performance. Adjusting the mole function of Al gives engineers an opportunity to make further improvements to the III-Nitride HFETs to improve their performance based on the intended application. This can, for instance, allow for more appropriate matching level of AlGaN lattice to a growth substrate, helping reduce strain. This capability results in effects on the qualities of the device such as its gate leakage, contact resistance and just about all other characteristics of devices.

Theory behind GaN/AlGaN HFETs: In its basic form, GaN/AlGaN HFETs are made up of a substrate, normally a sapphire, a Metal Organic Chemical Deposited Vapor (MOCVD) or MBE (Molecular Beam Epitaxy) grown GaN layer, Si/SiC and an $Al_xGa_{1-x}N$ barrier layer grown similarly as the MBE with ohmic drain contacts and source as well as a Schottky gate defined over a mesa, selectively etched onto the heterostructure. The band diagram of a basic GaN/AlGaN HFET (Fig. 1), when examined, illustrates the benefits of having a heterostructure. The band diagram (Fig. 2) shows that quantum well that is nearly triangular is formed at the hetero-interface between the GaN channel and the AlGaN barrier. This results in an ensemble of free electrons that create a two Dimensional Electron Gas (2DEG). The 2DEG creates a path of conduction along the HFET channel from the source to the drain; the 2DEG form without applied gate bias, unlike the case in inversion MOSFETs. To deplete the channel, there must be a negative bias applied between the GaN channel layer and the gate as such the Gan/AlGaN HFET is ‘normally on’ depletion mode device (Mahajan *et al*., 2014). The threshold HFET voltage can be shifted using techniques such as implanting a fluoride ion into the AlGaN layer to create ‘enhancement mode’ devices that require positive-gate channel bias to maintain a conductive path between the drain and source contacts. The ingenuity of the Gan/AlGaN HFET design lies in the fact that both the AlGaN and GaN are polar materials and so, the combination of crystal structures of certain Gan and AlGaN orientations create both peizoelectric PPE and spontaneous P_{SP} polarization discontinuity at the hetero-interface. Engineering the rowth of the GaN and AlGaN, the crystal orientations in the electric fields due

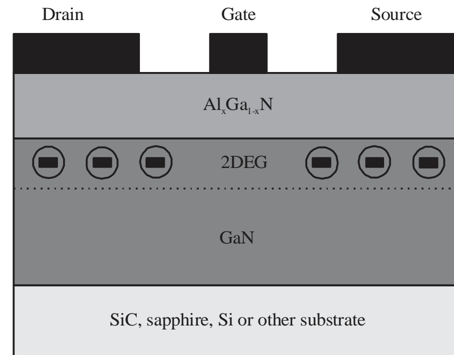

Fig. 1: The schematic diagram of basic HFET structure

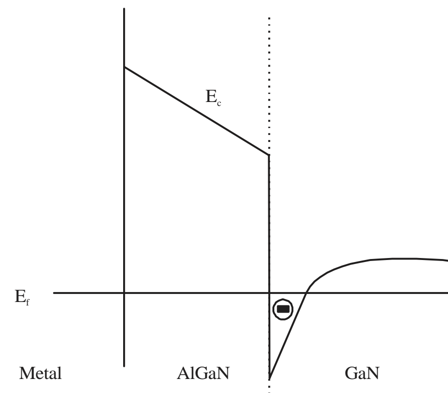

Fig. 2: The band diagram of basic GaN/AlGaN

to peizoelectric and spontaneous polarization act can be ensured to confine electrons at the GaN/AlGaN interface, hence, creating the 2DEG.

Prior work describing the peizoelectric and spontaneous polarizationphenomena to create 2DEGs in GaN/AlGaN HFETs was posited by Ambacher *et al*. The crystalline structure of GaN and AlGaN must first be understood to understand the formation of the 2DEG. Wurtzite binary A-B compounds, as those of the GaN, the Ga and N atoms sequence is reversed for [0001] and [0001^-] directions. The [0001] face is the Ga-face while the [0001^-] is the N-face which are not equivalent (the faces) because their physical and chemical properties are different. This is an important factor because the hetero-junction of one face yields a different 2DEG concentration than the other face. Growing two N-face and one Ga-face wafers, Ambacher *et al*. Established that 2 DEG formed at the GaN/AlGaN interface in the case of Ga-face GaN but in the case of N-face GaN, a 2DEG was formed by the structures at the AlGaN/GaN interface. This is because of different polarization directions in the N-face and Ga-face GaN. The sum of the spontaneous P_{PE} and P_{SP} polarization is total macroscopic polarization P. The net effect of the polarizations, described by σ, the

polarization charge sheet density is useful in the GaN and AlGaN net effect descriptions. The σ is defined as:

$$\sigma = P\,(top)\text{-}P\,(bottom)$$

$$\sigma = [P_{PE}\,(top)+ P_{SP}\,(top)]+[P_{PE}\,(bottom)+P_{SP}\,(bottom)]$$

To achieve 2DEG at the interface, the σ value has to be positive. In designing the GaN/AlGaN HFETs, the layers play a role in design and performance in relation to different scenarios of tensile strained, relaxed and compressively strained for N-face and Ga-face AlGaN depending on whether σ is positive or negative. When thick layers are used, they tend to relax to their freestanding-lattice constant while thin layers, on the other hand have a tendency to adapt to a strain, whether the strain is compressive or tensile and based on the layer upon which they are grown on, assuming the layer is thick. Despite being promising technologies with excellent performance, III-Nitrides are ethnologies that are relatively new and pose certain problems and challenges including the need to work out several technologies before they can be adopted and commercialized on a large scale. The problems and challenges include difficulty growing high quality GaN/AlGaN films using MOCVD and MBE, lack of lattice-matched substrates, difficulty forming Ohmic contacts of high quality and difficulty fabricating devices for enhancement modes. Reliability issues are also a concern, especially, gate lag, current collapse, strain relaxation and gate leakage.

Design of III-Nitride HFETS

Creating ohmic contacts to GaN/AlGaN 2DGES: The capability for creating low resistance ohmic contacts is crucial for any technology for fabricating semiconductors since good ohmic contacts play crucial roles. Resistive heating, for instance is reduced by reduced contact resistance, allowing for high saturation currents as and high trans-conductance as well as reduced knee voltage. The ohmic contact structure also affects the source and drain contacts surface morphology; the surface roughness of the contact is an important aspect of surface morphology. A rough contact makes probing difficult when the contact resistance is being measured. During lateral metal diffusion during high temperature annealing processes, the surface morphology also plays an important role.

Measuring the ohmic contact: Transfer Length Methods (TLM) are suitable for ohmic contact measurement because they allow contact resistance, R_C, to be characterized, along with the contact resistivity p_c and the sheet resistance Rsh.

Theory of ohmic contacts to GaN/AlGaN: For GaN/AlGaN HFETs, there are challenges to forming ohmic contacts, unlike in conventional silicone dominant technologies for semiconductors. The AlGaN layer is the effective barrier to carrier transport because of its wide band-gap, thus an effective ohmic contact has to enhance electrons tunneling through the layer from the drain/ source contact to the 2DEG. Normally, the Schottky and ohmic metalizations to III-Nitrides are achieved by e-beam evaporation of a stack of different multi-layered metals. For ohmic contacts, the ohmic layer normally follows the Ti-Al-metal-Au pattern with the top Au layer used for providing a smooth surface. The third layer of metal, normally Ni or Ti serves to prevent Al and Au combining, since, $AlAu_y$ compounds exhibit high resistivity. The first two Ti and Al layers serve to form and combine compounds with work functions allowing for the formation of ohmic contacts to AlGaN. The composition of metal stacks and the annealing temperatures have an impact on both the surface morphologies and contact resistance of the ohmic contacts.

Design: Khan *et al*. developed the first GaN/AlGaN HFET in 1993 where Ti/Au ohmic contacts of 25A/1500 A were deposited and temperatures of 250°C used for anneaing for 60 sec. The ohmic metalization method is important in the design abd fabrication of GaN/AlGaN HFETs. The proposed design is the Ti-Al multi-layered ohmic structure in which the metal stack is made up of Ti-Al-Ti-Al-Ti-Au. The meta stack should have a thickness of 250-750-110-750-100-250 A and the model is based on one produced by Pang and Kim (2015), similar to the metal stack model proposed by Gong *et al*. The thicknesses for the metals used in the stack are based based on the rationale that Ti (250A)-Al (1500A)-Ti (100A)-Au (250A) metal stack would result in very good ohmic contacts. Keeping the Al content the same at 1500A and leaving the thickness of the Ti barrier layer at 100A would result in the relations remaining unchanged as in the conventional structure with the additional benefit of the extra Al-Ti layers that (Pang and Kim, 2015) hypothesized. The difference in process flow between the ohmic contact structures happens at the source-drain deposition stages.

The process flow in fabricating the III-Nitride HFET based on the described design follows fur stages of mesa isolation, source/ drain deposition, gate deposition and pad deposition with every stage corresponding to its unique photo lithography step. The proposed design should have a total thickness of 50 μm. However, the design is such that sources 1 and 2 are not tied together meaning that the proposed design results in two, rather than one, complete transistors with the gate voltage being the same for both the transistors. Tying the source pads

together, the resultant device should handle twice the voltage, meaning that it is effectively a 100 μm gate width device. This design layout also has the benefit of ensuring the device still works because of a second gate finger being correctly aligned should one gate finger be misaligned. The design and the proposed fur stage fabrication process should result in a device with wide gates to provide better angular gate alignment. The III-Nitride HFET design ensures there are improved ohmic contacts to the GaN/AlGaN HFETs.

RESULTS AND DISCUSSION

Optimization: The performance of the GaN/AlGaN HFETs is closely tied to the manufacturing process; the choice of the materials used and their arrangement (the metal stack) is the first step towards achieving optimization by maximizing on individual materials performance when arranged in a stack. GaN/AlGaN HFETs have shown excellent RF performance that greatly benefits from the high carrier mobility, high charge sheet density as well as high saturation velocity within the channel. However, the GaN/AlGaN HFETs experience physical phenomena that result in their performance being degraded, particularly variations in Cgs with input power drives opposite the classical behavior of FET. At high current levels, trans conductance also gets degraded, resulting in the linearity and the performance frequency of the GaN/AlGaN HFETs. The source of the degradation of Cgs and gm at high drain levels of current is attributed to nonlinear resistance of the sources. The reliability problems associated with the GaN/AlGaN HFETs and gate leakage has been hypothesized to be due to accumulation of electrons tunneling from the gate on the edge of the gate or travel along surface of the AlGaN towards the drain via. a trap to trap hoping mechanism. Using TCAD simulations (Weiwei, 2008) was able to reproduce the measured stress time-dependent and the bias-dependent drain gate current and drain current of the GaN/AlGaN HFETs characteristics with high level accuracy. Weiwei (2008) explains the reliability problems and gate leakage using the surface electron hopping model.

The TCAD simulation gave a value of between 0.25 and 0.35 eV for the extracted value of activation energy of the surface traps. These values are consistent with the measured levels of energy associated with dangling bonds and/or nitrogen vacancies in the device. The proposed optimization solution is to reduce the non-linear source resistance while also improving the linearity and RF performance of the device. Weiwei (2008) proposes the use of approaches such as growing the device within an M-Plane, use of passivation as a way of reducing surface states using lower AlN mole fraction in the AlGaN or methods that control polarization such as using a GaN cap layer on top of the AlGaN layer can be used to mitigate the reliability and large gate leakage problems. In this proposed design, the traditional Ti-Al multi-layered design is used with the aim of eliminating the formation of AlN while retaining a Ti-Al alloy across the barrier layer. The traditional Ti (300Å)-Al (900Å)-Ti (300Å)-Au (600Å) stack is changed and replaced by a novel stack layer arrangement of Ti (300Å)-Al (300Å)-Ti (300Å)-Al (300Å)-Ti (300Å)-Au (600Å) stack. When annealed at 830°C for a duration of 30 sec during manufacture, it a nitrogen ambient environment, it has been shown that for the traditional metal stack [Ti (300Å)-Al (900Å)-Ti (300Å)-Au (600Å)] returned a contact resistance (Rc) of 1.7 Ωmm with a specific contact resistivity value (Pc) of $5.69\times10{-}5$ Ωcm^2. The proposed novel multi-layered design [Ti (300Å)-Al (300Å)-Ti (300Å)-Al (300Å)-Ti (300Å)-Au (600Å)] stack returned a contact resistance value (Rc) of 0.53 Ωmm with a specific contact resistivity value (Pc) of $4.52\times10{-}5$ Ωcm^2 (Karmalkar *et al*., 2003).

Further, Pang and Kim (2015), determining that reducing the second layer Al thickness lowered in-diffusion and this reduced thickness enables Au to fully penetrate the whole metal stack, thereby increasing contact resistance due to a combination of Al and Au and its high work function. The problem of the metal stack thickness is solved by the use of the multi-layered structure that prevents Au full penetration: this also solves the problem of just Al-Au formation by allowing for Ti-Al-Au formation in the stack. The next optimization approach is to have the optimal ratio of Ti to Al for the Ti-Al-Ni-Au metal stacks of the GaN/ Al 0.28 Ga 0.72 N HFET. After studying several ratios of Ti : Al (1:0, 1:1.5, 1:5 and 1:7), (Mahajan *et al*., 2014) found that the optimal Ti:Al ratio was 1:5 which returned a contact resistance (Rc) value of between 0.3 and 0.6 Ωmm at 820°C annealing temperature. In the study, it was also established that no ohmic contact was established when Al was not used. Based on the findings of Mahajan *et al*. (2014) and Pang and Kim (2015), the final proposed metal stack design in terms of thickness is Ti (250Å)-Al (750Å)-Ti (100Å)-Al (750Å)-Ti (100Å)-Au (250Å).

The process flow and workmanship/fabrication processes are the next step in GaN/AlGaN HFETs design optimization for the highest performance. The process flow entails cleaning, photolithography, deep reactive-ion etching and metalization and lift-off. Finally, rapid thermal annealing is done. Cleaning is done by first using a solvent to remove all contaminants followed by a wet etching process to remove native oxide. The next step is photolithography, a process where photoresist spin coating is done, followed by UV (Ultra Violet) exposure and then development. This process results in patterns being designed on materials that are photo sensitive, using light. Deep reactive ion-etching is then done in the mesa

isolation step and once this is done, the device is ready metallization and lift off of metal particles from the surfaces. The final step is rapid thermal heat annealing that is necessary to enable ohmic contacts to be formed.

Based on the works of Mahajan *et al*. (2014) and Pang and Kim (2015), the traditional Ti-Al-Ti-Au ohmic metallization when compared to the proposed multi-layered Ti-Al ohmic metallization should result in better ohmic contacts performance at room temperature and also reduce the lateral diffusion problems associated with the traditional Ti-Al-Ti-Au stack ohmic metallization. As the temperatures increase, the total resistance also increases and this is attributed to increased vibration of the crystal lattice due to higher kinetic energy wrought about by increasing temperatures. As such, increasing temperatures should result in reduced mobility and this requires counterbalancing as it will cause an increase in the total resistance of the HFET. However, based on the proposed design, it is assumed that the GaN/AlGaN proposed metal stack design will have negligible ionized impurities since the GaN channel in the heterojunctions ideally remain closed. studies have shown that contact resistivity has a weak dependence on temperature with contact resistivity rising just slightly as temperature increases (Lu *et al*., 2002). The design should attain a desired drain current consistent with the best published results with actual tests while the sub-threshold swing should return a lower value for the multi-layered compared to the traditional stack design; a lower value is desired because they show that less applied voltage is necessary to achieve a single magnitude order drain current change.

Simulation

Reverse gate leakage simulation: Gate leakage is a very important aspect of the performance of III-Nitride HFETs and are crucial in understanding the effect that different Al mole fractions have on various mechanisms of leakage. To perform the simulatio, traditional simulation platforms that measure transistor performance could not be used for the HFETs and so, MATLAB was employed to do the simulation. This would show how every component of the metal stack and its leakage varied in relation to the gate voltage for different mole fractions of Al. The simulation took into account a physics-model, complete gateleakage governed by the Trap assisted tunneling models and the Poole-Frenckel mechanisms for leakage. The values as measured are shown in Table 1.

The observed values from the simulation are nearly all consistent with those from an earlier experimentation study by Mojaver and Valizadeh (2016). Differences observed such as the conduction band discontinuity indicate that there is an extra mechanism for leakage such as from the sidewall as put forth by Mojaver and Valizadeh (2016) is the cause in the observed discrepancy. However, in real life, as suggested by Mojaver and Valizadeh (2016), the values of the trap density, the highest and lowest trap potential can be altered, in theory, so that, the value of the total simulated leakage closely resemble those found during experimental results. The simulation also showed that with every decrease in the fraction of the Al mole, there is a gradual shift of turning voltage towards gate voltages that are smaller. The results from the simulation are subject to specific assumptions made regarding the trapping process although similar results would be expected for real results. The fraction of Al mole also determines the threshold voltage. Using the MATLAB integral function, the simulation method is verified for convergence and will automatically give an error if there is no convergence if the values fall outside the error tolerances of between 1×10^{-10} and 1×10^{-6}. The simulation showed convergence, however, this does not necessarily imply the design is better; the simulation must also be valid and model the actual physical performance accurately. To ensure validity, the findings from the simulation were compared to those established by Karmalkar *et al*. (2003) and the results showed consistency.

Table 1 : The simulation results

Parameters	Symbols	Value realized
Barrier height	φ b	1.1 V
Electron effective mass	M*	$0.22\times9.1\times10^{-30}$ kg
PF constant	C_{PF}	1×10^{-9} $Am^{-1}V^{-1}$
Richardson constant	A*	2.74×10^{-5} $Am^{-2}K^{-2}$
High frequency relative barrier permitivity	ε s	5.1
Highest trap potential	φ_{t2}	1.15 V
Lowest trap potential	φ_{t1}	0.32V
Band discontinuity conduction	φ_c	0.44V
Trap density	N_t	1×10^{14} cm^{-3}
Barrier height	φ b	1.1 V

CONCLUSION

This study presented a design for III-Nitride HFET based on using GaN/AlGaN to propose a design for an efficient and high performing HFET with a proposed method for fabrication and optimization. HFETs are a desirable type of transistors that have high performance even at high temperatures and this is possible because of having a heterostructure acheved by band-gap engineering of tertiary semiconductors. Higher performance of HFETs is made possible by using materials with wider band-gaps as this implies a higher energy gap that enables the devices to continue operating efficiently at high temperatures. The III-Nitride family (Al, In, Ga) N fit the bill for such a family of HFETs because of excellent wide band-gap properties. GaN/AlGaN HFETs are made up of a substrate, normally a sapphire, a Metal Organic Chemical Deposited Vapor (MOCVD) or MBE

(Molecular Beam Epitaxy) grown GaN layer, Si/SiC and an $Al_xGa_{1-x}N$ barrier layer grown similarly as the MBE with ohmic drain contacts and source as well as a Schottky gate defined over a mesa, selectively etched onto the heterostructure. The proposed multi-layer metal stack for the GaN/AlGaaN HFET is Ti (250Å)-Al (750Å)-Ti (100Å)-Al (750Å)-Ti (100Å)-Au (250Å) which is consistent with proposals from previous designs and will optimize performance. For comparison purposes, the traditional Ti-Al-Ti-Au was also simulated. A simulation was run using MATLAB and the results found closely mirrored those established in actual test results of similar designs. The results showed that varying the mole ratios of Al resulted in changes in the performance of the HFET. Further, the multi-layer HFET design returned better results in terms of contact resistivity and contact resistance values.

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