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Analysis of Low Power Transmitters for Wireless Micro Sensor Networks

M. Sreedevi and P. Jenopaul
Department of Electronics and Communication Engineering, Anna University, Tamil Nadu, India

Abstract: In recent years, distributed wireless micro sensor networks will ensure the reliable and fault tolerant monitoring of wireless transmissions. Such micro sensors are required to operate for years with a small energy source. The working conditions of the sensor network are quite different from those of conventional wireless hand-held devices. These sensors requires communication of short packets in small area, start-up time plays a vital role in energy efficiency of transmission. One of the major challenges in constructing such networks is to maintain long network lifetime with less energy consumption. To achieve this goal, low power research is concentrated in the Wireless Sensor Network (WSN). Here, the high performance, CMOS integrated transmitters (low power CMOS FSK and MPSK modulators) are designed using 0.18 μm CMOS technology. The performance of the proposed transmitters are analyzed and the power consumption is halfly reduced for MPSK and 7 mW for FSK modulator.

Key words: CMOS FSK, CMOS MPSK, WSN, sensors, communicaton, network, India

INTRODUCTION

The demand for low-power wireless communications devices such as cellular phones, Wireless Local Area Networks (WLAN) and Global Positioning Systems (GPS) have been growing rapidly in recent years with higher speeds and increased functionality (Ammer and Rabaey, 2005). Normally, the WSN consists of many distributed and disposable sensor nodes that require a highly integrated, low cost single chip transceiver with high energy efficiency. To consume less power, it should work at a low duty cycle. The energy consumed by a transmitter is due to two sources. One part is due to RF signal generation which is mainly due to modulation and the other part is due to the electronic components needed for frequency synthesis, frequency conversions, power amplifiers, filters and so on (Karl and Willig, 2005). Low voltage, low power transmitters are required to obtain the low power consumption in the sensor nodes. By eliminating the IF circuits used in heterodyne systems, the size and the power consumption of the transmitter is reduced.

In this study, the low power CMOS FSK and BFSK modulators concept are proposed where, the carrier is modulated directly by digital data using static-logic and Pass-transistor Logic (PTL) circuits, respectively (Raja and Sasilatha, 2009; El-Gabaly and Saavedra, 2009). Also, the performance of these modulators is analyzed.

Frequency shift keying: FSK is the digital modulation scheme that conveys data by changing or modulating, the frequency of the reference signal. Any modulation signal uses a finite number of distinct signal to represents a digital data. FSK uses finite number of frequencies each assigned a unique pattern of binary bits. Usually, each frequency encodes each number of bits. Each pattern of bits forms the symbol that is represented by the particular frequency. The demodulator which is designed specifically for the symbol-set used by the modulator, determines the frequency of the received signal and maps it back to the symbol it represents thus, recovering the original data. This requires the receiver to be able to compare the frequency of the received signal to a reference signal. The block diagram of the FSK modulator is shown in Fig. 1.

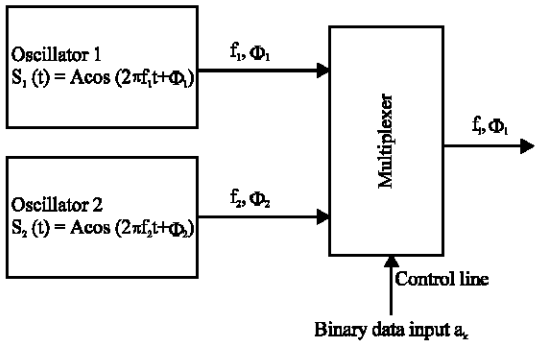

Fig. 1: Block diagram of FSK modulator

Corresponding Author: M. Sreedevi, Department of Electronics and Communication Engineering, Anna University, Tamil Nadu, India

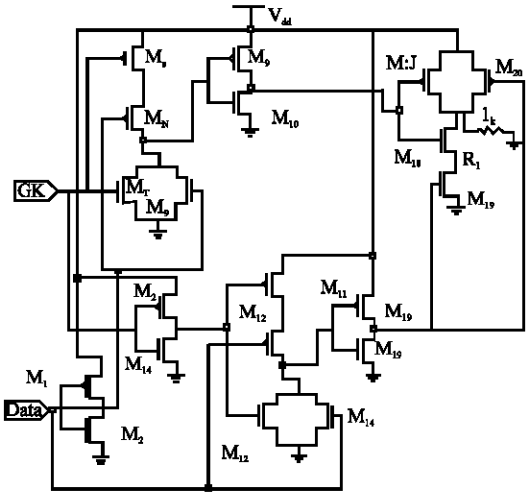

Fig. 2: FSK modulator

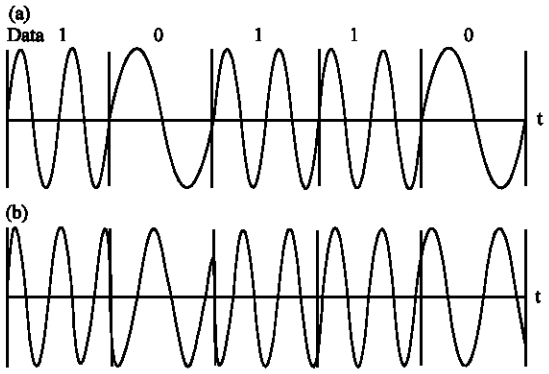

Fig. 3: Output of FSK modulator

FSK modulator: The FSK modulator is designed using static logic circuit design shown in Fig. 2. In FSK, the frequency of a transmitted signal is varied to convey information. The state of each bit is determined according to the state of the preceding bit. If the frequency of the wave does not change, then the signal state stays the same (0 or 1).

If the frequency of the wave changes by 180° then the signal state changes (from 0-1 or 1-0). Here, the normalized energy of 1.8 V is considered for simulation. The FSK modulator is designed and implemented using 0.18 μm CMOS technology. The output of this FSK modulator is shown in Fig. 3. The main advantage of this modulator is that several components in the heterodyne architecture are not needed including the Intermediate Frequency (IF) oscillator if bandpass filter if amplifiers and the RF upconverter. Hence, the power consumption and area of the modulator is reduced. Table 1 shows this researches' performance in comparison with other study.

M-ary Phase Shift Keying (MPSK): M-ary phase shift keying is another form of phase-modulated, constant envelope digital modulation. Accordingly with MPSK modulation, four output phases are possible for a single carrier frequency (El-Gabaly, 2007). The block diagram of MPSK modulator is shown in Fig. 4. MPSK is an M-ary encoding technique where, M = 4, since a MPSK output signal has four possible output phases.

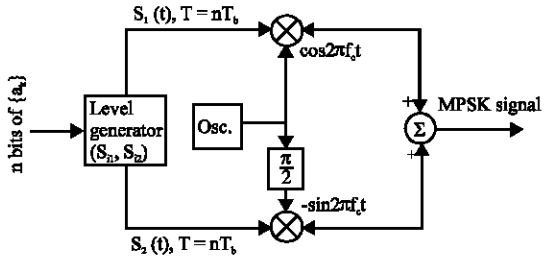

Fig. 4: Block diagram of MPSK modulator

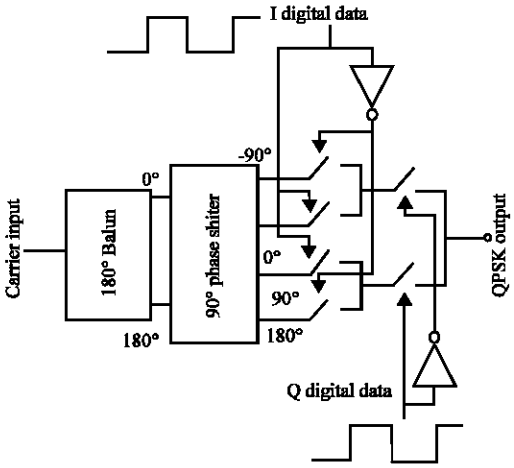

Fig. 5: Block diagram of MPSK modulator

Table 1: Performance of FSK modulator

Technologies	DC power
120 nm CMOS	5 mW at 1.2 V
0.18 μm CMOS	7 mW at 1.8 V

MPSK modulator: The MPSK modulator is designed using 0.18 μm CMOS technology. It consists of a 180° balun, a 90° phase shifter and a switch network. The main advantage of this topology is its relative simplicity compared to other MPSK modulator as it requires only one balun and no summing junction.

In addition, a lower DC power consumption can be attained if a passive 90° phase shifter is used making, it more attractive for portable communication devices that are battery powered. The block diagram of the MPSK modulator is shown in Fig. 5.

The 180° balun 1st splits the input RF carrier into a pair of differential balanced signals. These signals are then fed to the 90° phase shifter which generates differential quadrature signals, yielding all four quadrature

phases of the carrier: 0°, -90°, 90° and 180°. Only one from the four differential quadrature signals is later selected in the switch network according to both In-phase (I) and Quadrature-phase (Q) digital data values which constitute the MPSK symbol (dibit) value. This eliminates the need for a summing junction at the output to generate the MPSK signal.

Balun: The MPSK modulator requires a balun to generate 180° out-of-phase signals from the input carrier as shown in Fig. 5 (El-Gabaly *et al*., 2007; Saavedra and Jackson, 2006). Active balun consists of Common-gate and Common-source FETs (CG-CS) is also used here for the advantages of conversion gain, reduced area. Its performance was optimized, over the S-band frequency range from 2-4 GHz. The circuit schematic of the CG-CS pair active balun is shown in Fig. 6. The outputs V_0 and V_{180} of the balun (Fig. 6) are buffered using FETs in a common-drain (source follower) configuration. This is needed to isolate the outputs from the following 90° phase shifter, presenting larger loading impedance for improved performance including conversion gain. The output of the balun is shown in Fig. 7. To verify the circuit's operation, an S-parameter simulation is run over the S-band frequency range from 2-4 GHz with 50 Ω ports at the input and outputs. The magnitude of the resulting input reflection coefficient S_{11} is shown in Fig. 8. The reflection coefficient magnitude is quite low and <-11dB over the entire bandwidth. The transmission coefficient S_{21} from the input to the in-phase output is shown in Fig. 9. The reflection coefficient S_{22} is shown in Fig. 10.

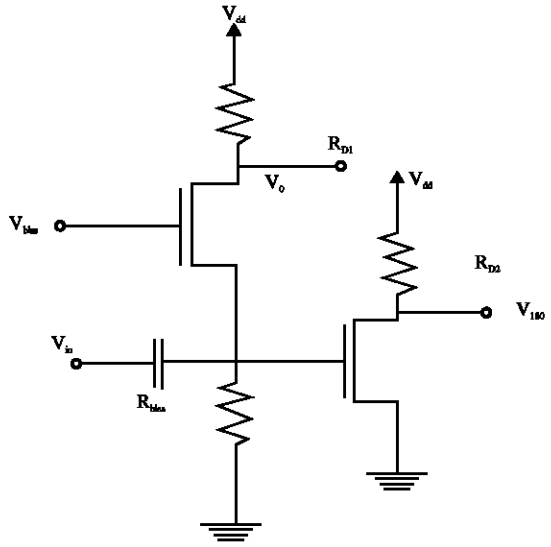

Fig. 6: CG-CS pair active balun

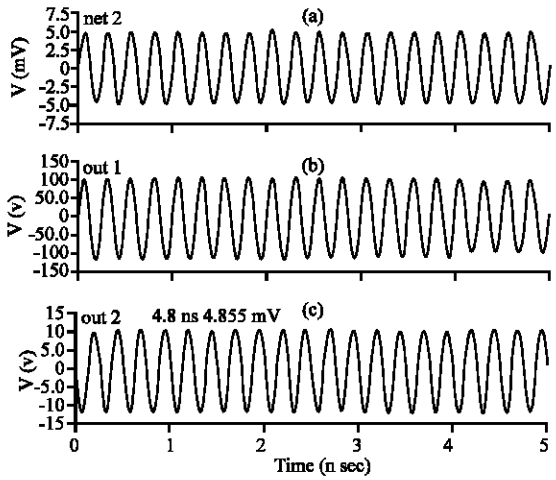

Fig. 7: Output of the balun

Quadrature phase shifter: The Resistor-Capacitor (RC) polyphase network is chosen for generating quadrature carriers due to its simple design and zero DC power consumption. It also offers a lower signal loss compared to using two RC-CR circuits, one for each differential signal. Figure 11 shows the circuit diagram of RC

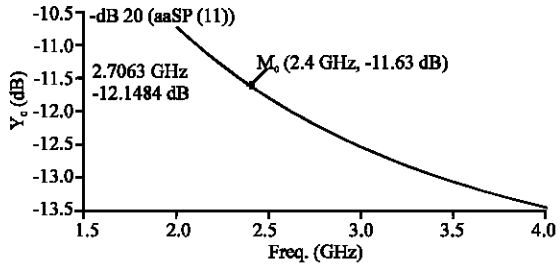

Fig. 8: Input reflection coefficient S_{11}

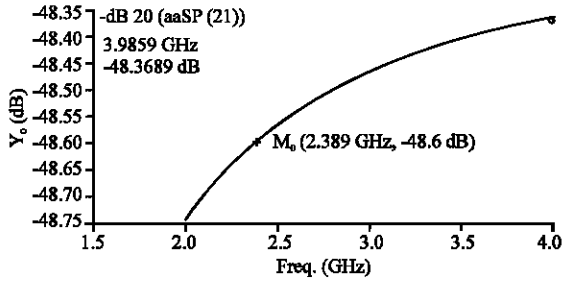

Fig. 9: Transmission coefficient S_{21}

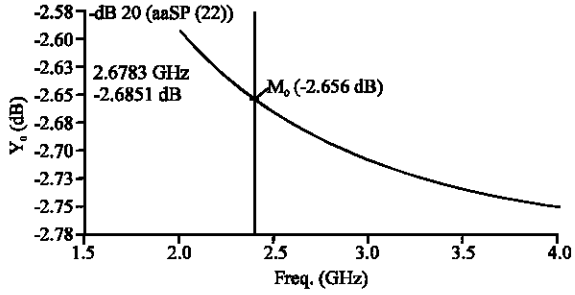

Fig. 10: Reflection coefficient S_{22}

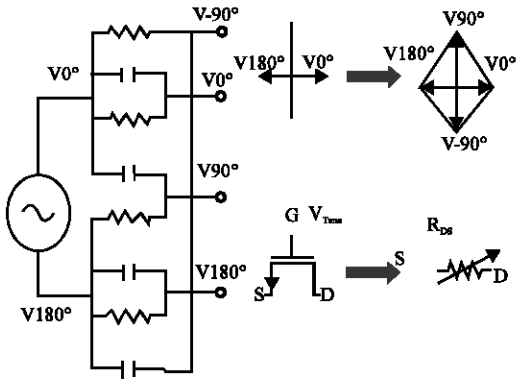

Fig. 11: RC polyphase network and NMOS FET resistor

polyphase network generating differential quadrature phase shifter (Gingell, 1973; Tiiliharju and Halonen, 2003). Resistor implementation is in the form of a NMOS transistor biased in the triode region and its resistance is controlled by a tuning voltage (V_{TUNE} = 0.7 V) applied to the gate (Fig. 11).

The advantage of using voltage-controlled resistors is that the RC polyphase network can now be fine-tuned for the lowest possible phase error. The NMOS transistor operating in the triode region has a channel induced between its drain and source with a drain current-voltage (I_{DS}-V_{DS}) characteristic given by:

$$I_{DS} = \frac{\mu_n CoxW}{1 + V_{DS}/(LEsat)L}\left[(V_{GS} - V_T)V_{DS} - \frac{1}{2}V_{DS}^2\right] \quad (1)$$

Since, the drain-to-source voltage (V_{DS}) is significantly smaller than the gate overdrive voltage (V_{GS}-V_T) and the velocity saturation voltage (LEsat), this equation can be approximated as:

$$I_{DS} \approx \mu_n Cox\frac{W}{L}(V_{GS} - V_T)V_{DS} \quad (2)$$

The equivalent resistance RDS:

$$R_{DS} = \left[\frac{\partial I_{DS}}{\partial V_{DS}}\bigg|Vgs = 0\right]^{-1} \approx \frac{1}{\mu_n Cox\frac{W}{L}(V_{GS} - V_T)} \quad (3)$$

Where, V_{GS} is the applied gate-to-source voltage which is equal to the tuning voltage V_{TUNE} in this case:

$$R_{DS} \approx \frac{1}{\mu_n Cox\frac{W}{L}(V_{TUNE} - V_T)} \quad (4)$$

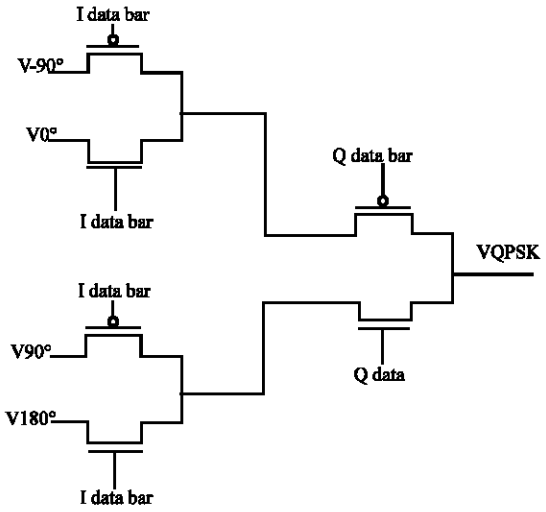

Fig. 12: Switch network

It is now clear that the device behaves as a variable resistor with its resistance (RDS) inversely proportional to the applied tuning voltage (V_{TUNE}) and gate width (W). Therefore, a large voltage and/or gate width can be chosen to yield a relatively low resistance value. The differential quadrature outputs V-90°, V0°, V90° and V180° of the polyphase filter (Fig. 11) are amplified using common-source amplifier.

Switch network: The purpose of the switch network is to pass one signal from the four differential quadrature signals (V-90°, V0°, V90° and V180°) while blocking the other three according to both I and Q data values which constitute the MPSK symbol. In particular, the following digital logic should be realized by the switch network in order to yield the desired MPSK signal constellation (Fig. 12) at the output:

$$V_{QPSK} = \bar{I}\bar{Q}(V - 90°) + I\bar{Q}(V0°) + \bar{I}Q(V90°) + IQ(V180°) \quad (5)$$

Which can be simplified to:

$$V_{QPSK} = \bar{Q}(\bar{I}(V - 90°) + I(V0°)) + Q(I(V90°) + \bar{I}(V180°)) \quad (6)$$

This is showed in Fig. 5 as a set of six complimentary switches in two stages, the 1st four being for the I data stream and the remaining two for the Q data stream. A Pass-transistor Logic (PTL) circuit consisting of six NMOS switches as shown in Fig. 12 is used to implement the needed switch network in (Fig. 5) which has the advantages of small footprint, zero DC power

consumption and high-speed operation. The MPSK signal output V_{MPSK} of the switch network is buffered, using a FET in a common-drain (source follower) configuration (Fig. 12).

This is needed to present large loading impedance for the switch network and the preceding common-source amplifiers to reduce the insertion loss. The buffer is also designed to drive the external 50 Ω load with a low reflection coefficient by ensuring an adequate output impedance match in the buffer given by:

$$Z_{OUT} = \frac{1}{g_m} \| Rs \approx 50\Omega \quad (7)$$

Where:

g_m = Transconductance of the FET

R_s = Source resistance

This can be achieved over a wide bandwidth as opposed to using a narrowband passive network which could also be prohibitively large in this frequency range (2.4 GHz).

MPSK modulator simulation: The simulation is then run over the S-band frequency range from 2-4 GHz. The voltage for the DC sources are swept from 0-1.8 V in a parametric analysis to include all four possible combinations of the I and Q data values (00, 01, 11, 10) with 0 V denoting logic 0 and 1.8 V denoting logic 1. The phase of the resulting transmission coefficient (S_{21}) from the input to the output in each of these four cases is plotted in Fig. 13.

As shown in the Fig. 13 at 2.4 GHz, the phase differences between the outputs are very close to the desired 90°, 180° and 270° (-90°) with a maximum phase error approximately 3°. The magnitude of this transmission coefficient is plotted on Fig. 14 indicating a particularly low amplitude imbalance at the same frequency.

The input (S_{11}) and output (S_{22}) reflection coefficients are also computed as part of these simulations and their magnitudes plots are shown in Fig. 15 and 16. It is clear

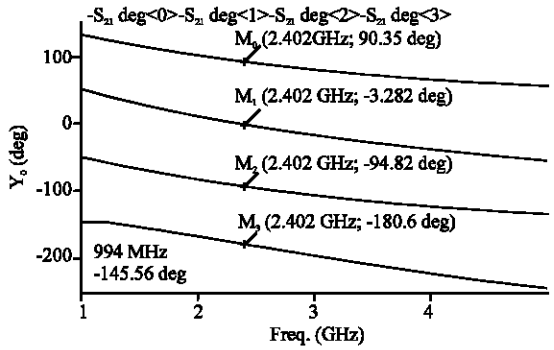

Fig. 13: Transmission coefficient S_{21} (phase)

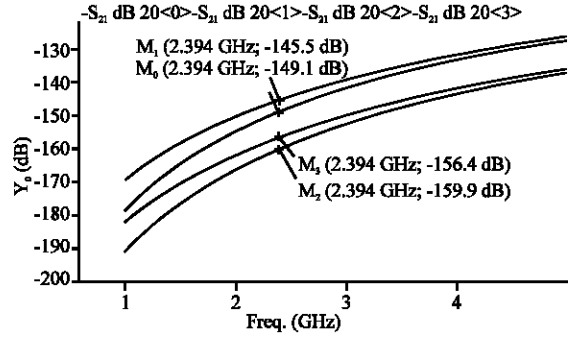

Fig. 14: Transmission coefficient S_{21} (magnitude)

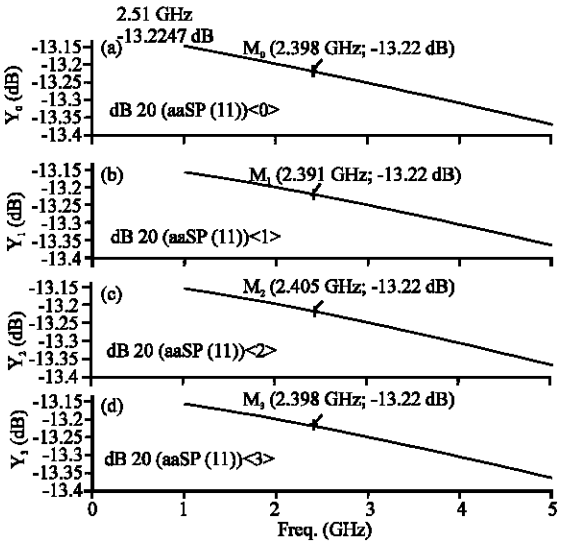

Fig. 15: Input reflection coefficient S_{11}

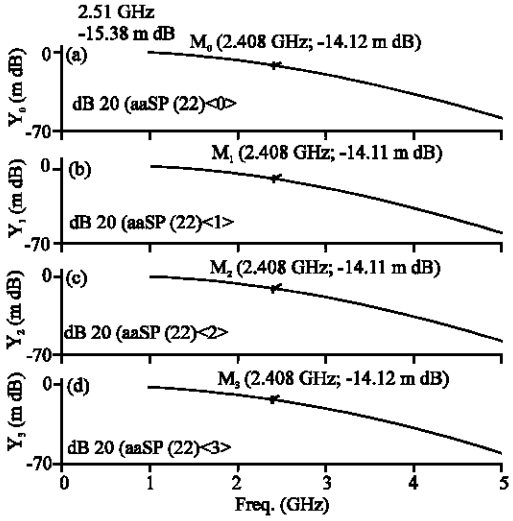

Fig. 16: Output reflection coefficient S_{22}

Table 2: Comparison of the MPSK modulator with other work

Technologies	DC power
0.5 μm GaAs	600 mW at 8 V
0.85 μm GaAs	110 mW at 3.1 V
18 GHz Si-bipolar	68 mW at 2 V
0.35 μm CMOS	188 mW at 3.3 V
0.18 μm CMOS	42 mW at 1.8 V
0.18 μm CMOS	42 mW at 1.8 V
0.18 μm CMOS	19 mW at 1.8 V
0.18 μm CMOS	7.6 mW at 1.8 V

that the reflection coefficients are quite low with magnitudes <-13 dB over the entire bandwidth. The same reflection coefficient is observed for all combinations of I and Q indicating that the switches are sufficiently isolated from the input and output ports. Table 2 shows this work's performance in comparison with five other competitive direct-digital MPSK modulators that were designed for similar applications within the carrier frequency range of 1-4 GHz.

CONCLUSION

The FSK and MPSK modulators concepts are designed where the carrier is modulated directly by the digital data using static-logic and Pass-transistor Logic (PTL) circuits, respectively. A major advantage of this topology is its relative simplicity in terms of size and power consumption compared to most other modulators. The concept was demonstrated through the design of a modulator in 0.18 μm CMOS technology showing very good performance. Here, the normalized energy of 1.8 V is considered for simulation. Power consumed by the FSK modulator is 7 mW and the MPSK modulator is 7.6 mW.

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