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Analysis of Three Level PWM for Two Phase Voltage Source Inverters

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Abstract: Three level PWM scheme offer good harmonic spectrum, more output voltage and less switching losses as compared to two-level PWM strategy. For inverters driving resistive loads, the three-level PWM gives better performance than two-level PWM. But, for inductive loads, due to lack of zero voltage freewheeling path, the load current waveform distorts and contain unwanted low order harmonics. Analysis of inverter performance with three-level PWM driving inductive load has not been investigated so far. In this paper the performance of a two-phase inverter driving a two-phase induction motor is investigated with three-level PWM technique. The performance of the three-level PWM scheme is simulated with a theoretical model using regular sampling strategy. The scheme is experimentally implemented with a TMS320C50 digital signal processor board and a 0.5 HP two-phase induction motor is used as the load of the two-phase inverter. The experimental performance is found in good agreement with the theoretical results and hence validates the theoretical model of three-level PWM.

Key words: Pulse width modulation, two phase inverter, three-level PWM, DSP-TMS320C50

INTRODUCTION

Normally the Pulse Width Modulated (PWM) inverters are used to drive and control ac motors. However, the application of PWM techniques to the two-phase induction motors has been restricted due to the complexity of the drive[1]. But for position control and reversible speed drive applications inverter driven two-phase induction motor is a good choice and these are done by varying voltage and frequency[2]. Researchers exclude phase angle because of computational burden on the processor. However, inclusions of phase angle control would result smooth speed reversal and reduce torsion stress on the drive shaft in addition to the speed control. For smooth variation of voltage, frequency and phase angle by using inverter faster computation of the switching points are required and for this purpose, Digital Signal Processor (DSP) would be the best choice. In this study, DSP kit TMS320C50 is used for computation of the switching points of the PWM patterns.

Two level PWM schemes are widely used for feed forward control of inverters. In this scheme the switches of the inverter in each leg are operated once in each carrier period with a lockout delay. The spectral distribution of two level PWM is good having negligible harmonic components in between the fundamental and the carrier frequency[3]. In three level PWM, only once switch is turned ON and OFF in a carrier cycle. Thus, theoretically the switching loss is less in three level PWM as compared to two level PWM. But, when three level PWM pattern is used to control two phase VSI some unwanted harmonics are introduced into the current waveform of the motor that is driven by the inverter. In this work, the performance of the three level PWM for two phase inverters in normal topology are investigated.

PWM PATTERN GENERATION IN THREE LEVEL

The generation of center justified symmetric regular sampled three-level sinusoidal PWM pattern is illustrated in Fig. 1. Three-level PWM waveform appears across the load switches between +1, 0 and -1 (for example), with the pulses changing polarity by half-cycle. In practice, the inverter dc link voltage scales the amplitude of the PWM waveform. The amplitude of the reference sine wave[4] modulates the widths of the PWM pulses.

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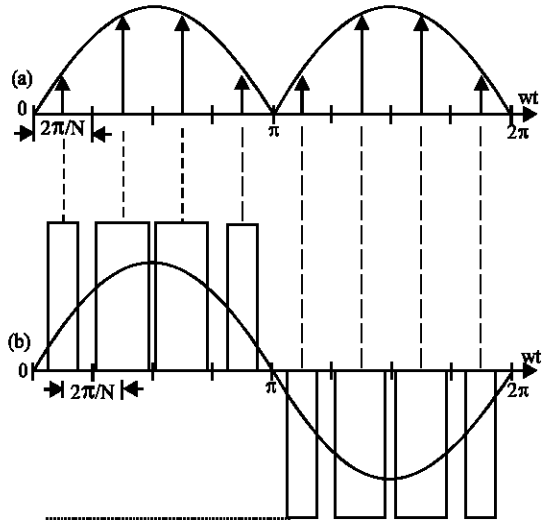

Fig. 1: Generation of three-level regular-sampled pwm, (a) regular-sampled modulating wave, (b) three-level pwm inverter voltage

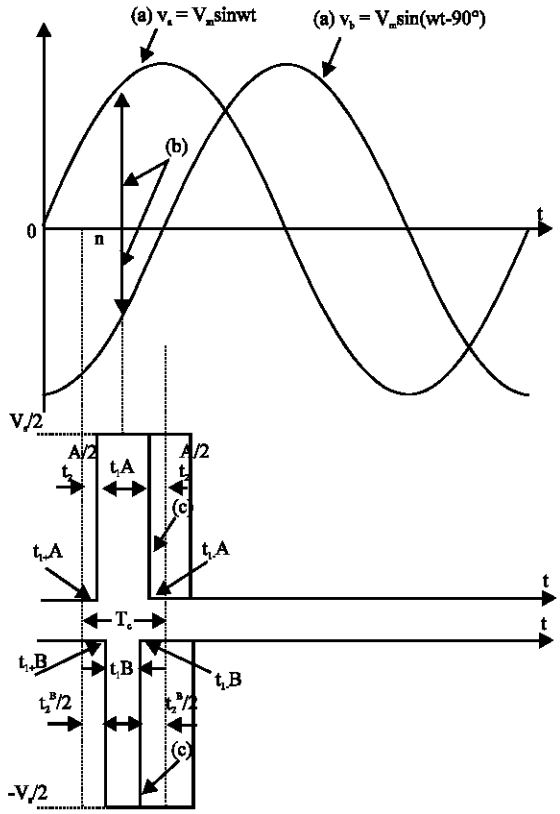

Fig. 2: Pulse width calculation (a) sinusoidal reference signal for both phases a and b (b) sampled signals for both phases (c) pwm output voltages for both phases

SWITCHING POINTS CALCULATIONS IN THREE LEVEL PWM SCHEME

The details of modulation process involved in the generation of symmetric three level regular sampled sinusoidal PWM pattern for two phase voltage source inverter is shown in Fig. 2.

$$A_1(n) + A_2(n) = V(n)T_c \quad (1)$$

A reference fundamental waveform $v = V_m \sin(\omega t)$ is considered where, V_m and ω are the amplitude and modulating frequency of the modulating wave. The voltage waveform is sampled with a sampling time of T_c. The pulse width during each carrier period is determined by making the area under the PWM signal equal to the area under the input-modulating signal, i.e., both the width and the equivalent area under the sinusoidal modulating signal over the sampling period[5]. Thus the sampled voltage V(n) at the nth sampling instant can be obtained by adding the areas $A_1(n)$ and $A_2(n)$ of the three-level PWM as shown in Fig. 2.

The fundamental voltage waveform can be represented in discrete time domain as $V(n) = V_m \sin(n\omega T_c)$. Hence, if the duration of the positive pulse and zero voltage of the three level PWM pulses are t_1 and t_2, respectively then Eq. 1 can be written as

$$V_s.t_1 - 0.t_2 = V_m T_c \sin(n\omega T_c)$$

$$\text{or, } t_1 = \frac{V_m}{V_s} T_c \sin(n\omega T_c)$$

$$\text{or, } t_1 = MT_c \sin(n\omega T_c)$$

$$\text{where, } M = \frac{V_m}{V_s} \text{ is called modulation index.}$$

For a two-phase voltage source inverter with the configuration as shown in Fig. 3 Eq. 2 can be used directly to determine the switching points for phase A. In three level PWM, only one switch is turned ON or OFF in a carrier cycle. The upper switch of any phase leg conducts the load current during positive half cycle of the fundamental period and the lower switch conducts during negative half cycle. For phase B, the switching points would be the same but shifted by 90°. The positive pulse widths for the two phases at the nth sampling instant will be as follows

$$t_1^A = T_c M \sin(n\omega T_c) \quad (3a)$$

$$t_1^B = T_c M \sin\left(n\omega T_c - \frac{\pi}{2}\right) \quad (3b)$$

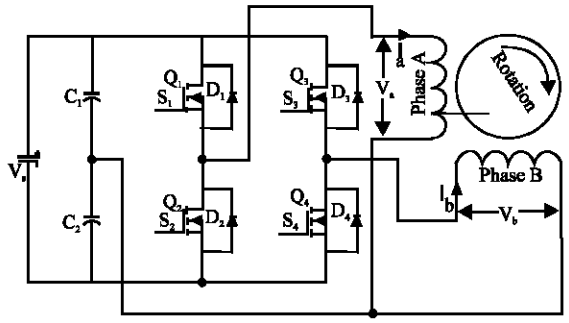

Fig. 3: Two phase half bridge voltage source inverter for two phase induction motor

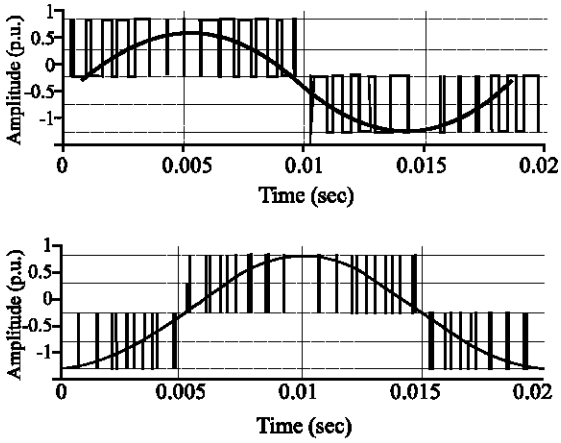

Fig. 4: MATLAB simulation of PWM patterns and phase voltages for both phase A and B

The switching points for the leading and trailing edges of the pulses of both phases A and B are determined by the following equations respectively from Fig. 2.

$$t_{1+}^{A} = nT_c - \frac{t_1^{A}}{2} \quad (4a)$$

$$t_{1-}^{A} = nT_c + \frac{t_1^{A}}{2} \quad (4b)$$

$$t_{1+}^{B} = nT_c - \frac{t_1^{B}}{2} \quad (5a)$$

$$t_{1-}^{B} = nT_c + \frac{t_1^{B}}{2} \quad (5b)$$

For the two phase voltage source inverter in normal topology as shown in Fig. 3, Eq. 3a, b represents the conduction times of Q_1 and Q_3 switches, respectively. Transistors Q_2 and Q_4 conduct in a complementary fashion with Q_1 and Q_3 respectively. In practice lockout time is incorporated at the switching edges to overcome the probability of dc bus short circuit due to the turn ON of the two switching transistors of a leg simultaneously.

The actual load voltage applied across a phase of the load is different from the switching patterns of the individual phase transistors. For one carrier period T_c, the output voltage for this half-bridge inverter will be $V_s/2$ for duration of t_1 and $-V_s/2$ for duration of t_2.

The theoretical development of these equations is then simulated using MATLAB before going into the practical implementations. For this purpose normal topology of the inverter in Fig. 3 is used. The simulated PWM patterns and its associated sinusoidal voltages for both phase A and B are shown in Fig. 4.

REAL TIME PWM PATTERN GENERATION ALGORITHM

The real time PWM patterns are generated using DSP kit TMS320C50. The programs are written using ANSI C compiler. The following algorithms are used:

- Set the fundamental and carrier frequency (f and f_c) and modulation index (M) and phase modulation index (Z) as $N = \frac{f_c}{f}$ start values. Get as the number of pulses in one fundamental period.
- Initialize j = 0.
- Configure ports A and B of 8255 of the DSP kit as the output ports and port C as the input port.
- Initialize an infinite loop so that the following steps are executed indefinitely until a reset signal is applied.
- Increment j.
- If j = 10 then go to next step 7 else go to step 9.
- Scan port C to check the status of the modulation index switches. If there is any high value then change the corresponding modulation index and then go to step 8, else to step 9 leaving modulation index unchanged.
- Reset the value of j to 0.
- Initialize i = 1.
- Calculate duty cycles for phase A and B.
- Convert these values into appropriate format to get the desired three level PWM patterns.
- Scan port C and wait for the ripple carry signal and when it is high then go to step 13 else stay here.
- Send the calculated duty cycles for phase A and B at port A and B respectively.
- Increment i. If i < N, go to step 10 else go to step 4.

PROPOSED SYSTEM

Figure 5 shows the functional block diagram of the main structure of the proposed system. Its main parts are a half-bridge type inverter Fig. 3, an electronic controller circuit, a hardware interfacing circuit and a Digital Signal

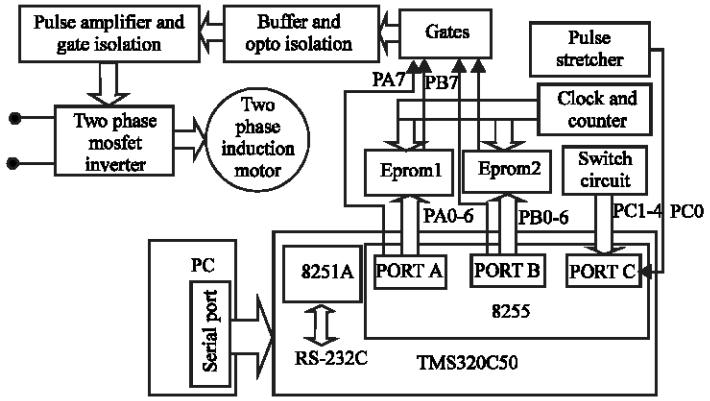

Fig. 5: Block diagram of the digital signal processor controlled PWM phase modulator for two-phase voltage source inverter

Processor (DSP) kit (TMS302C50). Besides, a PC is required to write the main program in ANSI C, to compile it to produce codes (in Hex format) for DSP and to upload these codes in the TMS320C50 module.

As the power is ON the 12 bit binary counter increments its count with the clock signal and read the stored data samples in the two EPROMs of the corresponding addresses for the two phases. The program uploaded in the DSP kit checks the status of the switch circuit to get the proper value of the modulation indexes and use it to calculate the switching points for the two phases of the inverter. As soon as the counter completes scanning all 256 addresses of the two EPROMs and PC0 line of input port C gets the ripple carry signal, DSP sends the calculated switching points through the port A and B to the data bus of the EPROMs. Accordingly required PWM patterns are obtained at the output of the EPROMs. This signal is then fed to the inverter to drive the motor via an electronic controller circuit.

SIMULATION AND EXPERIMENTAL RESULTS

Two phase induction motor is equivalent to a R-L load in steady state conditions. The motor used in this work has effective resistance R = 75 Ω and inductance L = 50 mH per phase. Taking these values for a R-L load, the proposed system is first simulated in MATLAB to get the PWM patterns for two phases, frequency spectrum in PWM pattern and in current waveform of phase A and current waveform of phase A in three-level PWM scheme. These are presented in Fig. 6-7. It is seen that the current waveform is distorted.

Then the implemented real time system is run and photographs of the PWM patterns and current waveforms for three-level PWM scheme are obtained from

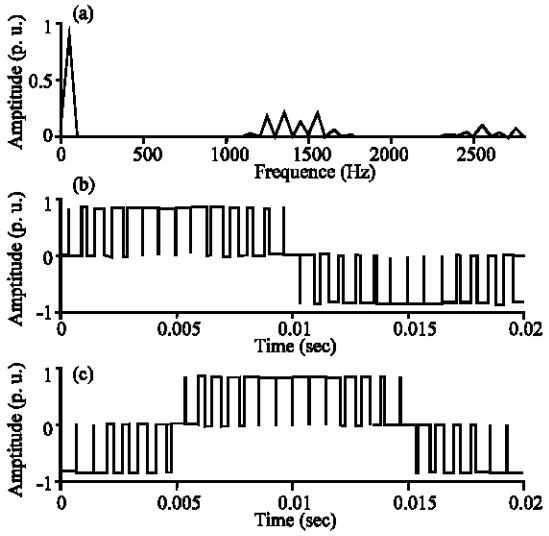

Fig. 6: MATLAB simulation of (a) harmonic spectrum of phase A, (b) PWM pattern of phase A, (c) PWM pattern of phase B with f = 50 Hz, f_c = 1400 Hz and M = 1.0

oscilloscope screen and presented in Fig. 8. Here it is also seen that the current waveform is distorted like the simulation results. Actually in three level PWM both positive and negative voltages as well as zero voltage are given to the inverter input. But positive voltage is being applied in one half cycle in one fundamental period and negative in the next. So, when zero voltage is applied during positive or negative half cycle of the inverter there should be a free wheeling path for the current to flow because of the inductive nature of the load. This path in three level PWM is obtained from negative supply voltage, but there is no reflection of

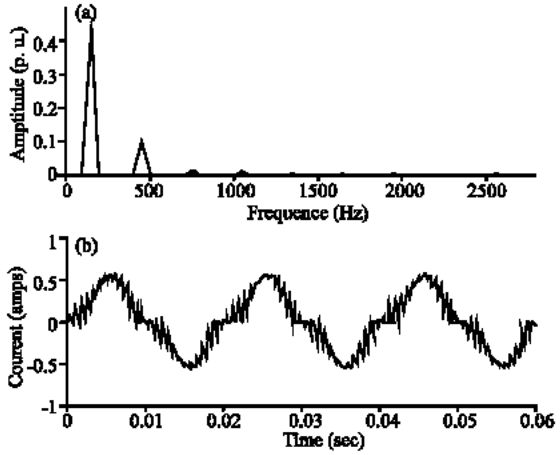

Fig. 7: MATLAB simulation of (a) harmonic spectrum of current for phase A and (b) current waveform for phase A with f = 50 Hz, f_c = 1400 Hz and M = 1.0

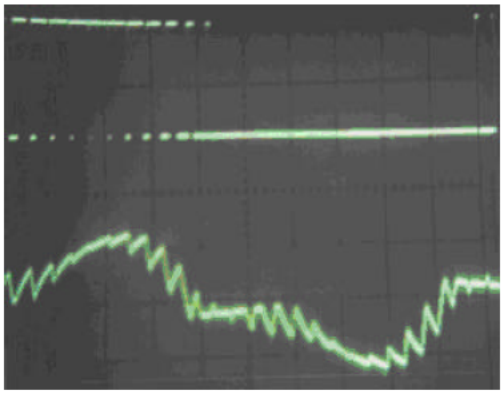

Fig. 8: PWM patterns at the output of the EPROM for Q_1 MOSFET and the phase current waveform of phase A with f = 50 Hz, f_c = 1400 Hz and M = 1.0

this path in the control pattern. That is why, low order harmonics are introduced in the current waveform and degrades the system performance.

CONCLUSION

For the normal topology of voltage source inverters, there is zero voltage free wheeling paths for the current in two level PWM scheme when any switch of a phase leg goes from ON state to OFF state. But in three level PWM, the load current freewheels through the supply voltage due to absence of zero voltage freewheel path. Hence an opposite polarity voltage is imposed across the load during turn-OFF process. The output voltage of any phase leg deteriorates from the control PWM pattern and low order harmonics are introduced. Hence topological change is needed in the inverter if three-level PWM scheme is to implement without harmonic degradation. This topology will be such that the free wheeling operation is done through a zero voltage path.

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