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Direct Digital Frequency Synthesizer Design and Implementation on FPGA

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Abstract: This study presents a design and implementation of a direct digital frequency synthesizer based on Quarter Sine Wave. The RTL level simulation and gate level simulation of a proposed design is done by means of a Quartus-Model-Sim. This design is a digital part. The digital part consists of a Phase Accumulator (PA) and a Look up Table (LUT). The Phase Accumulator is implemented by means of a register along with an adder and feedback loop. LUT is implemented using verilog code. The size of LUT is reducing by storing quarter of sine wave in the ROM. This design was tested with various tuning frequencies and the result shows that the output frequency is directly proportional to the tuning input frequency.

Key words: Frequency, gate level simulation, feedback loop, verilog code, input frequency

INTRODUCTION

Direct Digital Frequency Synthesis (DDFS) is a device that generating a sinusoidal wave. Direct Digital Frequency Synthesis is a heart of many modern communications system such as transmitter, receivers, GPS systems, mobile telephones, radiotelephones, etc. The concentration of this study is on the design, analysis and implementation of DDFS using FPGA. There are two methods to implement the frequency synthesizer. The conventional method utilizes a Phase Locked-Loop (PLL), for high bandwidth frequency synthesizers. The other method is a Direct Digital Frequency Synthesis. DDFS provides many considerable benefits over the PLL approach such as fast settling time, sub-hertz frequency resolution, continuous-phase switching response and low phase noise (Mortezapour and Lee, 1999). Since, the basic element of DDFS is a digital element, the speed and resolution depending on the size of the LUT and phase accumulator. The size of the LUT is a challenges issue. The large size of LUT which is slows down the speed of the DDS and results in higher power consumption. To reduce the size of the LUT, a mechanism of quarter of sine wave is utilized.

MATERIALS AND METHODS

The basic construction of direct digital synthesiser: The basic construction of Direct Digital Synthesizer (DDS) is a Phase Accumulator (PA), Lock up Table (LUT), Digital to Analog Converter (DAC) and Low Pass Filter (LPF).

The role of DDS is to gain an output signal in a shape of sinusoidal wave with a reference frequency. Since, the output of the DDS is in a form of a digital signal, a digital to analogue converter is needed. The DAC output should pass through a Low Pass Filter (LPF) to suppress the images of the output spectrum, repeating at intervals anti-aliasing filter. To obtain an output sinusoidal signal a sequence of input sampling sinusoidal signals is applied to the DAC. The way of alteration the sin wave in time is difficult and digital methods cannot be directly performed. Since, high speed is one of the main requirements for (DDS's) this way improbable to be used.

The most suitable method to form sinusoidal waves is the table method. A coding table (look up table) is most often placed in ROM. A code which is representing the address inputs of ROM is the argument of sin and the output code of ROM is equal to the value of the function for this argument. The argument of sin or phase in contrast to the values of the function varies with time. Forming a linear time-varying sequence of codes is much easier and this method can be implemented via digital devices, called accumulators (Vankka and Halonen, 2001). The accumulator is a registers along with adder which is each clock cycle equal to the old content plus a constant additive as shows in Fig. 1.

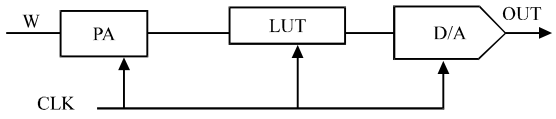

Fig. 1: Direct digital synthesizer based on the accumulator

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The register increases linearly with time and depends on constant addition. When the accumulator is used to generate the code of phase it is called the phase accumulator. The output code of the phase accumulator is the code of the instantaneous phase of the output signal. Constant additive which is added constantly to the phase accumulator is a phase increment per cycle. The quicker the phase varies in time, the greater the frequency of the generated signal is. Therefore, the value of the phase increment is actually a code output frequency. In fact if the phase increase is equal to unity, the conduct of the phase accumulator is no different from the conduct of a binary counter. But if the phase increase is equal to, for example, two then the code phase will change twice as fast. In this case, the DAC codes will come with the same frequency but will not be a neighbor and taken through one counts the sinusoidal function. If the frequency of a generated signal is twice as large, a sampling rate will be unchanged. A phase accumulator is operated with the period of overflow, providing arithmetic modulo 2N. This period of overflow corresponds to the behavior of a sinusoidal with the period of 2π . In other words, the frequency of overflow of the phase accumulator is the frequency of the output signal. This frequency is governed by the equation (Sharma and Upadhyaya, 2010).

$$f_0 = \frac{M \times f_{clk}}{2^n} \quad (1)$$

Where:

F_{out} = Output frequency
F_{clk} = Clock frequency
M = Code rate
N = Bit of phase accumulator

In essence, the clock frequency is divided by a number which is determined by the code frequency and phase accumulator word length. At the same time the frequency step is equal to:

$$D \times f_0 = \frac{M \times f_{clk}}{2^n} \quad (2)$$

Equation 2 means that increase the length of phase accumulator, it decreases the frequency step and there is no specific constraint for instance if the bit accumulator is 32 bits and the clock frequency is 20 MHz, the frequency resolution is in order of 0.004 Hz. This indicates that increase the length of phase accumulator does not require increasing the length of LUT (Hegazi *et al*., 1998). The address may only use the necessary number of significant bits of the phase code. To reduce the amount of ROM, you can use the symmetry properties of the sinusoidal function. In this case, DDS in the ROM contains only 1/4 period. In this case a complex logic of forming the address is required. Thus, in DDS the phase accumulator generates a sequence of code of the instantaneous phase signal that varies linearly (Bellaouar *et al*., 2000). The rate of phase change gives the frequency code. Further, by using ROM, the linear change of phase is converted to a varying sinusoidal which indicates the output signal (Sunderland *et al*., 1984; Nicholas *et al*., 1988). Samples are fed to the Digital to Analog Converter (DAC), therefore the output of the DAC is a sinusoidal signal consisting of steps. It is then filtered by LPF and its output is a sinusoidal wave.

System level simulation: In order to perform, the system level modelling and simulation of a DDS a Quarts-Modelsim is utilized to vision the influx from input part to output part. The model of DDS consists of Phase Accumulator (PA) and a Look up Table (LUT). Figure 2 and 3 show the RTL level schematic of the DDS. Every model is build up in verilog then put together in the top level. Thus, it is possible to modify according one's design requirements. The phase accumulator is implemented via a register along with an adder and a feedback loop. The LUT is implemented using Read Only Memory (ROM). The ROM is decreases by

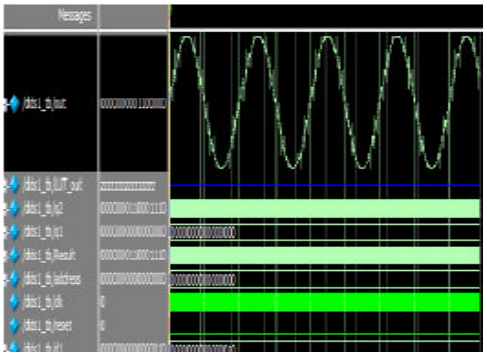

Fig. 2: GLS output for tunning word is equal to 2

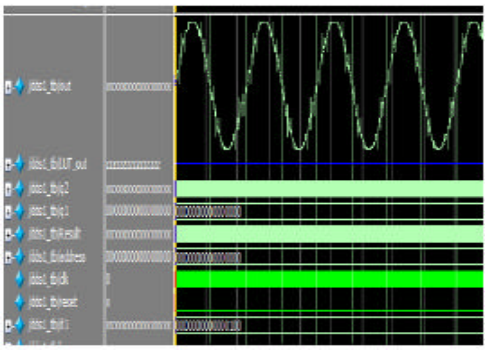

Fig. 3: GLS output for tunning word is equal to 4

stored only quarter period of sine instead of all period of sine wave. As shown in Fig. 3, the model works as follows. The phase register contents are added to the phase accumulator with every clock cycle. The phase accumulator generates the phase value of the output sinusoidal wave. The phase value of the PA provides an address for the LUT. The contains of look up table is a sample value of the sinusoidal wave forms. The look up table output represents one cycle of the sinusoidal waveform. The data was generated by MATLAB. The program calculates the period of sine as follows. When the value of sine reaches one, the quarter period of sine wave, the program will be multiplier the index of sample one by two and decrease the address from this value until the output reaches zero. Then, the program will be decrease index of sample one multiplied by two from the address and the resulted value will be multiplied by mines one until the value reaches mines one. Then, the program will be multiplied the index of value mines one by two and decrease the address from it and the resulted value multiplied by mines one until the value reaches zero. This is one period of sine wave. The program will be repeating the same algorithm. The overflow rate of the phase accumulator depends on the bit size of the phase accumulator and frequency tuning word. The larger the size of the frequency tuning word, the faster the PA overflows. The output frequency of the direct digital synthesizer is directly proportional to the frequency tuning Word (W). Therefore, the larger the frequency tuning word, the faster the PA overflows and the higher the output frequency.

RESULTS AND DISCUSSION

Gate level modelling and simulation: Figure 2 and 3 show the gate level simulation for frequency tuning words 2 and 4, respectively.

Experimental result

Implementation details: The system implementation was conducted on board Altera Cyclone®-II 2C35 FPGA. The usage is shown in Table 1. The clock taken from pattern generator of logic analyzer.

Table 1: Device utilization summary

Logic utilization	Used	Available	Utilization (%)
Total combination function	33,216	244	<1
Dedicated logic registers	33,216	42	<1
Total pins	98	475	21
Total element logic	33,216	258	<1
Total memory bits	0	483,840	0
Embedded multiplier 9-bit element	0	70	0
Total PLLs	0	4	0

Measurement results: The result was saved from the logic analyzer to text file. Then, it is plotted via MATLAB tool. The plotted result shows that the output is smooth sinusoidal with noise and the output frequency proportional to the frequency control word as shown in

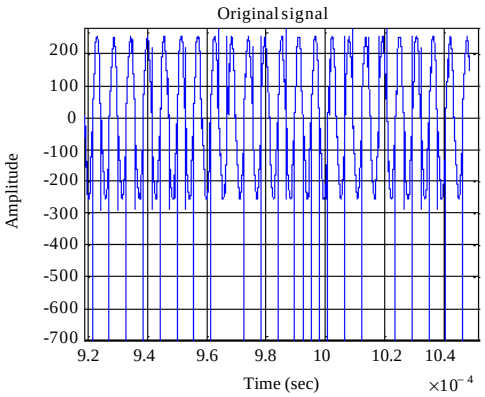

Fig. 4: Measuring output for tunning word is equal to 2

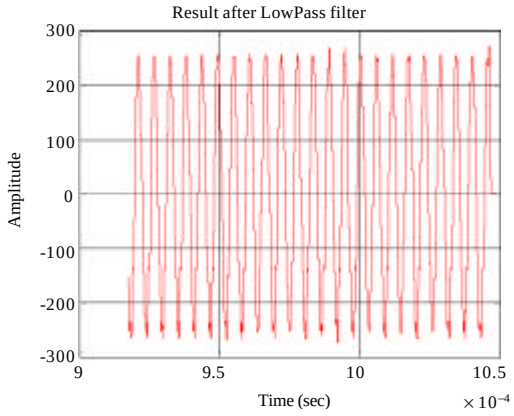

Fig. 5: Measuring output for tunning word is equal to 2 aftre filtration

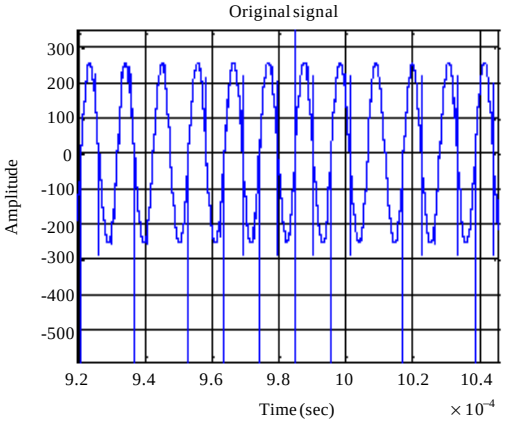

Fig. 6: Measuring output for tunning word is equal to 4

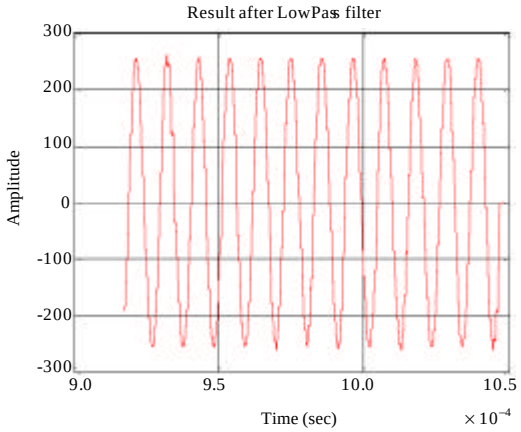

Fig. 7: Measuring output for tunning word is equal to 4 after filtration

figure. The result is improved by low pass filter which was written in MATLAB code. The result after filtration is very smoothing sinusoidal as shown in Fig. 4-7.

CONCLUSION

A design and implementation of a direct digital frequency synthesizer was conducted on FPGA. The DDFS 's digital part includes a Phase Accumulator (PA) and a Look up Table (LUT). The design is created using verilog HDL. The gate level modelling and simulation of a DDFS is implemented using Quarts-Modelsim. A phase accumulator is achieved by a register along with an adder and a feedback loop. The LUT is implemented via Read Only Memory (ROM). The size of the Look up Table (LUT) is decreases via using quarter of sinusoidal. The measuring result shows that the output frequency is directly proportional with the frequency tuning word.

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