Research Journal of Applied Sciences 8 (10-12): 477-485, 2013
ISSN: 1815-932X

Resource Efficient Implementation of Low Power LDPC Based CDMA Architecture

[1]T. Yasodha, [2]I. Jacob Raglend and [3]K. Meena Alias Jeyanthi
[1]Department of Electronics and Communication Engineering,
Christian College of Engineering and Technology, Oddanchatram, Tamilnadu, India
[2]Department of Electrical and Electronics Engineering,
Noorul Islam University, Nagercoil, Tamilnadu, India
[3]Department of Electronics and Communication Engineering,
PSNA College of Engineering and Technology, Dindigul, Tamilnadu, India

Abstract: In this study, LDPC codes based low power multi-user CDMA architecture is proposed. Also, a modified Min-Sum algorithm for LDPC Decoder design is built and used in the proposed architecture. Min-sum iterative decoder has a reduced complexity in terms of architecture-algorithm transformation, compared to other LDPC Decoding algorithms. The architecture is designed for LDPC encoder and the variants of Min-sum decoder. The architecture is synthesized on Xilinx and Synopsys tool targeted to 90 nm device. It is found from the synthesis report of the proposed architecture that it reduces the area and power overhead when compared with the conventional architecture design.

Key words: Coding-spreading trade-off, density evolution, Low-Density Parity-Check (LDPC) codes, turbo multi-user detection, LDPC-coded turbo CDMA System, Additive White Gaussian Noise (AWGN) channel, Min-Sum algorithm

INTRODUCTION

The error correction properties have put on great impact in the research fields. Among the various error correction codes, it is proved that LDPC codes are better and it is closer to the Shannon limit. LDPC codes achieve 0.04 dB of the Shannon's limit. Another advantage is the hardware implementation of LDPC codes being easier with iterative decoding. These codes have an enhanced error correcting capability. The performance of Code Division Multiple Access (CDMA) Systems is mainly determined by coding and the spreading which are the two aspects of signaling. To achieve maximum spectral efficiency, assigning the given bandwidth to coding and spreading should be appropriate. The trade-off problem has been focused on single-user detection. A speculative solution of this problem for multi-user detection is discussed by Verdu and Shamai (1999) and Tseng (2009). It is shown that the same optimum spectral efficiency of the single-user matched filter is achieved by the Minimum Mean Square Error (MMSE) receiver (Verdu and Shamai, 1999). The efficiency gain of the MMSE receiver increases with the single-user matched filter above 2.5 dB. The multi-user detection system almost has the same performance as the single-cell system as far as the coding-spreading trade-off is concerned whereas the Linear MMSE receiver in the multi-cell system offers better capacity compared with the conventional matched filter receiver (Moher, 1998). In this study, researchers solve the coding-spreading trade-off problem of CDMA Systems by applying the turbo multi-user detection with joint decoding.

Unlike the turbo multi-user detectors discussed by Yue *et al*. (2003), the front-end filters are considered to be performed only once before passing the soft or hard outputs to the individual single-user channel decoders. The channel decoders are considered to attain the residual capacities of the resulting single-user channels. For systems employing turbo multi-user detection, ideal decoding hypothesis will not ease a coding-spreading study in the decoding process (Boutros and Caire, 2002). It is understood that the users employ capacity-attaining Low-Density Parity-Check (LDPC) codes. Maximum spectral efficiency is attained in the turbo decoding process by hunting the tangent point between the extrinsic information Signal-to-Noise Ratio (SNR) evolution curves of the Soft-Input Soft-Output (SISO) detectors and that of the LDPC decoders when increasing the system load using density evolution technique. The results of the LDPC codes will be based on a ideal joint decoding since they provide near-capacity performance.

Corresponding Author: T. Yasodha, Department of Electronics and Communication Engineering,
Christian College of Engineering and Technology, Oddanchatram, Tamilnadu, India

The spreading sequences play an important role in the performance of CDMA Systems (Veeravalli and Mantravadi, 2002). It is necessary to acquire the basic knowledge of CDMA System design independent of its structure to attain the benefits of multi-user detection. Therefore, one should perform best system-analysis with number of users and the processing gain increased till infinity with their ratio remains constant. The turbo multi-user detection and its asymptotic performance were analyzed by Shamai and Verdu (2001).

The coding-spreading trade-off for turbo multi-user detection is analyzed for both single-cell and multi-cell systems. The FPGA family is analyzed using minsum algorithm by Tolouei and Banihashemi (2008). The Wave- Pipelined System is finally compared with the data of the above studied FPGA family.

LITERATURE REVIEW

Torrieri *et al.* (2008) describe direct-sequence Code Division Multiple Access (CDMA) Systems with M-ary modulation where channel estimation, coherent demodulation and decoding are iteratively evolved without using any training or pilot symbols. For CDMA systems with low-density parity-check codes, An Expectation-Maximization Channel-Estimation algorithm for the fading amplitude and interference-plus-noise Power Spectral Density (PSD) are proposed. The system design is simplified with the elimination of pilot symbols and improves either information throughput or spectral efficiency by way of increasing the information-symbol duration. The fading amplitude and noise PSD are initially estimated and the subsequent values of these parameters are iteratively updated from the channel decoder. These updated estimates are then combined with the received symbols and iteratively passed to the decoder. Experimental results show that the bit error rates of this system are slightly higher than other comparable systems and throughput of the system is found to be larger.

The analysis and design of Low-Density Parity-Check (LDPC) codes for turbo multi-user detection in multipath Code Division Multiple Access (CDMA) channel is discussed by Wang *et al.* (2005). Wang *et al.* (2005) have developed a technique for computing the probability density function (pdf) of the extrinsic messages at the output of the Soft-Input Soft-Output (SISO) multi-user detectors as a function of the pdf of input extrinsic messages. For the case of Additive White Gaussian Noise (AWGN) channels, the extrinsic messages can be well approximated as symmetric Gaussian distributed. In the case of asynchronous multi-path fading channels, the extrinsic messages are approximated by a mixture of symmetric Gaussian distributions. Simulation results are significant with the computed thresholds and irregular LDPC codes designed outperform the regular ones. Different methods for LDPC codes are used by the researchers in a slowly Rayleigh fading frequency-selective channel to evaluate the performance of the coded system (Behroozi *et al.*, 2003). The results are then compared with those of the super-orthogonal coded system. The observation made from the simulation depicts that the LDPC coded scheme drastically outperforms the uncoded and the super-orthogonal coded scheme.

A new method for designing the spreading permutations based on space time block code matrices for MIMO-CDMA Systems has been proposed (Yasodha and Raglend, 2012). The study focuses on wireless systems using Hybrid Automatic Repeat Request (HARQ) with emphasis on the multiple-input multiple-output paradigm. MIMO-HARQ offers new opportunities because of the additional degrees of freedom introduced by the multiple antennas at the transmitter and receiver. The architecture of MIMO transceivers that are based on bit-interleaved coded modulation and HARQ scheme is described. Modified Space Shift Keying (SSK) is used as the modulation format.

This study also analyzes the detection of multi-user signals in HARQ MIMO-CDMA Systems. The new designs improve the Bit Error Rate (BER) compared to MIMO-CDMA Systems that use spreading permutations based on T-designs. This BER improvement comes without any increase in system complexity.

Proposed research: The proposed system architecture consists of transmitter and receiver blocks as shown in Fig. 1. The data input is given to LDPC encoder and the encoded message is transmitted via the channel through CDMA transmitter. The reverse process of transmission takes place at the receiver side and LDPC decoder is used for error correction here. The minsum algorithm is used in the LDPC decoder for reducing the area and power overhead.

Min-sum algorithm: Min-sum (MS) decoding algorithm is an approximation of the iterative Sum-Product (SP) algorithm discussed by Papaharalabos *et al.* (2007). Even though the performance of MS is generally a few tenths

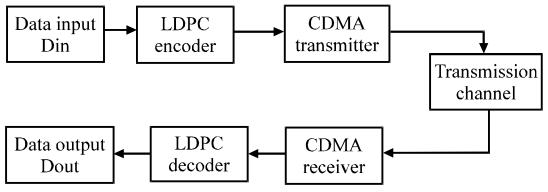

Fig. 1: Proposed system architecture

of a dB lower than that of SP decoding, it is most robust to quantization errors when implemented with fixed-point operations. Moreover, Min-sum is of reduced complexity and the knowledge of noise power is unnecessary in this case. In MS, the hardware for the check node function is simple when compared to the SP algorithm.

In MS decoding, similar to SP algorithm, the extrinsic messages are passed between check and variable nodes in the form of Log Likelihood Ratios (LLRs). Let $Z_{mn}^{(i)}$ represents the LLR value for bit n sent from variable node v_n to the check node c_m in the ith iteration and similarly $\varepsilon_{mn}^{(i)}$ represents the LLR value for bit n, sent from check node c_m to variable node v_n in the ith iteration. Suppose $W = \{w_1, w_2, ..., w_N\} \in C$ and $Y = \{y_1, y_2, ..., y_N\}$ are the transmitted codeword and the received sequence, respectively then the MS Decoding algorithm works as follows:

- Initialize the iteration counter (i) to 1 and let I_M be the maximum number of iterations allowed
- Initialize $Z_{mn}^{(i)}$ to the aposterior LLR:

$$\lambda_n = \frac{\log(P(v_n:0|y_n)}{P(v_n = 1|y_n))} \quad \text{for } 1 \le n \le N, m \in M(n)$$

- Update the check nodes, i.e., for $1 \le m \le M$, $n \in N(m)$ calculates:

$$\varepsilon_{mn}^{(i)} = \min_{n' \in N(m)\backslash n} \left|Z_{mn'}^{(i)}\right| \prod_{n' \in N(m)\backslash n} \text{sgn}(Z_{mn'}^{(i)}) \quad (1)$$

- Update the variable nodes for $1 \le n \le N$, $m \in M(n)$, calculates:

$$Z_{mn}^{(i)} = \sum_{m' \in M(n)\backslash m} \varepsilon_{m'n}^{(i)} \quad (2)$$

- Apply a hard decision, i.e., compute $\hat{W} = \{\hat{w}_1, \hat{w}_2, ..., \hat{w}_N\}$ where element $\hat{w}_n$ is calculated as:

$$\hat{W}_n = \begin{cases} 0 & \text{if } \lambda_n + \sum_{m \in M(n)} \varepsilon_{mn}^{(i)} \ge 0 \\ 1 & \text{otherwise} \end{cases} \quad (3)$$

If $\hat{W}H^T = 0$ (or) $i = I_M$ stop the decoding and go to step 6, otherwise set i = i+1 and go to step 3

- Output $\hat{W}^{(i)}$ as the decoder output

Min-sum with unconditional correction: For Min-sum unconditional correction, the variable node structure is the same as that of MS, only change is in the check node structure where a fixed correction factor is subtracted from the magnitude of the outgoing messages of check node. The optimal correction factor $Y_c = 1$ is used:

$$\varepsilon_{mn}^{(i)} = \max\left(\min_{n' \in N(m)\backslash n} \left|Z_{mn'}^{(i)}\right| - \gamma_c\right) \prod_{n' \in N(m)\backslash n} \text{sgn}(Z_{mn'}^{(i)}) \quad (4)$$

Min-sum with successive relaxation: In the Min-Sum algorithm with SR, check nodes architecture is the same as that of standard MS and the proposed change is in the variable node structure. The optimal value of $\beta = 0.5$ is used:

$$Z_{mn}^{(i+1)} = Z_{mn}^{(i)} + \beta\left(\left[\lambda_m + \sum_{m' \in M(n)\backslash m} \varepsilon_{m'n}^{(i)}\right] - Z_{mn}^{(i)}\right) \quad (5)$$

The check nodes and the variable nodes are described in the following sections. The variable nodes provide input to the check nodes for all iterations other than the first iteration. The inputs to the first iteration are provided from the channel. In the direction of the PCM matrix, connection exists between the nodes and the messages are iterated based on it. In each iteration, the check nodes $\varepsilon_m^{(i)}$ get updated by the messages from the corresponding variable nodes $Z_m^{(i)}$. Figure 2 and 3 illustrates the architecture of the magnitude update and sign update part for a check node unit, respectively. The check nodes provide input to the variable nodes. Unlike the previous case of check nodes considered, the inputs

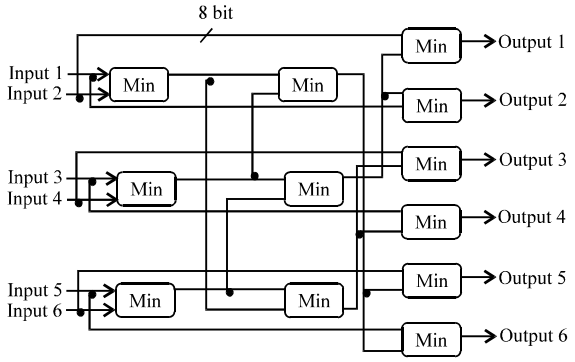

Fig. 2: Magnitude update part for check node unit

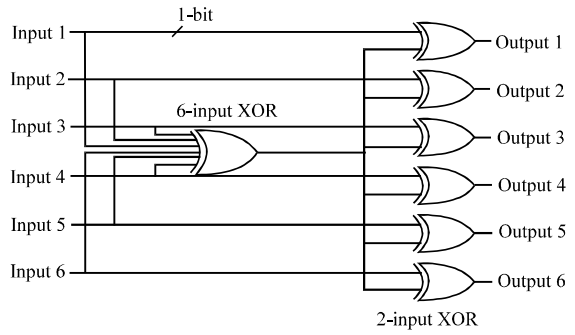

Fig. 3: Sign update part for check node unit

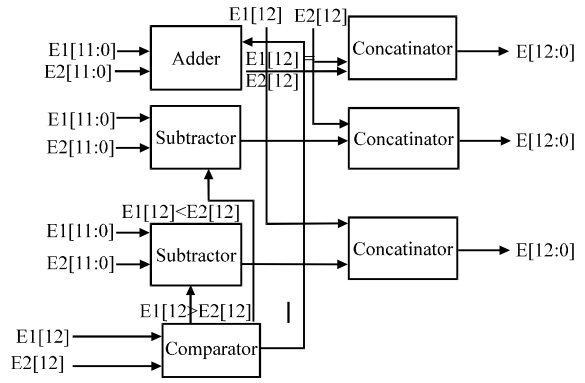

Fig. 4: Architecture of variable node unit of Min-sum decoder

are fed from the check node from the first iteration. The messages from the corresponding check nodes $\varepsilon_m^{(i)}$ update the variable nodes $Z_m^{(i)}$ in every iteration. Figure 4 shows the architecture of variable node unit of Min-sum decoder. Intermediate registers are included between the iterations which explain the concept of conventional pipelining.

The controller checks whether the hard decision has been achieved or not. If not achieved, the iteration count gets incremented and the updating of the check node unit and variable node unit takes place. At each iteration, the hard decision is checked. The output of each iteration is stored in the intermediate registers and given as input for the second iteration. This explains the concept of conventional pipelining. The presence of the intermediate registers increases the area which is an overhead. Even though the latency overhead gets improved when compared to the serial architecture, the area gets increased. The area-latency overhead is optimized by using the principle of wave-pipelining. The architecture shown in Fig. 5 is modified with the wave-pipelining technique called buffer insertion.

MIMO-CDMA System: A MIMO-CDMA System has N_t transmit and N_r receive antennas. The serial data whose bit rate is R_b is converted into N_t parallel data streams each with bit rate R_b/N_t. The ith data stream of user m is spread by spreading waveform $w_{mi}(t)$ which is an antipodal signal with chip rate R_c and is selected from a set of mutually orthogonal spreading waveforms $C_m = \{c_{m1}(t), c_{m2}(t), c_{mN}(t)\}$. In other words:

$$\frac{1}{T}\int_0^T C_{mi}(t)C_{mj}(t)dt = \begin{cases} 1 & \text{for } i=j \\ 0 & \text{for } i\neq j \end{cases} \quad (6)$$

where, $T = N_t/R_b$ denotes the signaling interval. Short spreading waveform with one signaling interval is used in this study. On the interval $0\le t\le T$, the mathematical expression for the ith spreading waveform from the set C_m is given by:

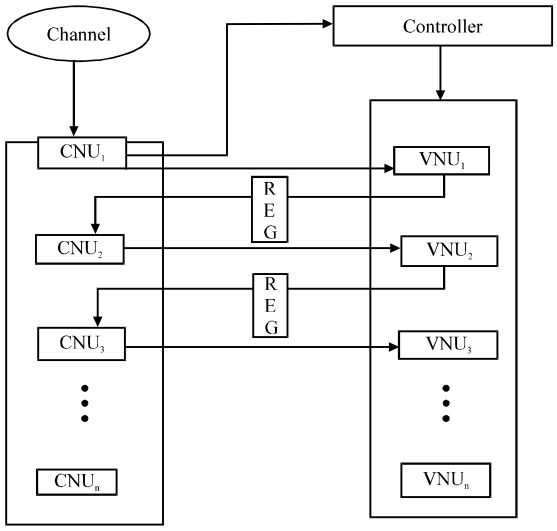

Fig. 5: Architecture of Min-sum decoder

$$C_{mi}^{(t)} = \sum_{j=1}^{L} C_{mi}^{(j)}\rho(t - jT_c) \quad (7)$$

Where:

$C_{mi}^{(t)}$ = ±1 is the jth bipolar chip of the mth user's ith spreading waveform

T_c = $1/R_c$ denotes the chip interval

L = The number of chips in the spreading waveform and is given by $L = T/T_c = R_cN_t/R_b$

$\rho(t)$ = The rectangular chip pulse shape is given by:

$$\rho(t) = \begin{cases} 1 & 0 \le t \le T_c \\ 0 & \text{otherwise} \end{cases} \quad (8)$$

Distinct sets of spreading waveforms are provided for different users. Therefore, $C_m \cap C_l = \phi$ for $m \neq l$. Figure 6 depicts the transmitter, receiver and link gains. During the interval $(n-1)T\le t\le nT$ (signaling interval n), the data transmitted is:

$$m^{(n)} = [m_1^{(n)}, m_2^{(n)}, ..., m_{N_t}^{(n)}]$$

where, $m_k^{(n)}$ is either 0 or 1 with equal probability and they are independent of each other. Binary Phase Shift Keying (BPSK) modulation is used in the proposed architecture. Researchers define:

$$b^{(n)} = 2m^{(n)} - 1 = [b_1^{(n)}, b_2^{(n)}, ..., b_{N_t}^{(n)}] \quad (9)$$

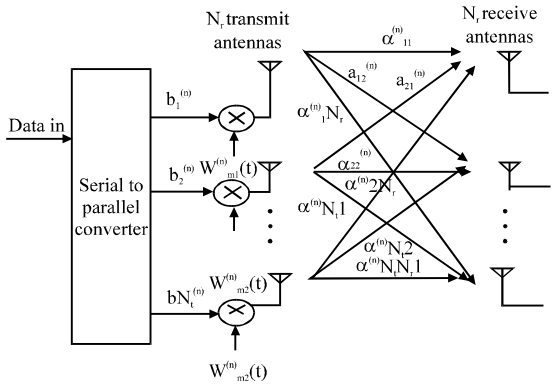

Fig. 6: MIMO-CDMA transmitter and link gains

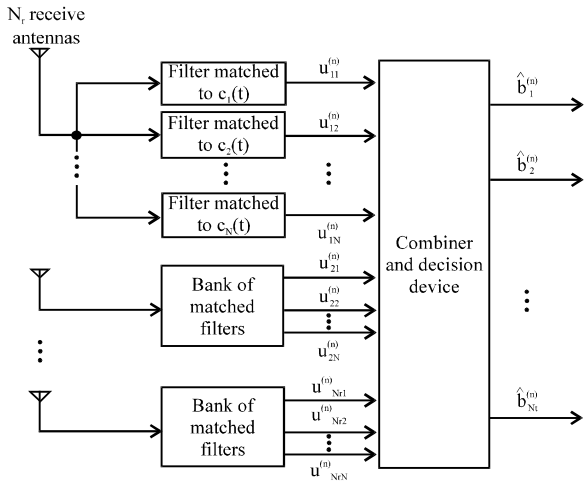

Fig. 7: MIMO-CDMA receiver

where, $b_k^{(n)} = \pm 1$ with equal probability and $E[b_k^{(n)} b_g^{(n)}] = 0$, if $k \neq g$ where E[.] is the expectation operator. $b_k^{(n)}$ is transmitted on transmit antenna k since every independent identically distributed (iid) bit transmitted on the nth signaling interval is assigned to a different transmit antenna. The mth user's data bit is multiplied by spreading waveform $W_{mk}^{(n)}(t)$ since, it is transmitted by transmit antenna k on the nth signaling interval. $\alpha_{ij}^{(n)}$ is the complex channel gain between transmit and receive antenna k and j on the signaling interval, respectively. Figure 7 shows the receiver structure for MIMO-CDMA.

Based on the spreading technique used, the receiver antenna correlates the signal received with each spreading waveform and the contributions from such antennas are combined. $u_{jk}^{(n)}$ denotes the kth matched filter output on receive antenna j with signaling interval n. The expressions connecting these decision variables and how they are related depend on the spreading method used at the transmitter side.

Parity-bit-selected spreading: MIMO-CDMA adapts the Parity-bit-selected spreading technique used for spread spectrum systems with slight changes. The input given to a parity-bit generator is vector m^n and it results a vector $p^{(n)} = [P^{(n)}_1, P^{(n)}_2, ..., P^{(n)}_N]$ where, $N = 2^{length(p)}$ and N is the number of spreading codes used. In each user set as many parity bit patterns as the spreading waveforms are used and each spreading waveform is allotted to one of the parity bit vectors. Therefore, if $p^{(n)} = p_x$ then:

$$W_{mi}^{(n)}(t) = c_{mx}(t - nT) \quad \text{for } i = 1, 2, ..., N_t \tag{10}$$

For Eq. 10, the decision variables mentioned in Fig. 6 are given by:

$$u_{jk}^{(n)} = \begin{cases} \sum_{i=1}^{N_t} \left(\sqrt{E_b} b_i^{(n)} \alpha_{ij}^{(n)} \right) + n_{jk}^{(n)} & k = x \\ n_{jk}^{(n)} & k \neq x \end{cases} \tag{11}$$

where, E_b is the received energy per bit. Let:

$$u^{(n)} = \left[u_{11}^{(n)}, u_{12}^{(n)}, ..., u_{1N}^{(n)}, u_{21}^{(n)}, ..., u_{2N}^{(n)}, u_{N_rN}^{(n)} \right]$$

which is a $1 \times N_rN$ vector. The xth channel gain matrix, $H_x^{(n)}$ is an $N_t \times N_rN$ matrix, defined as:

$$H_x^{(n)} = \left[0_{N_t,(x-1)}, h_1^{(n)}, 0_{N_t,(N-1)}, h_2^{(n)}, 0_{N_t,(N-1)}, h_3^{(n)}, ..., h_{N_r}^{(n)}, 0_{N_t,(N-x)} \right] \tag{12}$$

Where:

$0_{a,b}$ = An a×b all zero matrix

$h_i^{(n)} = [\alpha_{1i}^{(n)}, \alpha_{2i}^{(n)}, ..., \alpha_{N_ti}^{(n)}]$

The channel matrix used on signaling interval n depends on the spreading waveform used during that particular interval. Consider, for example, if the transmitter employs $c_{m1}(t\text{-}nT)$ then $H_1^{(n)}$ is the appropriate channel gain matrix to use. Researchers can now express $u^{(n)}$ as follows:

$$u^{(n)} = \left[\sqrt{E_b} b^{(n)} H_b^{(n)} + n^{(n)} \right] \tag{13}$$

where, $H_b^{(n)}$ is the channel matrix associated with data vector $b^{(n)}$ and $n^{(n)} = [n_{11}^{(n)}, n_{12}^{(n)}, n_{1N}^{(n)}, n_{21}^{(n)}, n_{2N}^{(n)}, n_{N_rN}^{(n)}]$ is a $1 \times N_rN$ noise vector. The elements of $n^{(n)}$ are uncorrelated zero mean complex Gaussian random variables with variance σ_n^2.

Table 1 gives the allocation of spreading waveforms to message vectors as well as the corresponding channel gain matrix used in Eq. 13. From the Table 1, the two

Table 1: Allocation of spreading waveforms in parity-bit-selected spreading technique for $N_t = 4$

Messages m(n)	Spreading waveform	Channel gain matrix
0000	$c_{m1}(t\text{-}nT)$	$H_1^{(n)}$
1111		
0001	$c_{m2}(t\text{-}nT)$	$H_2^{(n)}$
1110		
0010	$c_{m3}(t\text{-}nT)$	$H_3^{(n)}$
1101		
0011	$c_{m4}(t\text{-}nT)$	$H_4^{(n)}$
1100		
0100	$c_{m5}(t\text{-}nT)$	$H_5^{(n)}$
1011		
0101	$c_{m6}(t\text{-}nT)$	$H_6^{(n)}$
1010		
0110	$c_{m7}(t\text{-}nT)$	$H_7^{(n)}$
1001		
0111	$c_{m8}(t\text{-}nT)$	$H_8^{(n)}$
1000		

message vectors m = 0000 and m = 1111 (corresponding to b = -1-1-1-1 and b = 1111) forms a subset of all possible binary message vectors of length 4. This subset is then spread using spreading waveform $c_{m1}(t\text{-}nT)$. The messages from other spreading waveforms are simply co-sets of the subset {0000, 1111}. So, each co-set is associated with a distinct spreading waveform. The smallest of the squared Euclidean distances between $u^{(n)}$ and each of the vectors denoted in Table 1 is computed and is considered as the expected transmitted message vector. In terms of BER performance, $u^{(n)}$ is correlated to each of the vectors mentioned and the one with the maximum correlation value is picked.

Synthesis: The functionalities of the designed pipelined and wave-pipelined architectures are evaluated using Modelsim and the Xilinx and Synopsys tool targeted to 90 nm device is used for synthesis. The synthesis report gives the area and power utilization for the different modules. The area reduction is depicted in the synthesis of the wave-pipelined LDPC encoder architecture. Wave-pipelined architecture is proved to be superior through the latency analysis with the corresponding modules. The Xilinx analysis depicts, the decrease in the number of flip flops, number of slices and number of LUT has been identified with the effect of wave-pipelining. The architecture has been synthesized using Xilinx targeted to Virtex2p.

The encoder is synthesized on the Synopsis tool and the obtained area and power utilization for the encoder (5, 10) are shown in Table 2-4. The area analysis of the proposed model with the existing ones is tabulated in Table 3 and 4. The power analysis of encoder with the existing ones is compared and tabulated in Table 5.

Table 2: Area analysis of encoder (5, 10)

	Encoder (5,10)		
Area occupied (μm^2)	Two stage	Three stage	Wave-pipelined
Total cell area	56780.30	70731.76	32236.59
Total area	135950.10	197790.31	75683.89

Table 3: Area analysis of encoder (5, 10) with the existing results

Methodology	Total cell area (μm^2)	Total area (μm^2)
Behroozi *et al.* (2003)	3652.12	78378.19
Wang *et al.* (2005)	2873.15	76542.10
Wave-pipelined	32236.59	75683.89

Table 4: Power analysis of encoder (5, 10)

	Encoder (5, 10)		
Power	Two stage	Three stage	Wave-pipelined
Total dynamic power (mW)	2.289	2.524	0.1913

Table 5: Power analysis of encoder (5, 10)

Methodology	Total dynamic power (mW)	Logic elements
Behroozi *et al.* (2003)	0.2210	3212
Wang *et al.* (2005)	0.2540	3459
Wave-pipelined	0.1913	2685

EXPERIMENTAL RESULTS

The proposed LDPC coded based CDMA Architecture System is tested on a Spartan-3E family device XC3S500E using Modelsim and Xilinx. This proposed scheme utilized 1972 LUTs and 476 FFs at a maximum frequency of 200 MHz. The proposed research results shows that the CDMA System incorporated with LDPC leads to lower power consumption in terms of slices, Look Up Tables and Flip Flops. The various devices in the Spartan-3 family are tested against their frequency and power and tabulated in Table 6. The proposed LDPC decoder architecture implemented in VLSI is tested with the Spartan-3E family. Figure 8 depicts the power consumption details tested on Spartan-3E family. Quiescent, dynamic and total power is calculated for the Spartan-3E family.

Figure 9 shows the buffer insertion the wave-pipelined architecture. Figure 10 shows the RTL view of the proposed architecture and its technology schematic view. Indigital circuit design, Register-Transfer Level (RTL) is a design abstraction which models adigital circuitin terms of the flow of digital signals (data) betweenhardware registers and thelogical operations performed on those signals. Register-transfer-level abstraction is used inhardware description languages (HDLs) like Verilog and VHDL to create high-level representations of a circuit from which lower-level representations and ultimately actual wiring can be derived. Design at the RTL level is typical practice in modern digital design (Table 7).

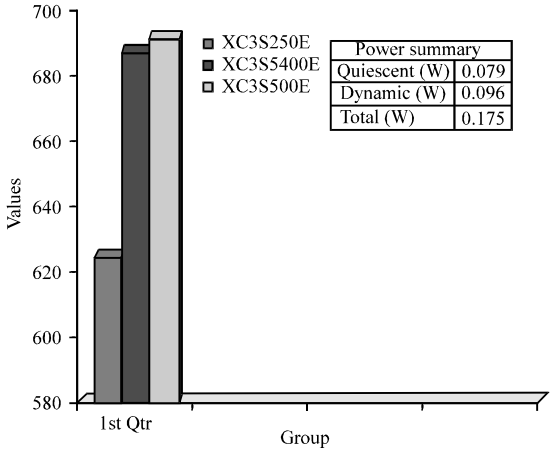

Fig. 8: Power summary of the transient circuit

RTL is used in thelogic design phase of the integrated circuit design cycle. An RTL description is usually converted to agate-level description of the circuit by alogic synthesis tool. The synthesis results are then used by placement and routing tools to create a physicallay out. Logic simulation tools may use a design's RTL description to verify its correctness. The proposed architecture code written using Verilog is synthesized using Xilinx FPGA Navigator 9.2i. The snapshots of the synthesis results for the LDPC architecture in Fig. 10 shows the RTL view and Fig. 11 shows the snapshots of the technological view. It utilized 116 LUTs and 464 Ffs at a maximum frequency of 200 MHz. The proposed research results shows that the CDMA System incorporated with LDPC leads to lower power consumption in terms of slices, Look Up Tables and Flip Flops.

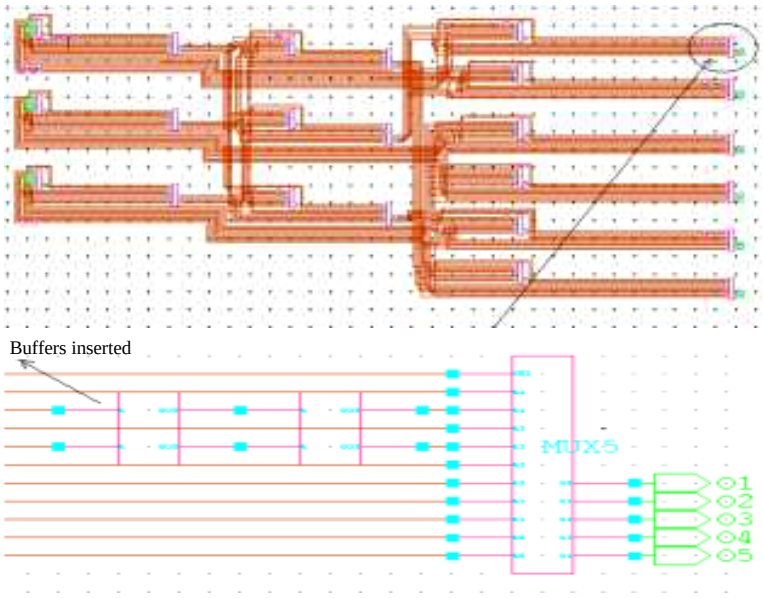

Fig. 9: Buffer Insertion of the wave-pipelined architecture

Table 6: Comparison of power consumptions of Spartan-3 family

FPGA family	Device specifications	Power consumption
Spartan-3E	Xc3s250E	625 mW
Spartan-3E	Xc3s400E	687 mW
Spartan-3E	Xc3s500E	692 mW

Table 7: Comparison between the proposed and existing methods

Methods	Blanksby and Howland (2002)	Liu *et al.* (2005)	Mansour and Shanbhag (2006)	Proposed method
Process	0.13 µm CMOS	0.18 µm	0.18 µm	90 nm
Architecture	Bit serial fully parallel	Partially parallel	Partially parallel	Wave-pipelined
Code construction	Regular 660 bit	Irregular 600 bits	Regular 2048 bits	Regular 2048 bits
Code rate	0.74	0.75	Programmable	Programmable
Supply voltage	1.2	1.8	1.8	1.2
Power (mW)	518	192	787	52 (xc3s250E) 81 (xc3s500E) 159 (xc3s1200E)
Gate count	690	551	-	912
Frequency (MHz)	300	96	-	200

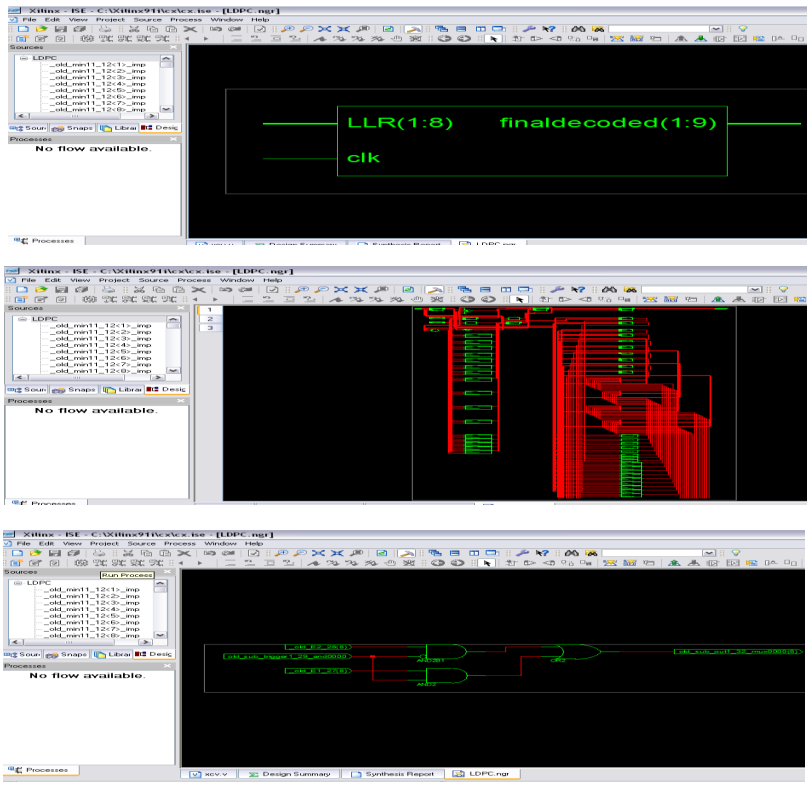

Fig. 10: RTL view of the proposed architecture

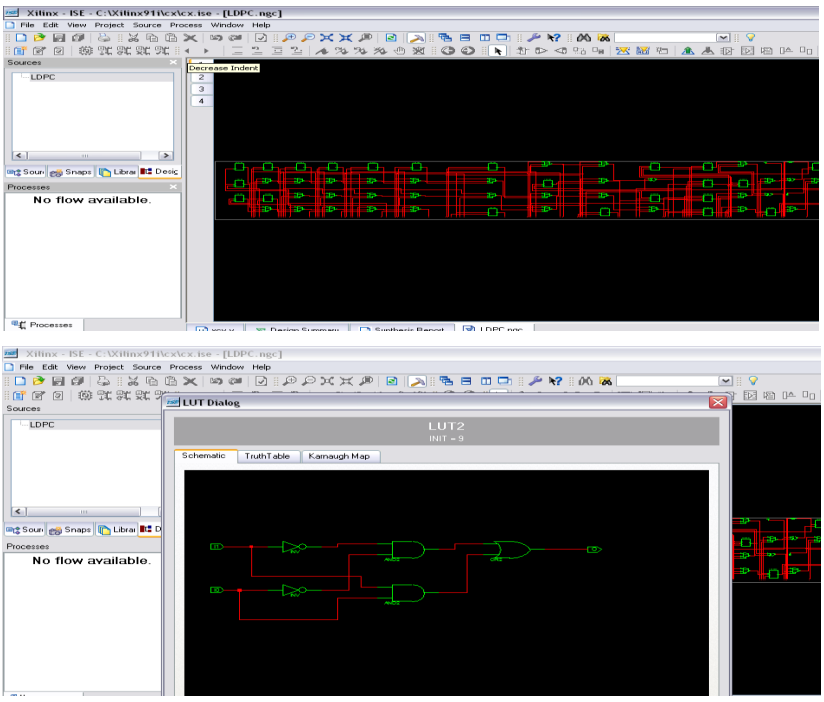

Fig. 11: Technology schematic view of the proposed architecture

CONCLUSION

Researchers proposed the low power LDPC architecture for CDMA System. This proposed Architecture is tested on a 90 nm device using Xilinx platform. Min-sum iterative decoder has a reduced complexity with respect to the architecture-algorithm transformation when compared to other LDPC decoding algorithms. This proposed scheme utilized 1972 LUTs and 476 FFs at a maximum frequency of 200 MHz. The proposed research results show that the CDMA System incorporated with LDPC leads to lower power consumption in terms of slices, look up tables and flip flops. The various devices in the Spartan-3 family are tested against their frequency and power consumption.

REFERENCES

Behroozi, H., J. Haghighat, M. Nasiri-Kenari and S.H. Jamali, 2003. Performance evaluation of LDPC coded MC-FH-CDMA systems over fading channels. Proceedings of the 14th IEEE Personal, Indoor and Mobile Radio Communications, Volume 2, September 7-10, 2003, Beijing, China, pp: 1574-1578.

Blanksby, A.J. and C.J. Howland, 2002. A 690-mW 1-Gb/s 1024-b, rate-1/2 low-density parity-check decoder. IEEE J. Solid-State Circ., 37: 404-412.

Boutros, J. and G. Caire, 2002. Iterative multi-user joint decoding: Unified framework and symptotic analysis. IEEE Trans. Inform. Theory, 48: 1772-1793.

Liu, H.Y., C.C. Lin, Y.W. Lin, C.C. Chung and K.L. Lin *et al*., 2005. A 480Mb/s LDPC-COFDM-based UWB baseband transceiver. Proceedings of the IEEE International Solid-State Circuits Conference, 2005. Digest of Technical Papers, Volume 1, February 10, 2005, San Francisco, CA., pp: 444-609.

Mansour, M.M. and N.R. Shanbhag, 2006. A 640-Mb/s 2048-bit programmable LDPC decoder chip. IEEE J. Solid-State Circ., 41: 684-698.

Moher, M., 1998. An iterative multi-user decoder for near-capacity communications. IEEE Trans. Commun., 46: 870-880.

Papaharalabos, S., P. Sweeney, B.G. Evans, P.T. Mathiopoulos, G. Albertazzi, A. Vanelli-Coralli and G.E. Corazza, 2007. Modified sum-product algorithms for decoding low-density parity-check codes. IET Commun., 1: 294-300.

Shamai, S. and S. Verdu, 2001. The impact of frequency-flat fading on the spectral efficiency of CDMA. IEEE Trans. Inform. Theory, 47: 1302-1327.

Tolouei, S. and A.H. Banihashemi, 2008. FPGA Implementation of variants of min sum algorithm. Proceedings of the 24th Biennial Symposium on Communications, June 24-26, 2008, Kingston, ON., pp: 80-83.

Torrieri, D., A. Mukherjee and H.M. Kwon, 2008. Doubly iterative LDPC-coded DS-CDMA receivers with coherent detection, EM channel estimation and no pilot symbols. Proceedings of the IEEE Military Communications Conference, November 16-19, 2008, San Diego, CA., pp: 1-7.

Tseng, S.M., 2009. Sequential detection for multi-user MIMO CDMA Systems with single spreading code per user. IEEE Trans. Wireless Commun., 8: 3492-3497.

Veeravalli, V.V. and A. Mantravadi, 2002. The coding-spreading trade-off in CDMA systems. IEEE J. Select. Areas Commun., 20: 396-408.

Verdu, S. and S. Shamai, 1999. Spectral efficiency of CDMA with random spreading. IEEE Trans. Inform. Theory, 45: 622-640.

Wang, X., G. Yue and K.R. Narayanan, 2005. Optimization of LDPC-coded turbo CDMA systems. IEEE Trans. Signal Process., 53: 1500-1510.

Yasodha, T. and I.J. Raglend, 2012. BER performance of HARQ MIMO-CDMA systems in multi-user environment. Eur. J. Scient. Res., 86: 340-347.

Yue, G., X. Wang and K.R. Narayanan, 2003. Design of low density parity check codes for turbo multi-user detection. IEEE Int. Conf. Commun., 4: 2703-2707.