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FHSS-FSK Modulator Design and Implementation for a Wireless Sensor Transmitter

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Abstract: This study presents a modulator design and implementation for a wireless sensor transmitter. The transmitter architecture presented combines a Binary Frequency Shift Keying (BFSK) modulator, an up conversion mixer, a power amplifier and an 863-870 MHz bandpass filter. The BFSK modulator uses the Frequency Hopping Spread Spectrum (FHSS) technique operating in the European ISM band 863-870 MHz. This modulator is intended for short-range wireless applications, such as the wireless sensors network. The modulator generates a 7 MHz wide single-sideband frequency hopped spread spectrum waveform. This modulator is designed using the Direct Digital Frequency Synthesizer (DDFS), which enables us to generate BFSK signal with the hopping frequencies. Low power DDFS architecture is presented. It uses a smaller lookup table for sine and cosine functions compared with existing systems using a minimum additional hardware. The evaluated Spurious Free Dynamic Range (SFDR) of the proposed modulator is -88 dBc. A modulator IC has been designed in AMS 0.35 μm standard CMOS process technology with a layout chip area of 0.16 mm^2 . A 20-bit frequency control word gives a tuning resolution of 41.29 Hz at 43.4 MHz sampling rate. This modulator consumes 47.7 μW with a 3V supply at 43.4 MHz.

Key words: Wireless sensor, FHSS, DDFS, SFDR, BFSK, direct conversion transmitter

INTRODUCTION

The market for low power, short-range wireless sensor and control technology is expected to show explosive growth during the coming years. The typical applications are home automation, industrial control and monitoring, automatic meter reading and alarms. There are so many applications for this low data rate short-range wireless sensor such as industrial and commercial, home automation, personal computer peripherals, consumer electronics, personal health care and game that should be able to operate for five years under battery energy supply.

Recently developed new standards are under consideration for wireless sensor networking. Examples include Bluetooth (IEEE 802.15.1), UWB (IEEE 802.15.3) and Zigbee (IEEE 802.15.4). Each of these standards is accompanied by limitations for sensor networks. For example, currently available Bluetooth devices show excessive power consumption for sensor network applications (Trung *et al.*, 2006).

The Electronic Communications Committee (ECC) has established new strategic plans for the future use of the 863-870 MHz band for Short Range Devices (SRD) (Electronic Communications Committee, 2002).

Therefore, the 863-870 MHz band, which is available only in Europe, is a good field to test new ideas and concepts toward the development of a low power transceiver for short range and low data rate applications.

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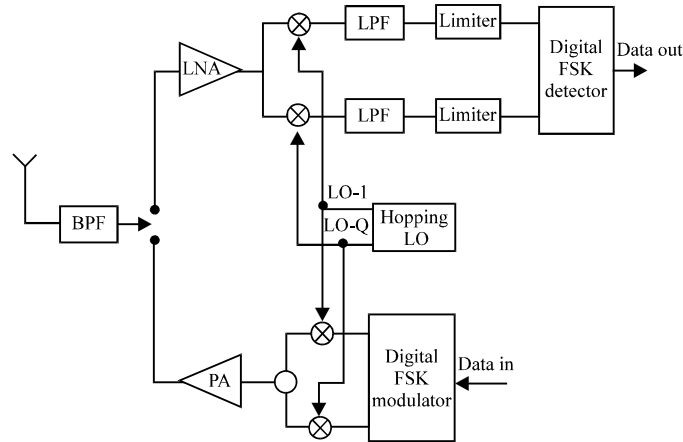


Fig. 1: Wireless sensor transceiver architecture

The direct conversion transmitter has recently attracted widespread attention for its simple architecture and easy integration with the base band circuit, as well as for its low power consumption and low manufacturing costs (Ahmadreza *et al.*, 1998).

Thus, our objective consists in the design of an independent wireless sensor in order to set up a wireless sensor network inside a building. The transmitter is designed for BFSK modulation, with a data rate of 20 kb sec⁻¹. This modulator is designed using the DDFS.

In this study, a low-power technique using a small ROM and 4 pipelined phase accumulator were used to implement DDFS.

Transmitter Architecture

The transceiver architecture is presented in Fig. 1. The transmitter part operates as follows: The digital FSK modulator modulates the data and synthesizes in a quadrature outputs a FHSS signals at base band.

A fixed-frequency oscillator up converts these outputs to the ISM band in a single-sideband mixer. With an 866.5 MHz oscillator, in the center of the ISM band either the upper or the lower sideband is selected to place the instantaneous carrier frequency anywhere in the band. The modulator is based on DDFS. The DDFS output frequency needs only to span from 0 to 3.5 MHz to cover the ISM range of 866.5±3.5 MHz.

The digital data is carried by symbol tones at an offset of either ±20 kHz from the carrier frequency. This system can achieve a maximum data rate of 20 kb sec⁻¹ by sending two symbols per hop.

The theoretical study for determining the data rate is presented in the following section.

Data Rate Selection

If at each transmission the node sends one full packet, then the overall average power consumption Pd of the transmitter node can be approximated by:

$$P_d = P_{tx} \frac{T_{tx}}{T} + \frac{P_{dss}}{T} (T_{tx} + T_{wu}) + \frac{P_{ide}}{T} (T - T_{tx} - T_{wu}) \quad (1)$$

where, P_{tx} is the power radiated from the antenna, T_{tx} is the time required for each transmission, T_{wu} is the wakeup time of the transmitter (i.e., the time required to start up the circuitry), P_{ide} is the

power dissipated in the idle mode when most of the transmitter functions are off, P_{diss} is the non-radiated power dissipated by the transmitter and T is the time interval between two consecutive transmissions. From the Shannon-Hartley theorem, it is known that:

$$D = B \log_2 \left(1 + \frac{S}{N} \right) \quad (2)$$

where, B is a fixed bandwidth and D is the maximum data rate achievable on an additive white Gaussian noise channel. The term S/N is the signal to noise ratio at the demodulator side ($SNR_{in, dem}$) and can be related to the signal to noise ratio at the receiver input ($SNR_{in, rec}$) by:

$$\frac{SNR_{in, rec}}{SNR_{in, dem}} = NF \quad (3)$$

where, NF is the noise factor of the receiver. Suppose that the received signal arrives attenuated by a factor PL (path loss), then:

$$SNR_{in, dem} = \frac{P_{tx}}{N_{AWGN} \cdot B \cdot NF \cdot P_L} \quad (4)$$

where, N_{AWGN} is the power spectral density of an additive white Gaussian noise channel. Substituting (2) in (4), yields an expression for the transmitted power as a function of all the other parameters:

$$P_{tx} = N_{AWGN} \cdot B \cdot NF \cdot P_L \cdot \left(2^{\frac{D}{B}} - 1 \right) \quad (5)$$

Now the transmission time is defined as:

$$T_{tx} = \frac{L_{packet}}{D} \quad (6)$$

where, L_{packet} is the packet length. Substituting (5) and (6) in (1), an approximated formula is obtained for the power dissipated by the transmitter as a function of the data rate. If the receiver has a noise factor of 20 dB, then the overall power consumption, as a function of D and P_{diss} appears as shown in Fig. 2 for a packet length of 100 bits. Here each node transmits every 1 min, with a bandwidth of 80 kHz, the channel attenuation is 102 dB, the wake-up time is 1 msec and the P_{idle} is 10 μ W. From this Fig. 2, it is clear that the data rate can be lowered to a certain value. Below some hundreds of bits per second the duty cycle will increase to a point for which, the power dissipated in the transmitter circuitry will dominate, increasing the overall power consumption.

In conclusion, target of 20 kb sec^{-1} is selected with a balance between the requirements of lower power, bandwidth efficiency favouring closely spaced channels and a BFSK tone frequency that avoids the impact of CMOS flicker noise and DC offset.

Frequency Allocation

The transmitter is designed for BFSK modulation, with a data rate of 20 kb sec^{-1} (Trabelsi *et al.*, 2006). The power spectrum of a BFSK signal is represented in Fig. 3. The transmission bandwidth B of the BFSK signal was calculated to be 80 KHz.

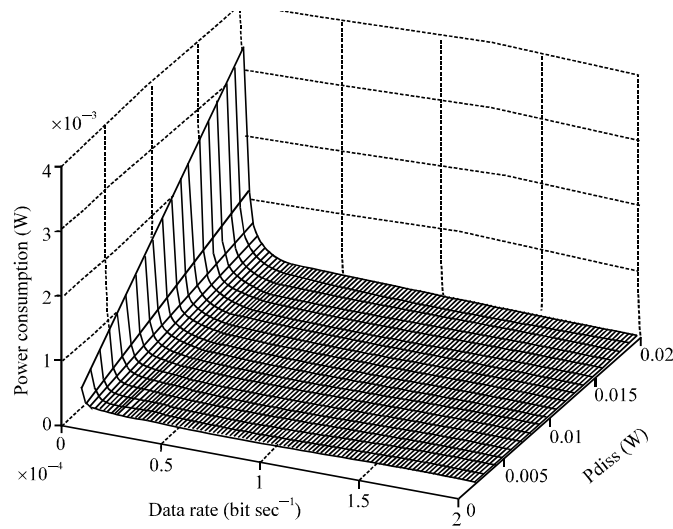


Fig. 2: Power consumption as a function of data rate and power dissipated by transmitter circuitry

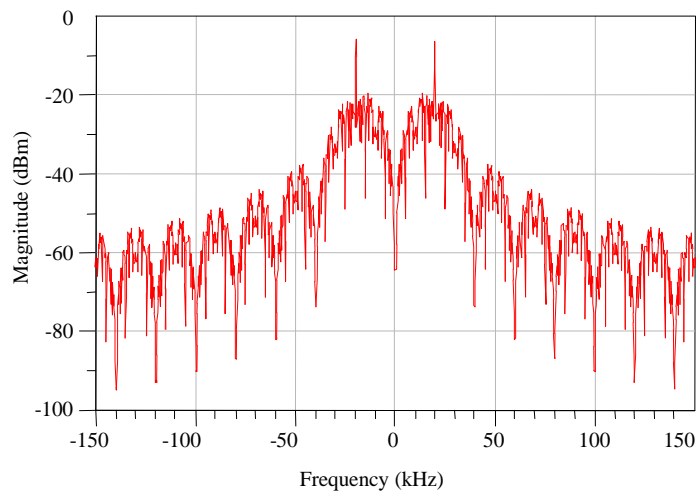


Fig. 3: Power spectrum of a BFSK signal (bit rate = 20Kbps)

A maximum of 58 channels has been chosen to fulfil FHSS requirement and ETSI regulations (which demand a minimum separation of 25 kHz between adjacent channels) (Electronic Communications Committee, 2002; Trabelsi *et al.*, 2006). Therefore, the separation between adjacent channels has been chosen equal to 40 kHz. The allocation of the 58 channels is shown in Fig. 4.

Modulator Design

The modulator is implemented using scalable cells, which have been sized down to the minimum required clocking speed of 43.4 MHz. Frequency is selected with a 20 bit frequency control word to obtain a $F_{clk}/2^N$ frequency control resolution, where N is the number of frequency control bits and Fclk

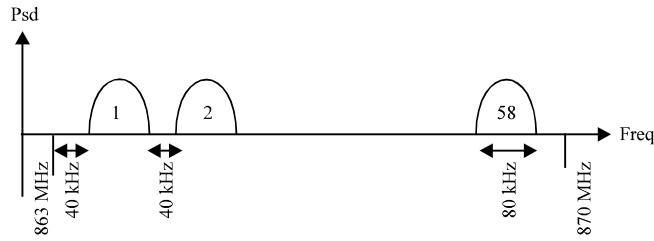


Fig. 4: Channels allocation in the 863-870 MHz band

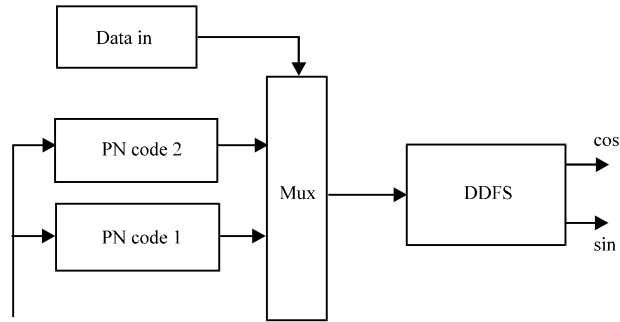


Fig. 5: The Modulator block diagram

is the sampling frequency of the DDFS/DAC. For $F_{clk} = 43.4$ MHz, the smallest frequency resolution is 41.29 Hz. The frequency control word sets the accumulation rate in the phase accumulator, which addresses ROMs containing coefficients of the trigonometric sine and cosine waveforms to produce digital-domain quadrature outputs at the programmed frequency. The choice of internal word length guarantees that in the worse case, imperfections in the DDFS will result in spurious tones of at least -72.6 dBc relative to the fundamental frequency (Yang *et al.*, 2004).

The architecture proposed of the modulator system is shown in Fig. 5. Essentially, a modulator consists of a DDFS, a PN code generator and a mixer. The DDFS creates digital samples of a baseband sinusoidal waveform by addressing a sine ROM at a frequency set by a 20-bit control word. The PN code is a random generator code, which corresponds to the hopping patterns. The mixer selects one of the two codes generated by both PN code generators.

The PN code generator and the DDFS used in the modulator are explained in the following sections.

Pn Code Generator

In its frequency hopping sequence, the signal hops to a different channel during each hopping period. The discrete hop frequencies are determined by a PN code sequence stored in the memory before the input control register of the DDFS. The carrier frequency hops at 20 hops sec^{-1} among these 58 channels, according to a pseudo random sequence.

The PN code is a random generator code which has a 20 bits length and works at the rising edge of a clock frequency which is lower than the sampling frequency. At each clock edge the PN code will generate a binary word N (frequency control word), which serves as incremental phase for the DDFS, as shown in Fig. 6. The N binary words are stored in a ROM memory that will be sent to the DDFS at each clock period. The hardware description and design of the PN code generation has

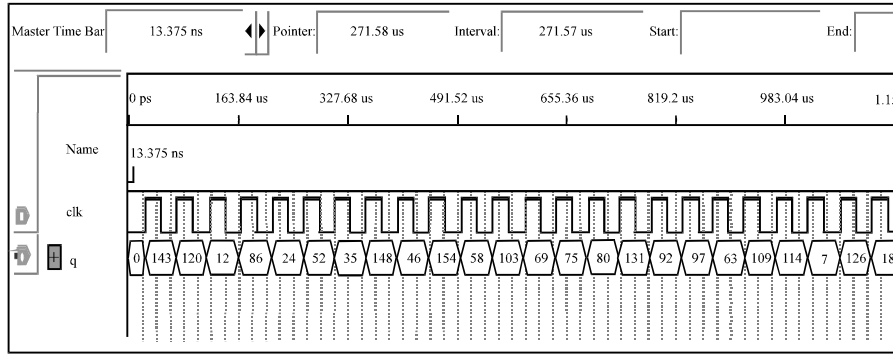


Fig. 6: Simulation results for PN code

been done using the VHDL. Post simulation of the designed modules has been done using the VHDL simulator to verify the description.

DDFS Description

The overall architecture of a typical DDFS system is shown in Fig. 7. Essentially, a DDFS consists of a phase accumulator and a sine/cosine generator. The phase accumulator input is a frequency control word (F_{cw}). The phase accumulator is an overflowing N bit accumulator whose value specifies the instantaneous phase. The rate at which this phase ramp overflows gives the generated frequency which is proportional to F_{cw}.

The amplitude of a sinusoidal signal is digitally stored in a ROM and is consecutively fetched by the output of an accumulator, which feeds the address line of the ROM (Tierney *et al.*, 1971). The output sine wave produced has the same frequency as the phase ramp rate overflow, which is proportional to F_{cw}. The output sine samples can be converted to an analog waveform using a digital-to-analog converter (DAC) and a low-pass filter (LPF) (Lee and Park, 2003).

The accumulator input and its word-length determine the output frequency value and resolution, respectively.

The generated frequency F_{out} is related to the frequency control word and the reference frequency F_{clk} by:

$$F_{out} = \frac{F_{cw} * F_{clk}}{2^N}$$

where, N is the accumulator word-length (Akram and Swartzlander, 2003).

The two main parts, the phase accumulator and the ROM, of the DDFS are explained in the following sections.

The Phase Accumulator

The phase accumulator, shown in Fig. 8, is a 20 bit adder that repeatedly increments the phase angle by F_{cw}. Therefore, its output increases by F_{cw} at each clock cycle. At the time n, the phase accumulator output is given by:

$$\Phi = \frac{n * F_{cw}}{2^N}$$

and the sine/cosine generator must compute $\sin(2\pi n F_{cw}/2N)$ and $\cos(2\pi n F_{cw}/2N)$.

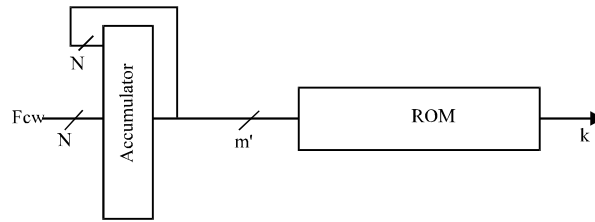


Fig. 7: Typical DDS system

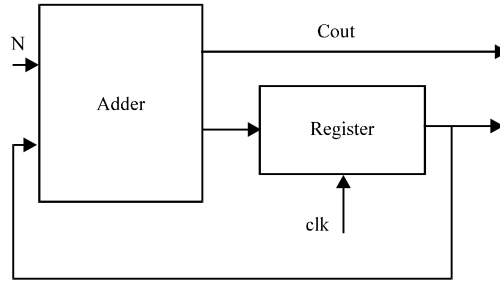


Fig. 8: The phase accumulator block diagram

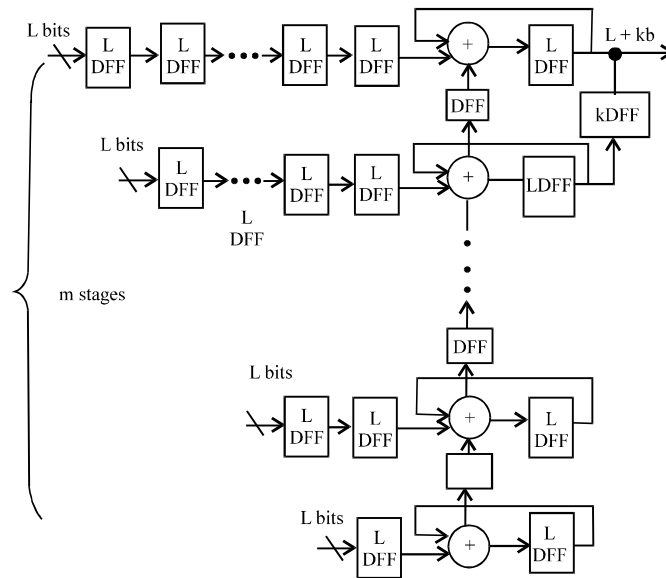


Fig. 9: A conventional pipelined accumulator

A large phase accumulator is frequently used in DDS for the fine frequency resolution at high clock frequency. However, this large accumulator cannot finish one addition in a small single clock period because of the delay caused by the carry bits propagating during the addition. A typical solution is to pipeline the phase accumulator as m stages of L bits each, such that $m \times L = N$ as shown in Fig. 9. Each adder generates $L+1$ bits output: L sum bits and one carry output bit. The carry output

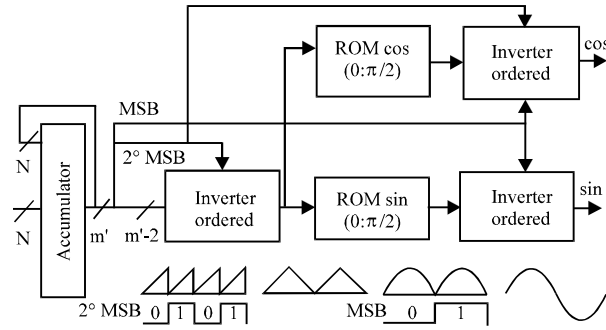


Fig. 10: Block diagram of proposed DDS

is latched between successive adders. Every new frequency control word is moved into the pipeline circuits consisting of D-flip-flops (DFF) and delay elements. The speed of the phase accumulator, based on this architecture, can be increased up to m times. For the DDS implementation, we used a four level pipelined phase accumulator.

However, the pipeline circuit requires considerable area and power and introduces more frequency switching latency. At the same time, increasing the number of pipelined blocks would increase the loading of the clock network.

The Read Only Memory

A first step towards the reduction of sine/cosine generator complexity consists in truncating the least significant bits (LSBs) from the phase accumulator (Fig. 10). This introduces spurious noise in the DDS outputs (Strollo *et al.*, 2007; Jafari *et al.*, 2005), which should be carefully taken into account in the design phase. Another common approach, usually used to simplify the sine/cosine generator, exploits the quadrant symmetry of trigonometric functions and identities. For a quadrature DDS, this reduces the task of the sine/cosine generator to the calculation of sine and cosine functions for angles belonging to the interval only. For a single-phase DDS, sine calculation for phase angles, belonging to the first quadrant, is required. Simple DDS implementations use a ROM lookup table to calculate trigonometric functions.

One effective method of reducing the ROM size is to exploit the quarter-wave symmetry properties of the sine curve. Thus the quadrant-decode technique is employed in order to generate a full sine wave.

The second MSB is used to determine whether the phase accumulator output has to be inverted and the first MSB determines whether the sine amplitude output of the LUT has to be inverted. This method produces a four-fold decrease in the ROM size.

MODULATOR SYSTEM-LEVEL SIMULATION

Modulator Simulations

The most demanding characteristics of modulator are SFDR and output spectrum. The simulation purpose is to determine the design performance of the modulator. The design in Fig. 5 is coded by VHDL, which is then simulated by Modelsim. The VHDL code is then synthesized by Quartus.

Figure 11 shows the modulator output for maximum code. At each clock rising edge (clk1), the PN code will generate a binary word N (frequency control word), which serves as incremental phase for the DDS. At each DDS increment (clk2), the modulator will generate a sample of sin and cos, as shown in Fig. 11. At each signal edge (s), the mixer switches between both PN code generators. The

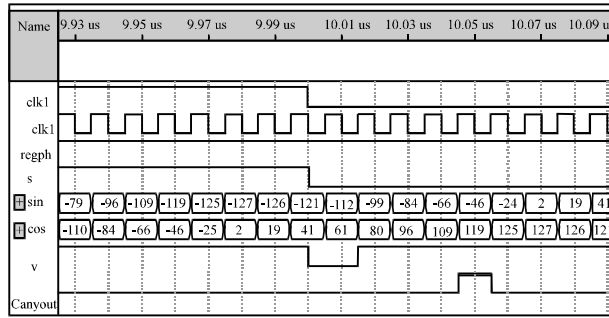


Fig. 11: Simulation results for maximum code

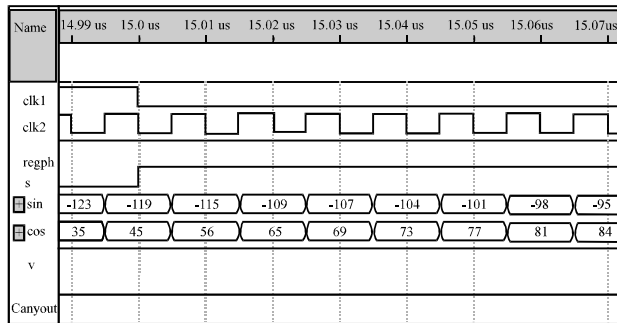


Fig. 12: Simulation results for minimum code

output of the modulator for minimum code is presented in Fig. 12. Figure 13 shows the quadrature phase between sine and cosine. We note that if the sine is zero, the cosine is in its maximum and when the sine takes maximum values, the cosine begins to take negative values. Figure 13 shows the transition of sine and cosine signals corresponding to two different codes before and after the inversion.

Spurious-Free Dynamic Range (SFDR)

The SFDR is defined as the ratio of the desired frequency component amplitude to that of the largest undesired frequency component at the output of a modulator, as shown in Fig. 14. Its value is usually expressed in decibels. An undesired (spurious) frequency component is often called a spur. Modelsim of Mentor and MATLAB of Mathworks are the software tools to perform system-level simulations. Meanwhile, the decimal output data in a 10-bit format are collected. The Fast Fourier Transform (FFT) command of MATLAB is executed to obtain the spectrum as shown in Fig. 14, which illustrates that the spurious performance of the proposed method is as high as -88 dBc. It is far better than any prior works.

The data shown in Table 1 compare the performances of the developed DDFS with recently published state-of-the-art circuits, using CMOS technology, SFDR and clock frequency similar to the ones considered in this paper. The proposed IC exhibits a power dissipation reduction by a factor larger than 10 and a substantial decrease of the maximum clock frequency, with respect to the solutions proposed in (Langlois and Al-Khalili, 2003). The DDFS of (De Caro *et al.*, 2004) dissipates 51% more power and has higher output resolution and SFDR. However, it is faster than our design.

Table 1: Performance and comparison of proposed DDFS

| Parameters | (Langlois and | | | |
|----------------------------------|--------------------------------|-------------------|-----------------------------|----------|
| | (De Caro <i>et al.</i> , 2004) | Al-Khalili, 2003) | (Chen <i>et al.</i> , 2006) | Proposed |
| Fcw (bits) | 24.00 | 32.00 | 32.00 | 20.00 |
| Phase accumulator output (bits) | 14.00 | 13.00 | 12.00 | 12.00 |
| Output (bits) | 12.00 | 12.00 | 10.00 | 10.00 |
| Fclk (MHz) | 480.00 | 150.00 | 500.00 | 43.40 |
| SFDR (dBc) | -80.00 | -84.00 | -70.00 | -88.00 |
| Power dissipation (μ W/MHz) | 72.00 | 500.00 | 34.40 | 47.70 |
| Pipeline levels (cycle) | 6.00 | 4.00 | 2.00 | 4.00 |
| Complexity (mm ²) | 0.075 | 0.09 | 0.04 | 0.08 |
| Supply voltage (V) | 2.500 | 1.80 | 1.80 | 3.00 |

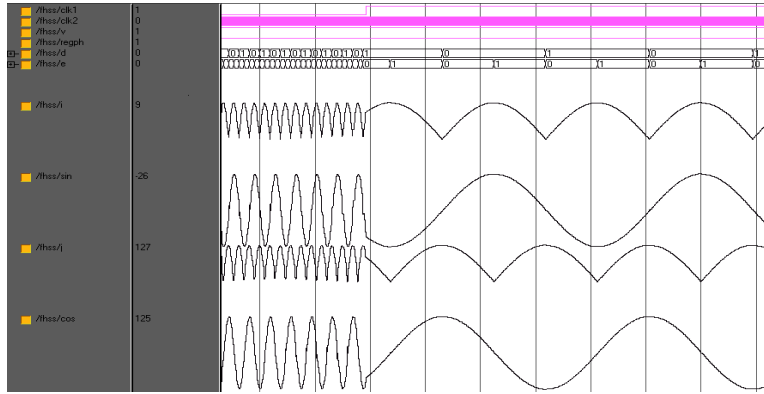


Fig. 13: Modulator Block simulation results

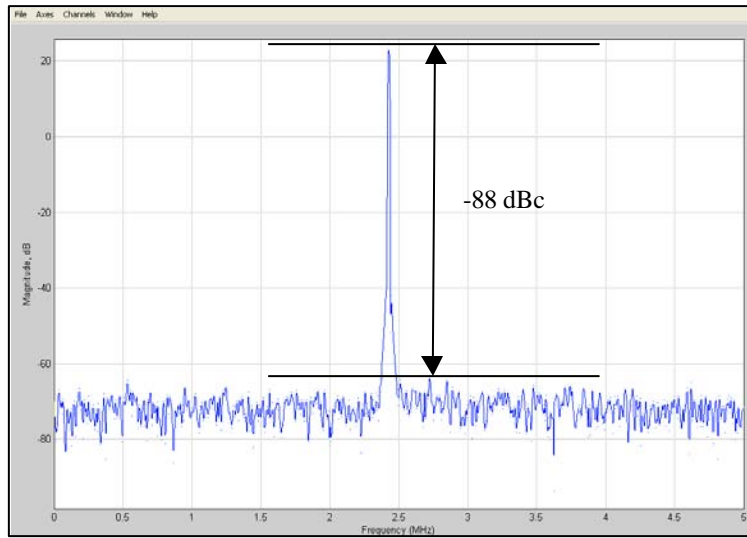


Fig. 14: Spurious performances of the proposed modulator for the 24th code

Simulation results show that the average power dissipated is 47.7 μ W at 43.4 MHz. It is interesting to conclude that the DDFS power dissipation is close to 63% of the total power. The power consumption of the PNcode1 and PNcode2 is 17 and 18%, respectively. The power dissipation of the accumulator is not negligible since it requires about 19% of the total power. The power consumption of the lookup tables is as low as 22%.

The chip operates from a nominal 3V power supply. The modulator chip layout, shown in Fig.16, contains 1205052 transistors and has a die size of approximately (0.396 \times 0.396) mm².

CONCLUSION

In this study, we have presented a novel FHSS-FSK modulator implementation design. First, we have presented a novel method exploiting the quadrant symmetry of trigonometric functions and trigonometric identities for the purpose of reducing DDFS spurious tones. A new DDFS architecture based on this technique was presented. A DDFS has been presented which uses a smaller lookup table for sine and cosine functions and four level pipelined phase accumulator. Furthermore, we described the modulator simulation results, which have been designed using the proposed DDFS. It enabled us to generate BFSK signal with frequency hopping. The design was implemented using a 0.35 μ m CMOS technology. It occupies a core area of 0.16 mm². The entire chip operates at a low supply-voltage of 3 V. Simulation results show that the average power dissipated is 47.7 μ W at 43.4 MHz with an 88dBc SFDR.

REFERENCES

- Ahmadreza, G., J.J. Chang, J.Y.C. Rael, M. Chang, P.J. Rofougaran, M. Chang, J. Djafari, E.Min, W. Roth, A.A. Abidi and H. Samueli, 1998. A single-chip 900-MHz spread-spectrum wireless transceiver in 1- μ m CMOS-Part II: Receiver Design. *IEEE J. Solid-State Circuits*, 33 (4): 535-547.
- Akram and Jr. E.E. Swartzlander, 2003. Direct digital frequency synthesis using piece-wise polynomial approximation. *IEEE Int. Signals Syst. Comput. Conference Paper*, 1 2: 2237-2241.
- Chen, R. Luo, H. Yang and H. Wang, 2006. A low power rom-less direct digital frequency synthesizer with preset value pipelined accumulator. *IEEE International Vlsi Design Conference Paper*, pp: 377-380.
- De Caro, E. Napoli and A.G.M. Strollo, 2004. High speed direct digital frequency synthesizers in 0.25 μ m CMOS. *IEEE Custom Integrated Circuits Conference Paper*, pp: 163-166.
- Electronic Communications Committee (ECC), 2002. Strategic plans for the future use of the frequency bands 862-870 MHz and 2400-2483.5 MHz for short range devices within the European Conference of Postal and Telecommunications Administrations (CEPT), Helsinki.
- Jafari, A. Ayatollahi and S. Mirzakuchaki, 2005. A low power, high SFDR, ROM-Less direct digital frequency synthesizer. *IEEE International Microelectronics Conference Paper*, pp: 50-54.
- Langlois and D. Al-Khalili, 2003. A low power direct digital frequency synthesizers in 0.18- μ m CMOS. *IEEE Custom Integrated Circuits Conference Paper*, pp: 283-286.
- Lee and I.C. Park, 2003. Quadrature direct digital frequency synthesis using fine-grain angle rotation technique in electron. *Letter*, 39 (17): 1235-1237.
- Strollo, D.De Caro and N. Petra, 2007. A 630 MHz, 76 mW Direct digital frequency synthesizer using enhanced ROM compression technique. *IEEE J. Solid-State Circuits*, 42 (2): 350-360.
- Tierney, C.M. Rader and B. Gold, 1971. A digital frequency synthesizer. *IEEE Trans. Audio Electoracust*, AU-19: 48-57.

- Trabelsi, Gh. Bouzid, Y. Jaballi, L. Bouzid, F. Derbel and Mohamed Masmoudi, 2006. System level design of a low power, short range FHSS transceiver for Wireless sensor in 4eme International Conference. JTEA, 06: 120-124.
- Trung, Nam J.O., H.L. Viet and G.L. Sang, 2006. A low power CMOS direct conversion receiver with 3dB NF and 30KHz flicker-noise corner for 915-MHz band IEEE 802.15.4 ZigBee standard. IEEE Trans. Microwave Theory Tech., 54 (2) Part 1: 735- 741.
- Yang, J., H. Choi, S.H. Han, L.S. Kim and H.K. Yu, 2004. An 800-MHz low-power direct digital frequency synthesizer with an on-chip D/A converter. IEEE J. Solid-State Circuits, 39 (5): 761-774.