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Research Article
An Optimized Balance Control for Capacitor Voltage of Modular Multilevel Converter under Max-Min Function Algorithm

[1]M.A. Kuntian, [1]L.I. Hua and [2]X.U. Yu

[1]Electric Power College, Inner Mongolia University of Technology, Inner Mongolia Autonomous Region, Hohhot 010080, China
[2]Inner Mongolia Electric Power Research Institute, Inner Mongolia Autonomous Region, Hohhot 010080, China

Abstract

Background and Objective: In the current MMC-HCDC engineering, the average voltage of the capacitor of the converter mostly adopts the sorting class algorithm. However, under this algorithm, after re-ordering each control cycle, the sub-modules will be heavily re-switched and the switching state of the sub-modules will change frequently. As a result, the service life of the sub-modules will be reduced and the investment in MMC-HVDC engineering will increase. So, it is important to research the switching frequency of sub-modules in MMC-HVDC engineering. **Materials and Methods:** In current research, the sub-module switching mode is divided into three types. Only change the switching status of Dn sub-modules with the largest or smallest capacitor voltage which have been selected. **Results:** The sorting algorithm which was already known and the Max-Min algorithm are compared in the PSCAD/EMTDC and the sub-module switching frequency of Max-Min algorithm is reduced from 1100-262.5 Hz. Max-Min algorithm has no negative effect on the amplitude of capacitance voltage fluctuation of the sub-module. The operation period is shortened and the operation burden is reduced. **Conclusion:** The computation time of the Max-Min function is shorter than that of the current sorting algorithm. Compared with the sorting algorithm which was already known, the switching frequency of the Max-Min function is smaller. It provides a new optimization strategy for the capacitance uniform voltage control under the sorting algorithm commonly used in the MMC-HVDC engineering.

Key words: Modular Multilevel Converter (MMC), capacitance voltage balancing, switching frequency, switching state, max-min function

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Corresponding Author: L.I. Hua, Electric Power College, Inner Mongolia University of Technology, Inner Mongolia Autonomous Region, Hohhot 010080, China

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INTRODUCTION

In the case of increasingly depleting fossil energy, the flexible DC transmission technology (HVDC) based on Modular Multilevel Converter (MMC) topology provides a flexible and reliable technical solution for the development of new energy. The reasonable control strategy of MMC determines whether it can run normally and stably, so it is particularly important. Many scholars at home and abroad have done a lot of research and exploration on the control strategy of MMC and the balance control of capacitor voltage of sub-module is one of the research focuses. The study of Rong *et al.*[1] is suitable for the large number of sub-modules, for the high switching frequency of the converter and the huge amount of operation. The base method is introduced to reduce the sorting times, reduce the work burden of the converter and reduce the unnecessary switching signal. Aiming at the dynamic distribution of the voltage of the sub-modules through programmable gates array to complete the fast segmentation of the capacitor voltage[2]. For the converter with pulse width modulation, the switching frequency of the sub-module can be operated under the fundamental frequency condition by the cooperation of the switching signals of each sub-module[3]. Aiming at the problem of the switching frequency of sub-modules, a method of comparing the reference values is used[4]. Dividing the sub-modules into two groups for switching can effectively reduce the switching frequency of the sub-modules. For the capacitor voltage in the MMC converter, the problems of fluctuation and high switching frequency of the sub-modules are divided into different groups for processing according to the voltage division[5]. For engineering problems, real-time simulation and programming are used to complete the sub-block voltage equalization control.

Since MMC usually contains hundreds of sub-modules in the project, the number of IGBT in so many sub-modules is more. Frequent switching of IGBT results in huge losses and shortened life. Therefore, research on how to reduce losses and reduce the switching frequency is particularly important. In current research, a change in the number of switching of the upper and lower arm sub-modules in the front-to-back period is proposed.

MATERIALS AND METHODS

Study area: The study was started in the month of August, 2018 at the Institute of Electric Power, Inner Mongolia University of Technology and the data were collected in the month of October-December, 2019.

Figure 1 shows the MMC and sub-module structure. Each phase of the three-phase modular multilevel converter includes two upper and lower bridge arms (i_C) and sub-module voltage u_C, current i_{SM}. The relationship can be expressed as[6]:

$$\begin{cases} u_C = u_C^0 + \frac{1}{C}\int_0^t i_C dt \\ i_C = Si_{SM} \end{cases} \quad (1)$$

where, S is the switching function, S = 1 is on, S = 0 is off.

The voltage formula of the bridge arm:

$$\begin{cases} u_{pi} = \sum_{j=1}^{N} S_{pij} u_{pij}, i = a,b,c \\ u_{ni} = \sum_{j=1}^{N} S_{nij} u_{nij}, i = a,b,c \end{cases} \quad (2)$$

where, u_{pi} with u_{ni} is the upper and lower arm voltage, S_{pij} u_{pij} is the switching state and capacitor voltage of the high-arm sub-module, S_{nij} u_{nij} is the switching state and capacitor voltage of the lower arm sub-module, that is, each arm voltage is supported by the sub-module capacitor voltages of all input states[7].

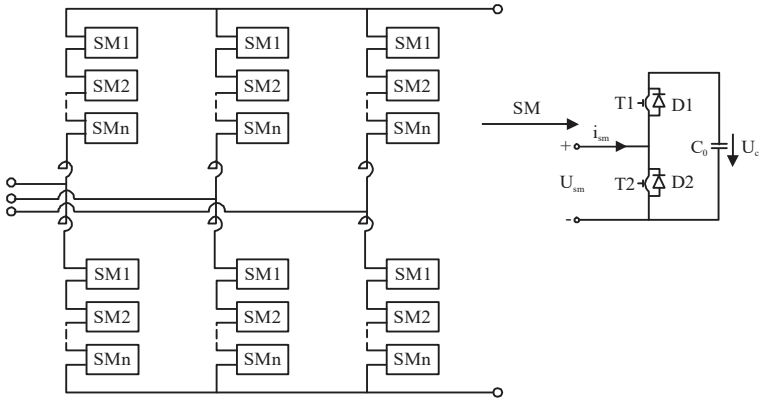

Fig. 1: Structure of MMC converter and sub-module
MMC: Modular multilevel converter

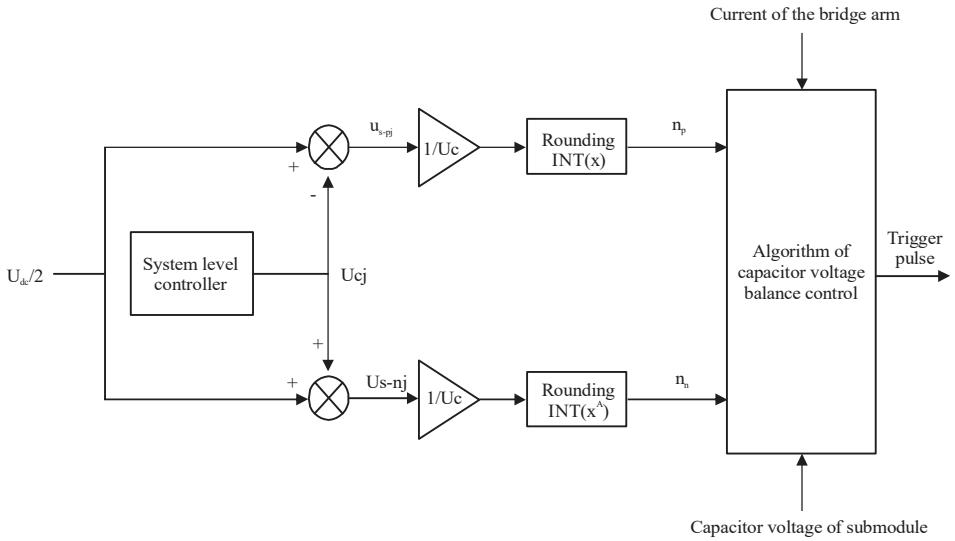

Fig. 2: The process of NLM

Phase voltage is:

$$\begin{cases} u_{si} = -l\frac{di_{pi}}{dt} - u_{pi} + \frac{1}{2}U_{dc}, i = a,b,c \\ u_{si} = l\frac{di_{ni}}{dt} + u_{ni} - \frac{1}{2}U_{dc}, i = a,b,c \end{cases} \quad (3)$$

Modulation method: The most recent level of NLM modulation used in current research is a modulation method commonly used in MMC converters, which is a low-frequency modulation, which is usually used in conjunction with a sorting algorithm. The NLM modulation is particularly suitable for multilevel converters and high-frequency converters compared with the modulation method, in a multilevel converter, it has a smaller calculation load, a relatively small workload, a lower harmonic content on the AC side and can output a better sinusoidal waveform[8].

Figure 2 is the process of NLM, the u_{s-pj} is the modulation wave voltage of the upper arm and the u_{s-nj} is the modulation wave voltage of the lower arm. It can get the number of sub-modules that should be put into on each arm by dividing sub-module rated voltage[9]. This process is the NLM, which can only determine the number of sub-modules switched, but cannot determine which sub-modules are switched, which need to be matched with the Algorithm for Capacitor Voltage Balance Control[10].

Max-min function algorithm: Although the current sub-module capacitor voltage balance control strategy can effectively control the capacitor voltage balance of the sub-modules, the high switching frequency has always been a difficult problem to solve[11], because it controls the sub-module capacitor voltage in each cycle. After sorting, a large number of sub-modules will be switched on and off again, resulting in a high switching frequency and the switching loss will increase accordingly. Therefore, as the core of the switching principle of the sub-module, the optimization of the capacitor voltage balance control strategy is particularly important[12,13].

Based on the sorting algorithm which was already known, current research uses a capacitor voltage balance control algorithm based on the max-min value function (Program A), only the sub-modules with the largest or smallest capacitor voltages are changed to change their switching status.

The core content of the algorithm includes:

The core 1: In order to make as few sub-modules as possible to change the switching state in each control cycle, it is necessary to follow n_p (or n_n) the unit climbs or descends and the switching event traverses each level of MMC. In order to meet the above requirements, the sampling period of the controller must be lower than the shortest period between two adjacent switching events, which must follow formula of Eq. 4:

$$T_S \le \frac{1}{1.2\omega}\arcsin\left(\frac{2}{1.4N}\right) \quad (4)$$

where, ω is the grid angular frequency, T_S is the sampling period. The N is bigger and Δt is smaller.

The core 2

Sub-module selection method: Switching change according to the number of bridge arm sub-modules Δn different, the switching of the sub-module can be divided into three working modes, as follows:

- **Working mode 1:** The change of switching number of each bridge arm sub-module Δn>0 when selecting the Δn sub-module, the bridge arm current is positive (or negative), the sub-module is charged (discharged) and the capacitor with the smallest (or maximum) capacitor voltage is selected in the bypassed sub-module Δn make investments
- **Working mode 2:** Number of input sub-modules Δn<0 the bridge arm current is positive (or negative) and the sub-module is charged (discharged). Select the largest (or the smallest) capacitor voltage among the sub-modules that have been put in Δn resection
- **Working mode 3:** When the number of input sub-modules does not change, that is, Δn = 0, the bridge arm current is positive (or negative), the sub-module is charged (discharged), when the capacitor voltage in the input state is the largest (or minimum) sub-module and the capacitor module in the cutoff state is the smallest (or maximum). When the absolute value of the voltage difference between the two exceeds the set threshold, it is replaced, otherwise the original state is maintained

Figure 3 shows the flow chart of the capacitor voltage balance control algorithm based on the Max-Min function. $\Delta n > n_{on}(t) - n_{on}(t-\Delta t)$, $n_{on}(t)$ is the number of sub-modules that need to be in the current cycle, $n_{on}(t-\Delta t)$ is the number of sub-modules that need to be in the previous cycle, i_{pn} is the bridge arm current and $|\Delta U|$ is the absolute value of the voltage difference between the sub-module with the largest (or minimum) capacitor voltage in the input state and the sub-module with the smallest (or maximum) capacitor voltage in the cut-off state, ΔU_{ref} is the decision threshold.

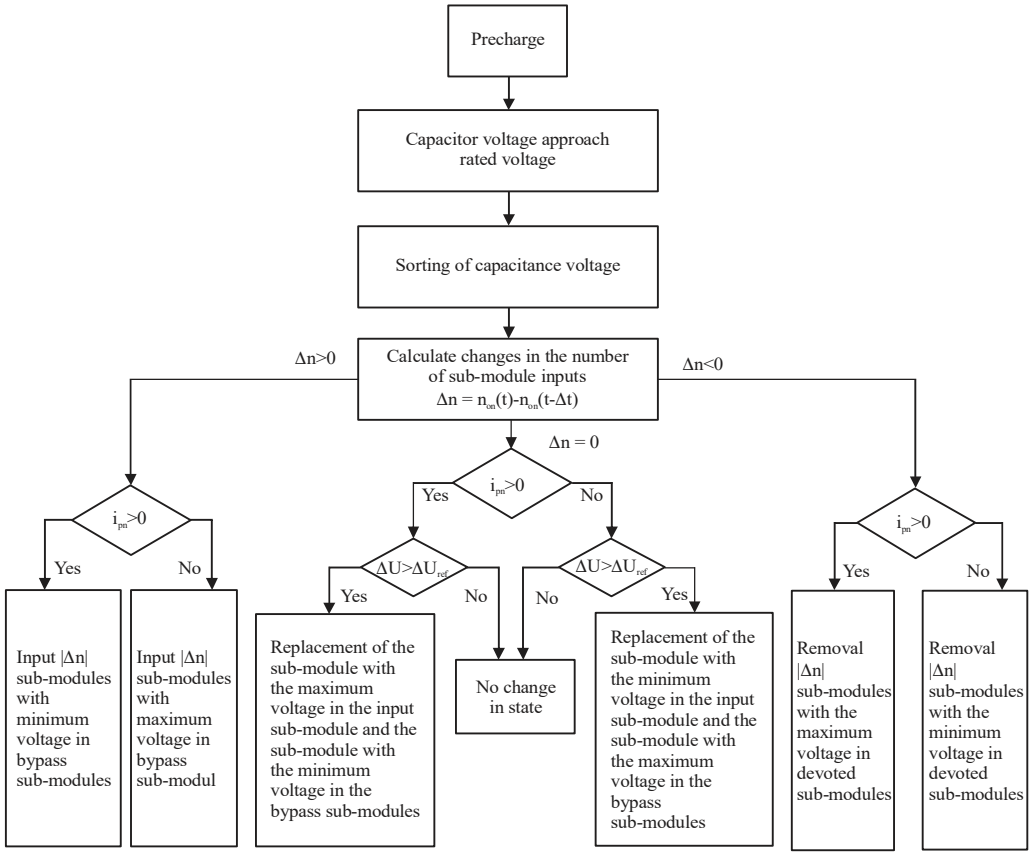

Fig. 3: Flowchart of capacitor voltage balance algorithm based on max-min function

Program A: Max-Min function algorithm (Fortran)

```
SUBROUTINE SMOPT_DETECTOR(SW1,SW2, N, OPT_OUT)
      INTEGER N,I
      INTEGER SW1(N),SW2(N),OPT_OUT(N)
      DO I=1,N
         OPT_OUT(I) = SW1(I)*1 + SW2(I)*2
      END DO
      END SUBROUTINE
      SUBROUTINE LOCK_LOCK(MODULE_NUM, SW1, SW2,Upref_forw)
      INTEGER MODULE_NUM,I,Upref_forw
      INTEGER SW1(MODULE_NUM), SW2(MODULE_NUM)
      DO I=1, MODULE_NUM
SW1(I) = 0
SW2(I) = 0
END DO
Upref_forw = 0
END SUBROUTINE
      SUBROUTINE
 UN_LOCK(MODULE_NUM,SW1,SW2,Upref_forw,Upref,Ip,OPT_in,Uc)
      INTEGER MODULE_NUM,Upref_forw,Upref,Sub_index
      INTEGER I
      REAL Ip,Uc(MODULE_NUM)
      INTEGER SW1(MODULE_NUM), SW2(MODULE_NUM)
      INTEGER OPT_in(MODULE_NUM)
      DO I = 1, MODULE_NUM
         SW1(I) = 0
           SW2(I) = 1
      END DO
      Upref_forw =Upref
END SUBROUTINE
SUBROUTINE BANLANCE_CAP(Upref_forward, Upref,Uc, Ip, SW1, SW2,
Module_num, OPT_in, U_sm, V_tri)
      INTEGER Module_num, Upref_forward, Upref
      INTEGER SW1(Module_num), SW2(Module_num), OPT_in(Module_num)
      REAL IP, Uc(Module_num),U_sm, V_tri,UT,Delta_U
      INTEGER Sub_index1,Sub_index2,Sub_index
INTEGER U_out(Module_num)
      INTEGER I
      UT = U_sm * V_tri
      call MAX_to_MIN(Module_num, Uc,U_out)
      IF (Ip>0.01) THEN
      DO I=1,Upref
      SW1(U_out(I)) =1
SW2(U_out(I)) =0
OPT_in(U_out(I)) =1
END DO
      DO I=Upref+1,Module_num
      SW1(U_out(I)) =0
SW2(U_out(I)) =1
OPT_in(U_out(I)) =2
END DO
      ELSE
      DO I=Module_num-Upref+1,Module_num
      SW1(U_out(I)) =1
SW2(U_out(I)) =0
OPT_in(U_out(I)) =1
END DO
      DO I=1,Module_num-Upref
      SW1(U_out(I)) =0
SW2(U_out(I)) =1
OPT_in(U_out(I)) =2
END DO
END IF
Upref_forward=Upref
      IF(Upref_forward .EQ. Upref) THEN
      call MAX_SERACH_IN(Module_num, Uc, OPT_in, Sub_index)
         Sub_index1=Sub_index
         call MIN_SERACH_OUT(Module_num, Uc, OPT_in, Sub_index)
         Sub_index2=Sub_index
         Delta_U=ABS(Uc(Sub_index1)-Uc(Sub_index2))
         IF (Delta_U>UT) THEN
         SW1(Sub_index1)=0
         SW2(Sub_index1)=1
         SW1(Sub_index2)=1
         SW2(Sub_index2)=0
         END IF
      END IF
      END SUBROUTINE
      SUBROUTINE MAX_SERACH_IN(Module_num, Uc, OPT_in, Sub_index)
      INTEGER Module_num
      INTEGER OPT_in(Module_num), Sub_index
      REAL Uc(Module_num)
      INTEGER I
      REAL Uc_temp
      Uc_temp =0
      DO I=1,Module_num
         IF (OPT_in(I) .EQ. 1) THEN
            IF (Uc(I).GE.Uc_temp) THEN
                        Uc_temp = Uc(I)
                        Sub_index = I
            END IF
         END IF
      END DO
      END SUBROUTINE
      SUBROUTINE MAX_SERACH_OUT(Module_num, Uc, OPT_in, Sub_index)
      INTEGER Module_num
      INTEGER OPT_in(Module_num), Sub_index
      REAL Uc(Module_num)
      INTEGER I
      REAL Uc_temp
      Uc_temp =25
      DO I=1,Module_num
         IF (OPT_in(i).EQ.2) THEN
            IF (Uc(I).GE.Uc_temp) THEN
                        Uc_temp = Uc(I)
                        Sub_index = I
            END IF
         END IF
      END DO
      END SUBROUTINE
      SUBROUTINE MIN_SERACH_IN(Module_num, Uc, OPT_in, Sub_index)
      INTEGER Module_num
      INTEGER OPT_in(Module_num), Sub_index
      REAL Uc(Module_num)
      INTEGER I
      REAL Uc_temp
      Uc_temp =25
      DO I=1,Module_num
         IF (OPT_in(i) .EQ. 1) THEN
            IF (Uc(I) .LE. Uc_temp ) THEN
                        Uc_temp = Uc(I)
                        Sub_index = I
            END IF
         END IF
      END DO
      END SUBROUTINE
```

```
SUBROUTINE MIN_SERACH_OUT(Module_num, Uc, OPT_in, Sub_index)
INTEGER Module_num
INTEGER OPT_in(Module_num), Sub_index
REAL Uc(Module_num)
INTEGER I
REAL Uc_temp
Uc_temp =25
DO I=1,Module_num
    IF ( OPT_in(i).EQ.2 ) THEN
        IF (Uc(I).LE.Uc_temp) THEN
                Uc_temp = Uc(I)
                Sub_index = I
        END IF
    END IF
END DO
END SUBROUTINE
SUBROUTINE MIN_SERACH_LOCK(Module_num, Uc, OPT_in, Sub_index)
INTEGER Module_num
INTEGER OPT_in(Module_num), Sub_index
REAL Uc(Module_num)
INTEGER I
REAL Uc_temp
Uc_temp =25
DO I=1,Module_num
    IF (OPT_in(I).EQ.0) THEN
        IF (Uc(I).LE.Uc_temp) THEN
                Uc_temp = Uc(I)
                Sub_index = I
        END IF
    END IF
END DO
END SUBROUTINE
SUBROUTINE MAX_SERACH_LOCK(Module_num, Uc, OPT_in, Sub_index)
INTEGER Module_num
INTEGER OPT_in(Module_num), Sub_index
REAL Uc(Module_num)
INTEGER I
REAL Uc_temp
Uc_temp =25
DO I=1,Module_num
    IF ( OPT_in(I).EQ.0 ) THEN
        IF (Uc(I).GT.Uc_temp) THEN
                Uc_temp = Uc(I)
                Sub_index = I
        END IF
    END IF
END DO
END SUBROUTINE
SUBROUTINE MAX_to_MIN(Module_num, Uc,U_out)
INTEGER Module_num
REAL Uc(Module_num)
INTEGER U_out(Module_num)
INTEGER I,J
INTEGER temp
REAL Uc_temp
Uc_temp =0
DO I=1,Module_num
U_out(I)=I
END DO
DO I=1,Module_num-1
Uc_temp=Uc(U_out(I))
DO J=I,Module_num
        IF (Uc(U_out(J)).LT.Uc_temp) THEN
                Uc_temp = Uc(U_out(J))
temp=U_out(I)
U_out(I)=U_out(J)
U_out(J)=temp
        END IF
    END DO
    END DO
    END SUBROUTINE
```

RESULTS

A two-terminal 201-level MMC-HVDC transmission model is built in PSCAD/EMTDC as shown in Fig. 4. Its two-terminal AC system is active system it is used to simulate the operation of the MMC-HVDC system.

Table 1 is the simulation parameters of MMC-HVDC system. It is designed according to the relationship between voltage level, capacity and distance of HVDC transmission system. Table 2 is the parameters of controller. Fixed DC voltage control and fixed reactive power control are adopted on MMC1 side. Fixed active power control and fixed reactive power control are adopted on MMC2 side.

In order to verify the effectiveness of the capacitor voltage balance control under the maximum value function, the capacitor voltage balance control of the current sequencing algorithm and the proposed algorithm were simulated and verified, respectively.

Figure 5 is the capacitor voltage of sub-module under sorting algorithm which was already known. Figure 6 is the capacitor voltage of sub-module under the max-min function algorithm. By comparing Fig. 5 and 6, it was found that the max-min function algorithm cause the capacitance of the sub-module with the largest capacitor voltage to have a deviation,

Table 1: Simulation parameters of MMC-HVDC system

Parameters	Values
Conveying power	500 MW
Inter-electrode voltage	500 kV
Number of bridge arm sub-modules	200
Sub-module capacitance	7500 uF
Sub-module voltage	2.5 kV
Bridge arm reactance	0.1 H
AC-side system voltage	230 kV
System frequency	50 Hz

Table 2: Parameters of controller

Controller	K_p	T_i
Active power controller	0.0001	0.03
Reactive power controller	0.0001	0.03
DC voltage controller	2.5	0.05
Inner ring current controller	0.48	0.007
Circulation controller	0.8	0.001

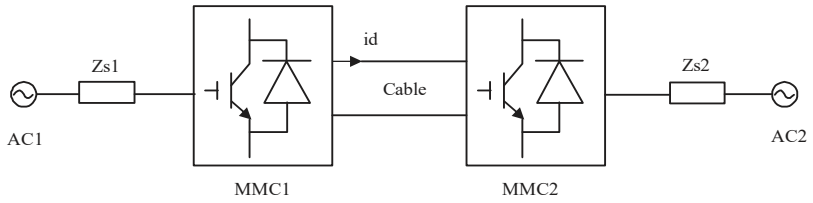

Fig. 4: MMC-HVDC system structure

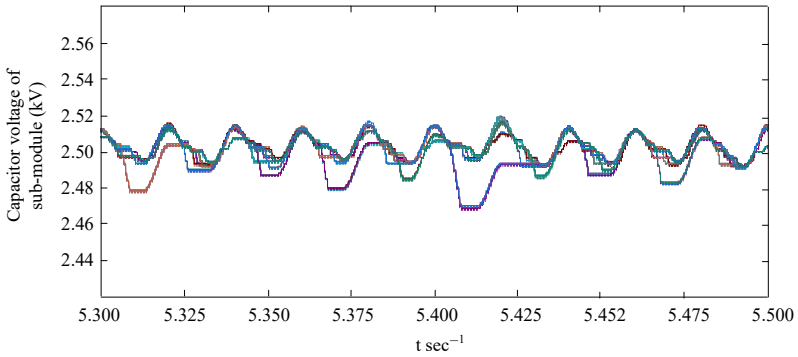

Fig. 5: Capacitor voltage of sub-module under sorting algorithm which was already known

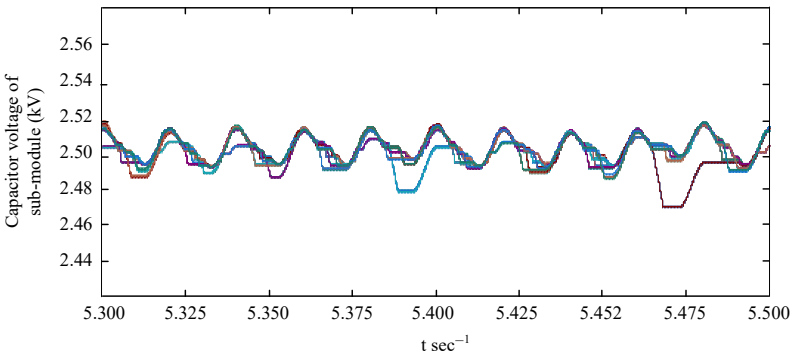

Fig. 6: Capacitor voltage of sub-module under the max-min function algorithm

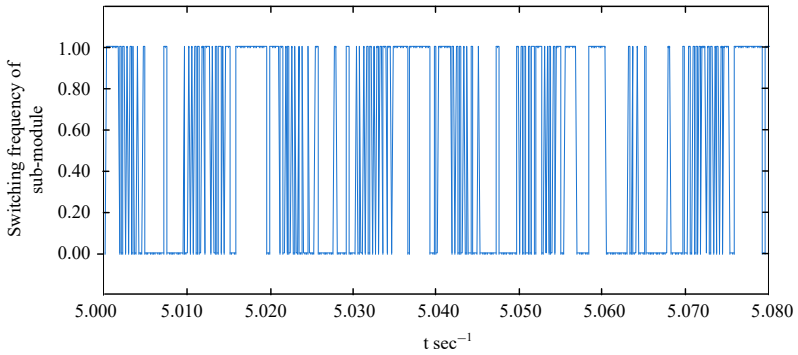

Fig. 7: Switching frequency of sub-module under sorting algorithm which was already known

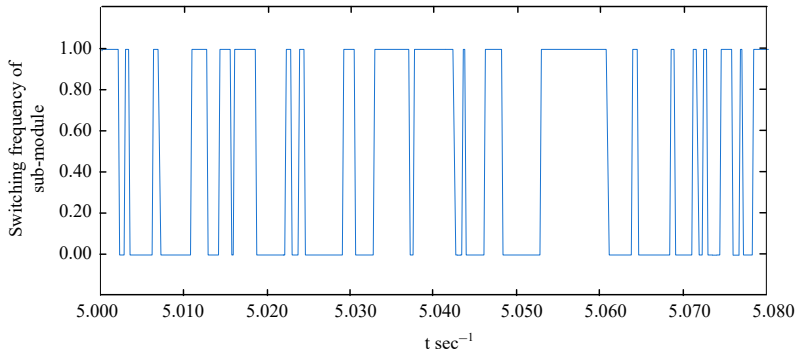

Fig. 8: Switching frequency of sub-module under the max-min function algorithm

Table 3: Trigger frequency of the sub-modules under the two algorithms

Control algorithm	Average switching frequency of sub-module
Sorting algorithm which was already known	1100 Hz
Max-min function algorithm	262.5 Hz

but the deviation is low and it has little effect on the converter voltage. This is because the energy stored in the sub-module is proportional to the square of its voltage.

Figure 7 is the switching frequency of sub-module under sorting algorithm which was already known. Figure 8 is the switching frequency of sub-module under the max-min function algorithm. As is shown in Fig. 7 and 8, the switching frequency of sub-module under the max-min function algorithm decreased obviously in 4 cycles (1 cycle is 0.02 sec).

Through a large number of experiments and collected relevant data. It can be seen in Table 3 that the average switching frequency of sub-module under the max-min value function capacitor voltage balance control is reduced from 1100-262.5 Hz.

DISCUSSION

In May, 2006, State Grid Corporation of China established the Research Framework on the Key Technologies of HVDC System. Then the first MMC-HVDC test project in China was completed in 2008[14]. The key technology of MMC-HVDC (the control strategy of MMC converter) is not perfect, especially the fluctuation limit of capacitance voltage, the switching frequency of sub-module and the protection control of MMC.

Based on the multiple studies that were read while conducting this study, one of them was based in Guan and Xu[15]. They studied the MMC control strategy, which can limit the switching frequency of sub-modules to some extent. Their study mainly aimed at limiting the voltage fluctuation of sub-modules, but the goal of this study is to reduce the switching frequency of sub-modules more often as is shown in Fig. 5-8 and Table 3. Wang *et al.*[16] studied the modulation of MMC converters, which mainly focused on the application of two different modulation methods: NLM and CPS-PWM in MMC. Their study did not link the modulation mode to the capacitor voltage equalization control, but this study combined NLM modulation with capacitor voltage equalization control. The research result of Luo *et al.*[17] showed that the calculation time of the MMC controller can be reduced effectively, which is similar to this study, both of them can reduce the operation time of the controller. This study achieved the goal of reducing the calculation time of the controller through the core algorithm 1, but their study achieved this goal by grouping the sub-modules. Chang *et al.*[18] studied the capacitance equalization problem, which used FPGA (Field-Programmable Gate Array) to sort the capacitance voltage of the sub-module in real time. So that the operation time of the controller does not increase with the increase of the number of sub-modules, but also reduces the switching frequency of the sub-module. There were various similarities in the results; both of them can reduce the operation time of the controller and reduce the switching frequency of the sub-module at high level. The difference is that the operation time of the controller in this study is fixed. When the number of levels is low, the operation time of the controller in their study is higher than that in this study. So, it is only suitable for high level converters. A theory of closed-loop charging strategy for MMC sub-modules is proposed by Zhang *et al.*[19]. Their study has a good auxiliary role for this study. It helps to speed up the operation of MMC into the phase of sub-module capacitance voltage control.

The current research focuses on the problem of high switching frequency of the MMC-HVDC converter. On the one hand, it can effectively reduce the switching frequency and improve the life of the IGBT. On the other hand, it reduces the operation time of the MMC controller. As the direct current

transmission system develops towards high voltage and high power, if there is no significant breakthrough in the future research on IGBT withstand voltage, then only by continuously optimizing the control strategy of the MMC converter can the stable control of the capacitance voltage be completed with the increasing number of sub-modules.

CONCLUSION

In current research, the sub-module switching mode is divided into three types. Only change the switching status of Δn sub-modules with the largest or smallest capacitor voltage which have been selected. Advantages of the capacitor voltage balance control strategy under the max-min function algorithm. The work mode has been optimized. The calculation of the max-min value function takes less time than the sorting algorithm which was already known. Compared with the sorting algorithm which was already known, each control cycle basically only changes the switching state of a very small number of sub-modules. Ensuring extremely low IGBT tube switching frequency provides a new optimization strategy for capacitor voltage equalization control under the sequencing algorithm commonly used in MMC-HVDC engineering, which can extend the service life of IGBT tubes in MMC systems and reduce investment.

SIGNIFICANCE STATEMENT

This study discover the max-min function can effectively reduce the switching frequency of sub-module in MMC-HCDC project, that can be beneficial for raising the service life of IGBT in the sub-module. So, that the cost of this link of MMC-HVDC project can be reduced. At the same time, there is no negative effect on the fluctuation amplitude of the capacitance voltage of the sub-module. In addition, the operation time of the algorithm is relatively broken and the workload is small. This study will help the researcher to uncover the critical areas of balance control for capacitor voltage of MMC that many researchers were not able to explore. Thus, a new theory on balance control for capacitor voltage of MMC may be arrived at.

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