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Glitch Free and Cascadable Adiabatic Logic for Low Power Applications

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Abstract: There have been several reports in literature on realization of adiabatic circuits. In our investigations we propose a family of adiabatic circuits which consist of two branches and which enable control of charging and discharging of the capacitive load only by the input signal alone, work with single time varying supply and with no need of complementary inputs unlike in most of the adiabatic circuits reported in literature. A mathematical expression has been developed to explain the energy dissipation in our adiabatic inverter circuit. Measurements of energy drawn, energy recovered and dissipated have been carried out through simnlation and they agree well with those obtained from the theoretical expression. In the proposed circuit, the input and output logic levels are approximately the same and can be used for building cascaded logic circuits. The energy saving in this family is to the tune of 50% compared to CMOS circuits constructed with similar circuit parameters, up to 250 MHz.

Key words: Adiabatic logic, low power digital circuits, cascadable logic, adiabatic inverter, hierarchical circuits

INTRODUCTION

There is considerable work going on in low power VLSI design through out the world. While there are several conventional approaches like altering the input vectors, operating the circuits at low voltages, using devices with multiple threshold voltages, switching off idle circuits etc, there is an unconventional approach where in, part of the output energy is pumped back into the supply. Adiabatic circuits are a family of circuits in which the energy is saved by pumping it from the capacitive loads back into supply. Several attempts have been made to realize adiabatic circuits. In the adiabatic logic families proposed by Younis and Knight (1994) the energy dissipation is less but each gate requires 16 times the number of devices compared to conventional logic. The 2N-2P and the 2N-2N2P circuits proposed by Kramer *et al*. (1995) and the Efficient Charge Recovery Logic (ECRL) circuit proposed by Moon and Jeong (1996) require four-phase clocking. The need for a mnltiple-phase power clock not only increases the power dissipation of the clocking network, but also it results in extra complexity of both the logic and the required power clock generator. The scheme for realization of adiabatic circuits proposed by Athas *et al*. (1994) is based on transmission gates with limited cascadability. Dickinson and Denker (1995) proposed diode based dynamic logic to form adiabatic dynamic logic circuits. Gates are simple and they occupy small area. Drawbacks are that the gates are

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dynamic and a four phase clocking is needed for cascading the gates. Further, the load capacitor is charged irrespective of inputs and the outputs of these circuits are only valid during a particular phase of the power clock cycle which limits the cascadability and produces unwanted outputs also.

We have proposed a new family of adiabatic circuits (Glitch Free and Cascadable Logic- GFCAL), which consist of two branches, one for charging and another for discharging of the capacitive load. These require single-phase supply and input and can be used in cascaded and hierarchical circuits. Further, glitches in this circuit are avoided as the capacitor either charges or discharges depending only on the input conditions. The energy saving in this family is to the tune of 50% compared to CMOS circuits constructed with similar circuit parameters. A description of inverter circuit based on this architecture is given below which clearly illustrates the proposed architecture.

GFCAL INVERTER AND ITS OPERATION

The structure of an adiabatic inverter proposed by us is shown in Fig. 1. This circuit consists of one P-channel MOSFET and a diode in parallel with one N-channel MOSFET and a diode, which in turn are connected in series with the load capacitor C as shown in Fig. 1. The supply voltage V_{DD} is a slowly varying triangnlar voltage as shown in Fig. 2a. The P-channel MOSFET (T_1) and diode (D_1) provide charging path and N-channel MOSFET (T_2) and diode (D_2) provide discharging path for the load current. These diodes are used to prevent the currents to flow towards the unwanted directions. The importance and the role of the components T_1, D_1 and T_2, D_2 can be understood considering the four following cases with respect to rising and falling portions of V_{DD} as shown in Fig. 2a.

Case 1

Rising V_{DD} (portion a) with input zero (logic 0). In this case, T_1 is on and T_2 is off. Path T_1, D_1 allows the current flow from the supply and the capacitor gets charged close to the peak value of V_{DD}, producing logic 1.

Case 2

Falling V_{DD} (portion b) with input low (logic 0). As in case (1), T_1 is on and T_2 is off. This provides a conducting path via T_1, D_1. There is a possibility of charging of the capacitor if the output is less than $V_{DD}(t)$ and also a possibility to discharge back into the supply, if $V_C > V_{DD}$. But the diode

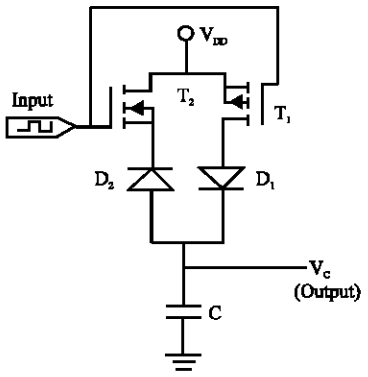

Fig. 1: Circuit of GFCAL inverter

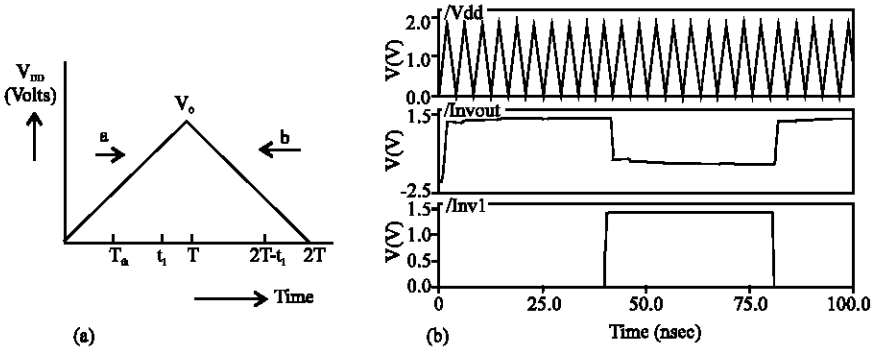

Fig. 2: (a) Supply and (b) typical input and output waveforms

D_1 does not allow discharge into the supply since it is reverse biased. Thus, path T_1, D_1 is only a charging path when the input is zero. This results in output voltage corresponding to logic 1, which is the compliment of input viz., logic 0.

Case 3

Rising V_{DD} (portion a) with input high (logic 1). When the input is logic 1, T_2 is on and T_1 is off. The path D_2, T_2 becomes conducting. The diode D_2 allows only discharging of capacitor if the output voltage is higher than $V_{DD}(t)$ while preventing the charging even if $V_{DD}(t)$ is greater than output voltage. Thus, during this portion, ouly discharging of the capacitor takes place or it may remain at the previous value. However, when falling of V_{DD} takes place as seen in the next case, the discharge of the load capacitor would be complete and the output assumes a value corresponding to logic 0.

Case 4

Falling V_{DD} (portion b) with input high (logic 1)). In this case, T_1 is off and T_2 is on. Path D_2, T_2 can allow current flow from the capacitor to the supply. If there is no charge on the capacitor (output voltage at logic 0), the output voltage remains in that state ouly. The diode, D_2 prevents charging of the capacitor since it is reverse biased when $V_{DD}>V_C$ and allows only discharging of the capacitor or pumping of energy back into the supply. Thus the capacitor voltage is brought down to a low value when the input is high irrespective of the previous output. Hence, output is the compliment of the input. These four cases clearly bring out the purpose of the transistors T_1, T_2 and diodes D_1, D_2.

Through these devices, charging path (T_1, D_1) and discharging path (D_2, T_2) for the capacitor are formed and charging and discharging are controlled by input voltages to T_1 and T_2. Further it is clear that the output voltage level is almost independent of the time at which the input voltage is applied with respect to the supply voltage as long as it is applied at a time before V_{DD} reaches the peak value. Thus, this circuit operates as an inverter.

The glitches in this circuit are avoided as the capacitor either charges or discharges depending ouly on the input conditions. Further, the circuit elements can be designed to make the output logic levels the same as the input logic levels. Thus, the circuit can be easily cascaded. The power saving in these circuits is because of (i) the supply voltage is a slowly varying voltage which results in saving of energy during charging and discharging, (ii) the energy stored in the load capacitor is pumped back into the supply for realizing logic 1 to logic 0 transition, (iii) there is no short circuit current from the supply to the ground at any time during the transition of logic 1 to logic 0 or logic 0 to logic 1 unlike in the CMOS circuits and (iv) the diode in the discharge path prevents current spikes from input data entering the load capacitor.

ESTIMATION OF ENERGY DISSIPATION IN GFCAL INVERTER

The energy dissipated in this inverter is calculated for a triangular supply voltage using the approximate expression derived by the authors.

Energy Dissipation During Charging

When the input is logic 0, the p-channel MOSFET, T_1 is on and as V_{DD} increases from 0 to V_0, the capacitor is charged through the diode D_1.

Consider the supply voltage V_{DD} as shown in Fig. 2a. The voltage reaches a peak value V_0 in a time period T and its value V_{DD} (t) at any time t is:

$$V_{DD}(t) = \frac{V_0}{T}t, \text{ When } 0 \le t \le T \tag{1}$$

$$= V_0[1 - \frac{(t-T)}{T}], \text{ When } T \le t \le 2T \tag{2}$$

The voltage $V_{DD}(t)$ reaches a value V_B in a period T_{th}, when the diode starts conducting. Let R_{ch} be the total resistance in the charging path.

The voltage V_C across the load capacitor C for $t>T_{th}$, is given by;

$$\frac{V_0}{T}t = V_B + R_{ch}C\frac{dV_C}{dt} + V_C \tag{3}$$

Solving the above equation and assuming that $T_{th} > C\ R_{ch}$, Energy E_{Ch} dissipated over the period 0-T in the diode and the transistor can be shown to be:

$$E_{Ch} \approx V_0 C(R_{ch}C\frac{V_0}{T} + V_B)(1 - \frac{V_B}{V_0}) \tag{4}$$

Energy Dissipation During Discharging

When the input is logic 1, the p-channel MOSFET is put off and charging of the capacitor is prevented. Since N-channel MOSFET is on, the capacitor discharges through D_2, T_2 till t_1 i.e., till V_C is higher than the supply by at least V_B, during the period when V_{DD} increases from 0 to V_0. The capacitor then stops discharging at t_1 and again continues discharging from $2T\text{-}t_1$ until $V_C = V_B$.

Let R_{dis} be the total resistance in the discharging path. Assuming $CR_{dis}<t_1$, the energy E_{dc} dissipated during discharging is the sum of energy dissipated during 0 to t_1 and $(2T\text{-}t_1)$ to 2T which can be shown to be;

$$E_{dc} = t_1(2\frac{V_0^2}{T^2}C^2R_{dis}) - 2C\frac{V_0}{T}BC\ R_{dis} + V_B BC + \frac{B^2}{2}C \tag{5}$$

Where:

$$B = V_{c0} - V_B + RC\frac{V_0}{T} \tag{6}$$

The total energy E_D, dissipated during one cycle of charging and discharging is given by

$$E_D = E_{ch} + E_{dc} = V_0 C(R_{ch}C\frac{V_0}{T} + V_B)(1 - \frac{V_B}{V_0}) + t_1(2\frac{V_0^2}{T^2}C^2R_{dis}) - 2C\frac{V_0}{T}BC\ R_{dis} + V_B BC + \frac{B^2}{2}C \tag{7}$$

Where, t_1 is given by

$$t_1 = RC\ In\left[\frac{V_{C0} - V_B + \frac{V_0RC}{T}}{\frac{V_0RC}{T}}\right] \quad (8)$$

From Eq. 7, which is the theoretical expression for energy dissipation during charging and then discharging, it is clear that the energy dissipated decreases as T increases. Also, T indicates the rate at which the supply voltage varies. So, the energy dissipated decreases with varying supply voltages (not constant V_{DD}).

RESULTS AND DISCUSSION

The experimental work essentially consists of simulating the circuit shown in Fig. 1 and measuring the energy drawn, energy pumped back and the logic levels that are obtained. The simulator used for this purpose is VIRTUOSO SPECTRE circuit simulator of cadence EDA Tools. The models used for this simulation are BSIM3V3 model parameters. The energy dissipated is calculated by subtracting the energy pumped back from the energy drawn. The theoretical and simulated values of energy dissipation for adiabatic inverter are shown in Table 1 for input data of 01, i.e., for one cycle of charging and discharging with the following circuit parameters. Length and Width of Transistor are 180 um and 720 mm, respectively and Value of load capacitance is 30 fF, Supply waveform is triangular and supply frequency is 25 MHz. The input signal is a square wave with frequency of 25 MHz. The peak supply voltage is fixed at 1.8 volts, which is enough to drive the transistors with reasonable logic values. The input logic 0 value is 0.45 volts and input logic 1 value is 1.4 volts. Along with the energy measurements, the out put logic values have been measured and found to be 0.45 volts and 1.4 volts corresponding to logic 0 and logic 1, respectively. From the Table 1, it is observed that for the adiabatic inverter, the simulated value of energy dissipation is comparable to the theoretical value obtained from Eq. 7.

With a view to compare this energy dissipation with that of CMOS inverter, the circuit of CMOS inverter is simulated. The supply voltage for this circuit is 1.8 volts, which is constant. The load capacitance, width and length of transistors, input data are the same as that of adiabatic inverter. The energy dissipated as measured is given in Table 1. The calculated energy dissipated ($C V^2$) in CMOS inverter for one cycle of charging and discharging is also given in Table 1 for the purpose of comparison. It may be seen that the measured energy dissipation is approximately the same as the calculated energy dissipation. From Table 1, for both the cases, it is clear that in our adiabatic inverter, the energy dissipation is ouly about 50% of that in CMOS inverter. The simulation of the circuit has been performed for supply frequencies up to 500 MHz and input data frequencies up to 250 MHz. Typical input and output waveforms for this circuit are shown in Fig. 2b.

Using this basic structure of the inverter, universal GFCAL gates namely NAND and NOR are realized as shown in Fig. 3. The energy dissipated in these gates are also compared with CMOS circuits constructed with similar circuit parameters. The simulation results of these gates at input frequency of 25 MHz are also given in Table 1 which indicates that the energy dissipated in adiabatic circuits proposed by us is about 50% compared to CMOS circuits. The simulation of the circuits has been performed for supply frequencies up to 500 MHz and input data frequencies up to 250 MHz. The functionality of the circuits is ensured by having the supply frequency higher than the frequency of input data when several gates are connected in cascade. The rise and fall times of the output waveform are decreased at higher value of supply frequency but with slight increase in energy dissipation.

Table 1: Comparison of energy dissipation during one cycle of charging and discharging for the proposed GFCAL and similar CMOS circuits at input frequency of 25 MHz

Name of the circuit	Measured energy (joules) per cycle	Logic 1	Logic 0	Calculated energy (joules) per cycle
GFCAL inverter	4.04E-14	1.40 V	0.45 V	4.38E-14
GFCAL nand gate	4.88E-14	1.40 V	0.45 V	4.83E-14
GFCAL nor gate	4.94E-14	1.40 V	0.45 V	4.87E-14
CMOS inverter	9.12E-14	1.78 V	0.00 V	9.72E-14
CMOS nand gate	1.15E-13	1.78 V	0.00 V	1.13E-13
CMOS nor gate	1.22E-13	1.78 V	0.00 V	1.13E-13

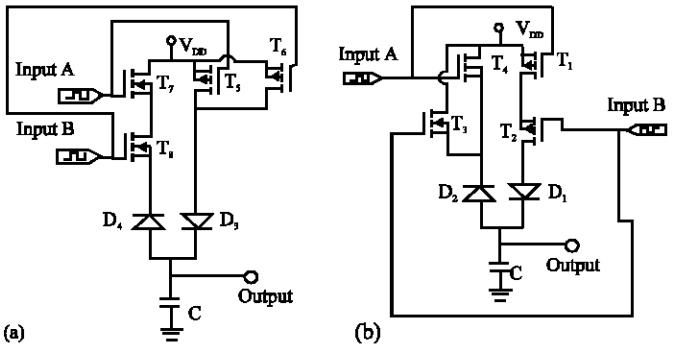

Fig. 3: (a) GFCAL NAND gate circuit and (b) GFCAL NOR gate circuit

CONCLUSION

This research reports an approach for realization of a family of adiabatic circuits consisting of two branches, one for charging and another for discharging of the capacitive load. The operation of the circuit has been explained through a simple theory. These circuits can be used in building hierarchical circuits as the input and output logic levels are the same, just like in the case of conventional digital circuits and there are no glitches. Further, all the circuits can be operated with a single power supply. These circuits have been found to result in about 50% of energy saving compared to CMOS circuits constructed with similar circuit parameters. We feel that these circuits may pave the way for extensive use of the adiabatic circuits in low power electronics.

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